
How to Wake-up Fast From an External Event on Cortex M0+ Based MCUs

Introduction

Microchip's 32-bit Arm® Cortex®-M0+ based microcontrollers provide features to reduce power consumption through different sleep modes, such as Idle, Standby, Backup and Off. When entering into sleep modes, the CPU is stopped, and some modules and clock domains are automatically switched off according to the selected Sleep mode. External events, such as interrupts from the ADC, RTC, DMA, and others can then be used to wake up the CPU and go back to Active mode.

Waking up the device from Sleep mode is not immediate and can differ according to the sleep modes, clocks, and peripherals used in the application.

This document describes wake-up time and how to configure the device to optimize the wake-up time. It also includes an appendix that describes a method to be used to measure the wake-up time.

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1. Wake-up Time

1.1 Principle

Wake-up time (also called *Response* time) is the time required to transit the CPU from Sleep mode to Active mode. Wake-up time is computed based on the occurrence of an external event to the first CPU instruction fetched in the interrupt handler. Depending on the sleep modes the CPU is in, the wake-up time also differs, for example, it will take more time for the CPU to recover from Standby Sleep mode, than from Idle Sleep mode. In addition to the sleep modes, other factors such as, peripheral event source, CPU clock source, and voltage regulator mode also have an impact on wake-up time. The following figures show the total wake-up time from different sleep modes (Idle and Standby) for a Cortex-M0+ based MCU:

Figure 1-1. Total Wake-up Time from Idle Mode

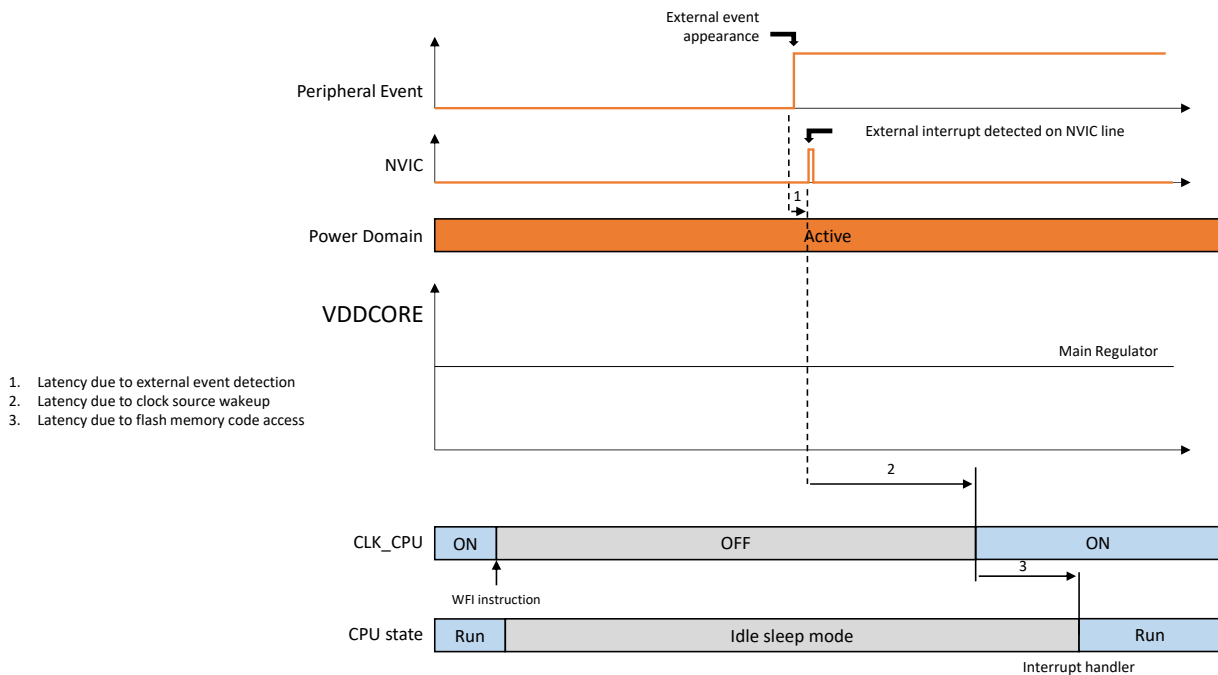
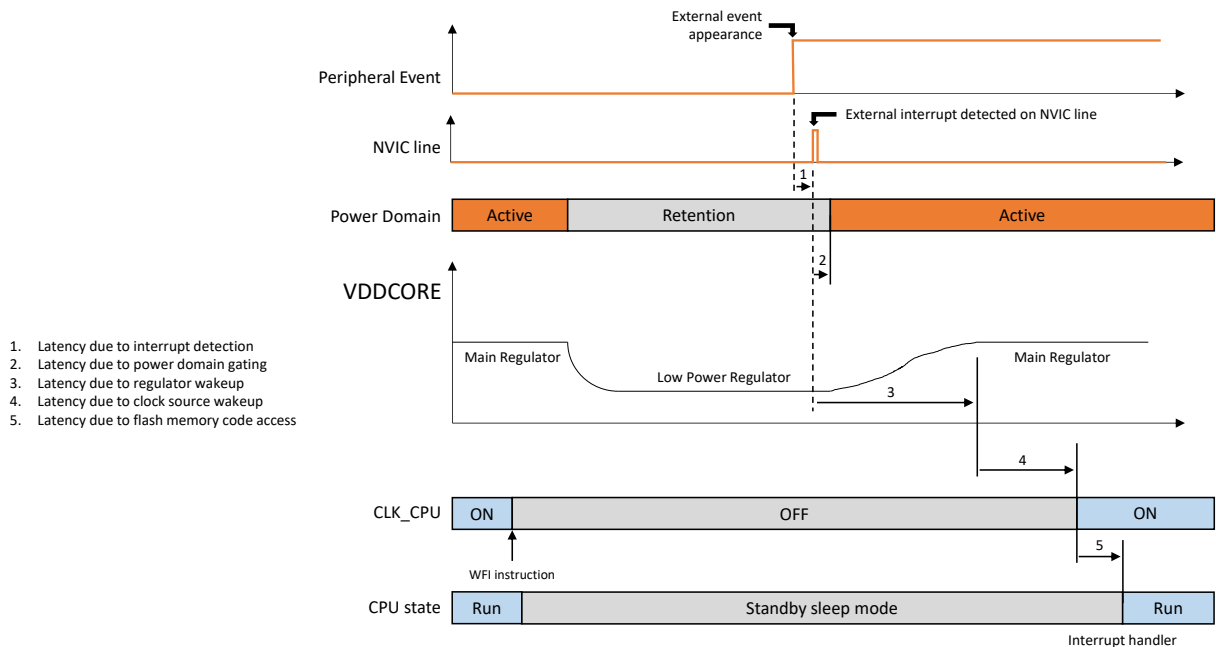


Figure 1-2. Total Wake-up Time from Standby Mode



The figures above highlight the typical elements that can influence the response time for all Microchip's Cortex-M0+ based MCUs:

- **Sleep mode:** If the device in the deeper sleep mode, it will take more time for wake-up. This is caused by the following elements:
 - The CPU clock is stopped during sleep modes.
 - **Voltage Regulator:** In Standby mode, the main voltage regulator is turned off (unless the user forces the voltage regulator to keep it active while in Standby mode) and the low-power voltage regulator is used instead depending on which configuration is used on the chip. This means, when the interrupt is detected, the low-power voltage regulator is turned off and the main voltage regulator requires time to switch on, which effects the total wake-up time of the device.
 - The main clock is running in Idle mode, but shut down while running on a deeper sleep mode
- **CPU clock source:** Peripherals and core require a specific number of asynchronous/synchronous clock cycles to perform wake-up and interrupt management actions. Using a higher clock frequency can decrease the wake-up time. In addition, the CPU wake-up time with internal oscillators (OSC8M and OSC48M) as clock source is less compared to the wake-up time with other clock sources (crystal oscillators, DFLLs, DPLLs). These other clock sources require time for their wake-up and initialization, therefore increasing the total wake-up time.
Note: Increasing the clock frequency can impact the power consumption during sleep mode.
- **Peripheral (interrupt source):** The peripheral used to generate the interrupt for waking-up the CPU can increase the response time. For example, the External Interrupt Controller (EIC) features level or edge detection, filtering and debouncing. If the interrupts are configured for level detection when filtering or debouncing are disabled, detection is done asynchronously. When filtering or synchronous edge detection or debouncing is enabled, the EIC automatically requests the GCLK_EIC or CLK_ULP32K to operate synchronously. Therefore, enabling filtering, debouncing or synchronous edge detection will require more clock cycles to detect the interrupt, which will increase wake-up time as shown by the following table. Due to these considerations, the user must ensure to configure the peripheral to detect interrupts as fast as possible and avoid adding time in the interrupt detection process.

Table 1-1. EIC Detection Latency

Detection mode	Latency (worst case)
Level without filter	Five CLK_EIC_APB periods
Level with filter	Four GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods

.....continued	
Detection mode	Latency (worst case)
Edge without filter	Four GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods
Edge with filter	Six GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods

- **Interrupt detection:** The Nested Vector Interrupt Controller requires time to detect an external event. For Cortex-M0+ based MCUs, it takes between 12 to 20 clock cycles to measure and identify the interrupt, hence the faster the CPU clock is running the quicker the wake-up time.
- **Power Domains:** Power domains allow for the shut down of sets of clocks during Standby mode to further reduce the power consumption at the cost of wake-up time. When using Power Domain Gating, changing a power domain from retention to active state will take time. If all power domains are already in Active mode during Standby mode, this latency is zero.
- **Non-Volatile Memory accesses:** When entering into Sleep mode, the NVM block is put into a power reduction mode that increases the wake-up time. If the MCU supports *Wake-up Instant* capability for the NVM, the NVM block exits Low-Power mode when exiting sleep and keeps wake-up time low while benefiting from low-power consumption.
- **Power Supply Voltage:** For application considerations, it is possible to provide different ranges of supply voltage for the chip, as long as the supply voltage provided respects the operating conditions of the CPU. However, supply voltage affects the wake-up time. According to Ohm's law ($V = R * I$), for a fixed resistance value, the higher the input voltage, the higher the load current will be, which provides better CPU performance and allows for faster wake-up.

Note: Increasing the power supply voltage will increase the current load in detriment of power consumption.

The total wake-up time obtained then depends on the elements listed above. There are other elements that affect the wake-up time that are not shown in the previous figures such as:

- **Wait States:** While running fast clocks on an MCU, the user must ensure to add a specific amount of wait-states according to the clock speed to synchronize read operations between the core and the NVM memory to avoid hanging the MCU while reading the NVM. These wait-states will hold the clock for few clock cycles which will increase the response time.
- **Cache memory:** Cache memory is a close-to-core volatile memory which allows the storage of a small amount of code for quick accesses. Due to its proximity with the CPU, there will be no wait states to launch handler instructions stored in the cache memory even if the device is configured to run at maximum frequency with wait states. This means the wake-up time will be decreased. However, if the device allows different wake-up sources, it may happen that the right handler is not stored in the cache before entering into Low-Power mode. Therefore, enabling cache memory will have no impact on wake-up time, or can increase the response time due to parallel storage of the instruction on a cache miss.

1.2 SAM C2x and SAM DA1/D09/D1x/D2x Family Specifics

The SAM C2x and SAM DA1/D09/D1x/D2x family of devices have similar architecture, but the following points differ across the SAM C2x and SAM DA1/D09/D1x/D2x devices which have an impact on the wake-up time:

- The SAM DA1/D09/D1x/D2x family of devices offer three levels of Idle mode (Idle0, Idle1 and Idle2) although the SAM C2x family of devices offers two levels of Idle mode.
 - Idle0 mode - Only switches off the CPU clock.
 - Idle1 mode - Turns off the APB clocks.
 - Idle2 mode - Turns off the AHB clocks.

The device will take more time to go from Idle2 mode to Active mode, than from Idle0 mode to Active mode.

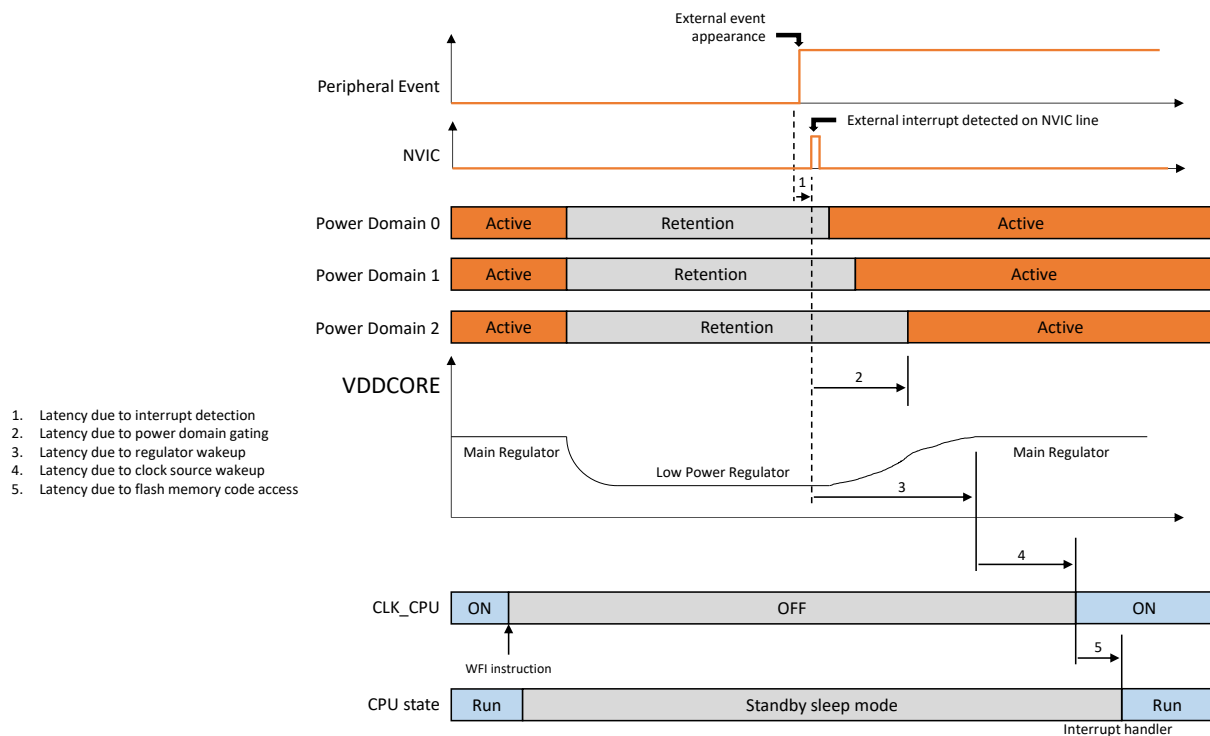
- The SAM C2x family of devices embed an OSC48M as an RC oscillator, but the SAM DA1/D09/D1x/D2x family of devices offers an 8 MHz RC oscillator clock source.
- The SAM C2x family of devices is a 5V tolerant MCU, while the SAM DA1/D09/D1x/D2x family of devices is a classical 3.3V MCU

1.3 SAM L2x Specifics

The SAM L2x family of devices offers a wide range of ultra low-power microcontrollers, which are based on the 32-bit Arm Cortex-M0+. On top of the SAM C2x and SAM DA1/D09/D1x/D2x Idle mode and Standby mode, the SAM L2x family of devices benefit from several other features, such as backup and off modes, power domain performance levels, specific voltage regulator. Each of these features has its impact on the global wake-up time:

- **Sleep mode (Backup and Off mode):** Backup mode and Off mode enables the SAM L2x family of devices to reduce power consumption. During Backup mode, only the backup domain is kept powered, allowing a few features to run (RTC, 32 kHz clock sources and wake-up from external pins). During OFF mode, the entire device is powered off and the entire chip needs to be reset for waking up.
- **Performance Level:** Two performance levels on the SAM L2x devices are PL0 and PL2. PL0 is aiming for the lowest power consumption by limiting the speed of the logic clock and CPU frequency, which increases the wake-up time. PL2 allows the chip to use full functionality and capabilities.
- **Voltage Regulator (LDO or Buck converter):** The SAM L2x family of devices embed two voltage regulators that can run in Active mode: LDO regulator and Buck converter. The Buck converter is the most appropriate regulator in terms of power efficiency. The LDO regulator can provide a fast response to a load change compared to the Buck converter, which makes it the fastest regulator to use for fast wake-up time considerations.

Figure 1-3. SAM L2x Family's Total Wake-up Time from Standby Mode



2. Optimizing the Wake-up Time

The following important elements must be considered for optimizing the wake-up time:

- Peripherals must be configured to detect or generate interrupts as fast as possible to avoid adding time in the interrupt detection process.
- The CPU local bus (IOBUS) feature is implemented in the Cortex-M0+ based MCUs. IOBUS is an interface that connects the CPU to the PORT. This single-cycle bus interface is generally used for low-latency operation. If the first instruction to be fetched by the device is a pin state modification, it is recommended to configure this pin through the PORT IOBUS register to lower the wake-up time.

2.1 SAM C2x and SAM DA1/D09/D1x/D2x Family of Devices

To optimize wake-up time on the SAM C2x and SAM DA1/D09/D1x/D2x family of devices, the following configurations must be applied to the device, depending on which sleep mode the device is using:

Wake up from Idle mode:

- VDD = 3.3V (VDD = 5.0V for SAM C2x)
- Idle0 mode
- OSC8M running at 8 MHz (OSC48M running at 48 MHz for SAM C2x) and feeding GCLK0
- Non-volatile memory in Wake-up Instant mode
- '0' wait-states (2 WS for SAM C2x)
- Cache memory is enabled

Wake up from Standby mode:

- VDD = 3.3V (VDD = 5.0V for SAM C2x)
- Standby mode
- OSC8M running at 8 MHz (OSC48M running at 48 MHz for SAM C2x) and feeding GCLK0
- Non-volatile memory in Wake-up Instant mode
- '0' wait-states (2 WS for SAM C2x)
- Cache memory is enabled
- Voltage Regulator is in Automatic mode

2.2 SAM L2x Family

To optimize the response time on the SAM L2x family of devices, the following configuration is recommended depending on which sleep mode the device is in:

Wake up from Idle mode:

- VDD = 3.3V
- OSC16M running at 12 MHz with 1 wait state
- Non-volatile memory in Wake-up Instant mode
- Cache memory is enabled
- Voltage regulator: LDO
- Performance Level 2

Wake up from Standby mode:

- VDD = 3.3V
- OSC16M running at 12 MHz with 1 wait-state
- Non-volatile memory in Wake-up Instant mode
- Cache memory is enabled
- Voltage regulator: LDO

- Voltage regulator is in Normal Operation mode
- Performance Level 0
- All power domains are forced active

Note:

1. The configurations listed above are optimized to benefit from the best wake-up time values while considering power consumption. The reason is a trade-off between fast wake-up and power consumption. Reducing the wake-up time will increase the power consumption and vice versa.
2. It is recommended to configure the chip with the configurations listed above before entering into sleep mode for optimizing the response time. Once the device is woken-up, it is possible to reconfigure the device (clock sources, peripherals and other chip configurations) to fit with application requirements.
3. This document is designed specifically for Cortex-M0+ devices, but it also covers many similar concepts in other Cortex families, hence it can be used as a reference for wake-up time optimization using other Cortex products.

3. Appendix A - Measuring Wake-up Time

Users can use different methods to measure the wake-up time. This section illustrates the most common method used to measure the wake-up time. The user needs to consider the following prerequisites are met before measuring the wake-up time:

Hardware Requirements:

- 1 x Microchip Xplained Pro board (SAM C2x Xpro, SAM L2x Xpro, SAM D1x Xpro and so on)
- 1 x Oscilloscope or 1 x Logic Analyzer

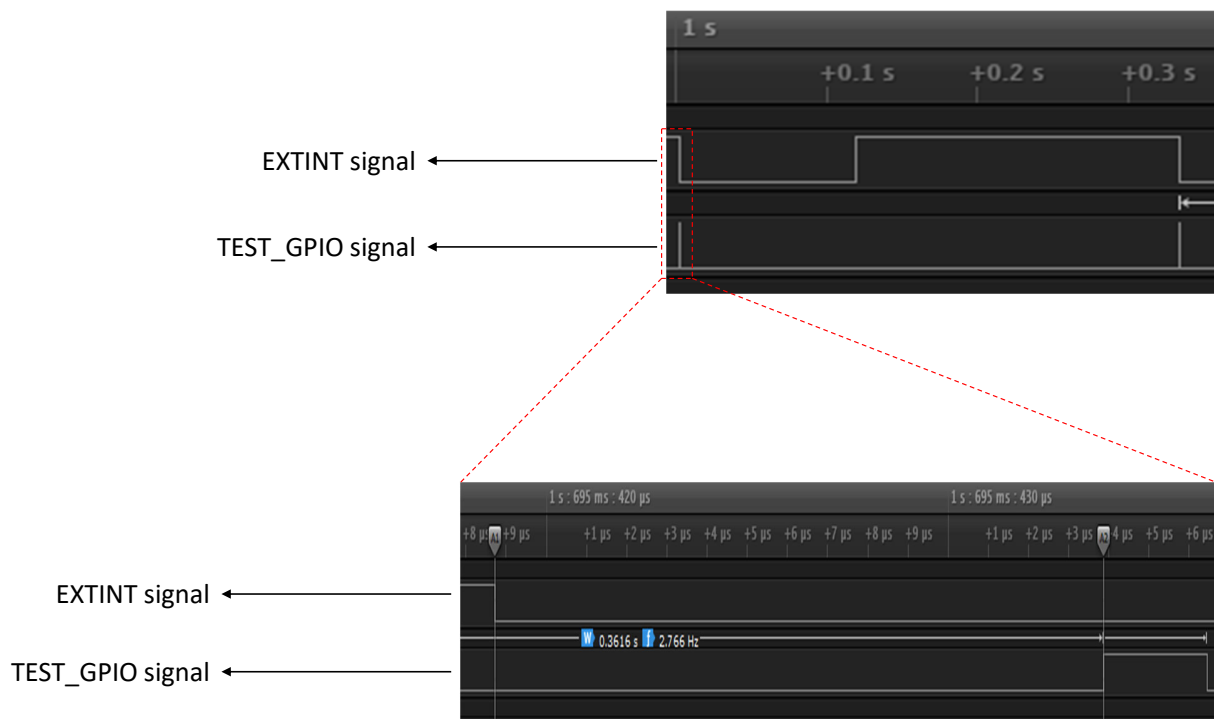
Note: This method described in this section can be applied to all Microchip Xplained Pro boards.

Follow these steps to measure the wake-up time using a SAM C21 Xplained Pro board and a Logic Analyzer:

1. The first pin, EXTINT, is configured as an external interrupt by using the External Interrupt Controller (EIC).
2. The second pin, TEST_GPIO, is configured as a GPIO in output low or high.
3. The oscilloscope (or logic analyzer) probes are connected to these two pins: TEST_GPIO and EXTINT.
4. A pulse is generated on TEST_GPIO after interrupt detection on the EXTINT pin.
5. The wake-up time is measured between the edge on EXTINT (wake up input) and the first edge on TEST_GPIO.

The following figures illustrates the process to measure the wake-up time using a SAM C21 Xplained Pro board and a Logic Analyzer:

Figure 3-1. Response Time Measurement on a Logic Analyzer



4. Conclusion

Reducing power consumption is important for cost reduction and increasing the battery life for an application. However, there is always a trade-off, and the right balance needs to be found between power consumption and wakeup time. To get the lowest wake-up time, the user must configure specific features of the device such as, sleep mode, CPU clock sources, NVM accesses and so on. It is recommended to configure the chip before entering into sleep mode to ensure a faster wake-up than to modify the device clock configuration while running in Active mode to fit with application requirements.

5. References

For additional information, refer to the following documents which are available for download from the Microchip website:

- SAM C2x Family Data Sheet:
 - <http://ww1.microchip.com/downloads/en/DeviceDoc/SAM-C20C21-Family-Datasheet-DS60001479C.pdf>
- SAM DA1/D09/D1x/D2x series Family Data Sheet:
 - <https://www.microchip.com/design-centers/32-bit/sam-32-bit-mcus/sam-d-mcus>
- SAM L2x Family Data Sheet:
 - <https://www.microchip.com/design-centers/32-bit/sam-32-bit-mcus/sam-l-mcus>

Note:

1. The SAM D5x family of devices are based on the Cortex-M4 architecture; however, this technical brief can be used as a source document for wake-up time optimization.
2. The SAM L1x family of devices are based on the Cortex-M23 architecture; however, this technical brief can be used as a source document for wake-up time optimization.

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