TB3295

Handling Cache Coherency Issues at Runtime Using Cache Maintenance Operations on Cortex-M7 MCUs Using MPLAB Harmony v3

Introduction

The cache coherency issue is inevitable on applications running on microcontrollers (MCUs) that have cacheable memory regions, which use Direct Memory Access (DMA) for data transfer operations. This is due to the CPU performing a read/write from the cache while the DMA transfers data between the peripheral and physical memory.

One of the methods to handle cache coherency requires the application to manage the cache at run-time using the Cortex-M7 cache maintenance operations. The Arm® Cortex® Microcontroller Software Interface Standard (CMSIS) provides cache maintenance Application Program Interfaces (APIs).

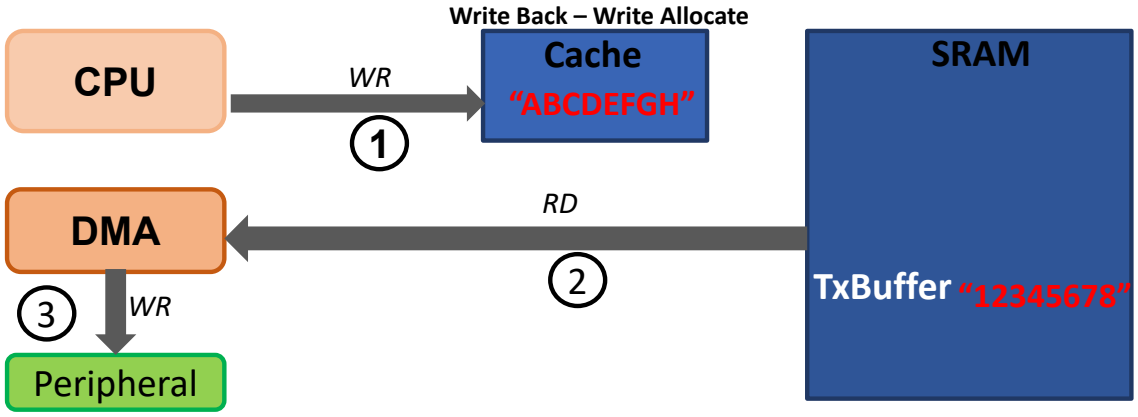
This document explains how an application can manage cache coherency issues at run time by using the CMSIS provided cache management APIs under MPLAB® Harmony v3.

Note: The concepts discussed in this document are common for all Arm Cortex-M7 MCUs, and the SAM E70 MCU is used as an example to discuss the concepts.

1. Description

The following figure illustrates the cache coherency issue as observed when the DMA reads from the SRAM on the SAME70 MCU.

Figure 1-1. Memory to Peripheral Transfer (DMA reads from SRAM)

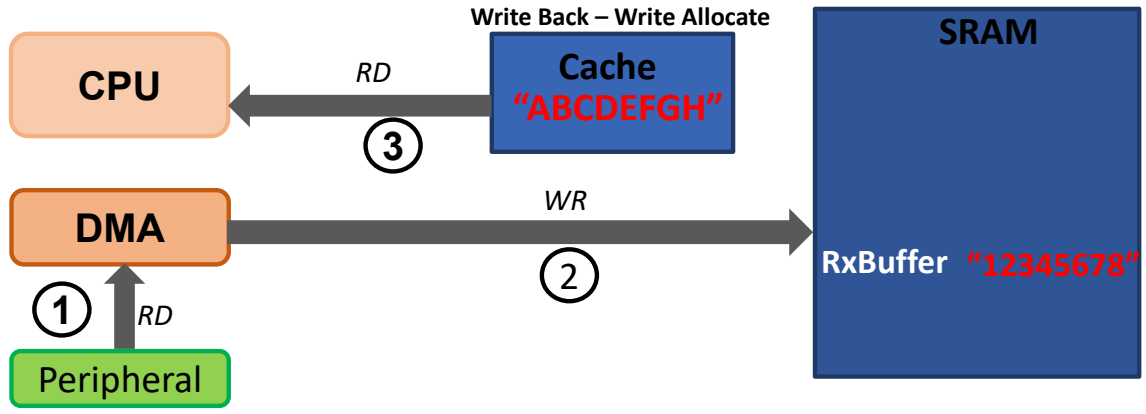


The application submits a request to transfer data buffer *TxBuffer* (value 'ABCDEFGH') to the peripheral. The CPU populates the DMA write buffer (*TxBuffer)* with the data to be written (value 'ABCDEFGH') to the peripheral. However, due to the set cache policy "Write Back and Write Allocate", the DMA write buffer (*TxBuffer*) may not be immediately written to the main memory, and the written data may remain in the data cache. The DMA write buffer (*TxBuffer*) in the main memory still contains the old value (12345678).

When the DMA is triggered to initiate the memory to peripheral transfer, the DMA reads the buffer (*TxBuffer*) from the main memory (12345678). As a result, the DMA ends up transferring stale data to the peripheral.

The following figure illustrates the cache coherency issue observed when the DMA writes to the SRAM.

Figure 1-2. Peripheral to Memory Transfer (DMA writes to SRAM)



The application submits a request to receive data in the *RxBuffer* (value '12345678') from the peripheral. The DMA populates the *RxBuffer* (with value '12345678') in the SRAM. However, the data cache is not updated, and it

continues to hold the previous data. When the CPU reads the *RxBuffer*, it ends up reading the previous value contained in the buffer (value 'ABCDEFGH').

1.1 Handling Cache Coherency

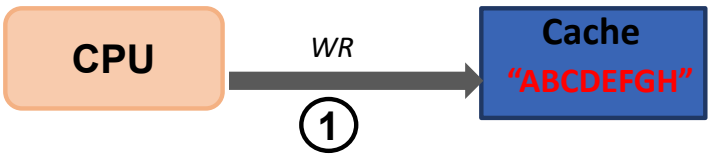
A method to handle the cache coherency issues illustrated in the figures Cache Coherency (DMA Reads from SRAM) and Cache Coherency (DMA writes to SRAM) involves the application to manage the cache at run-time using the Cortex-M7 cache maintenance operations. The operations include the ability to perform these actions:

- Enable or Disable the cache
- Invalidate the cache – Marks the cache lines as invalid. Subsequent access forces the data to be copied from the main memory to the cache.
- Clean the cache – Writes the cache lines, which are marked as dirty, back to the main memory

To handle the cache coherency discussed in Cache Coherency (DMA Reads from SRAM), perform the following actions:

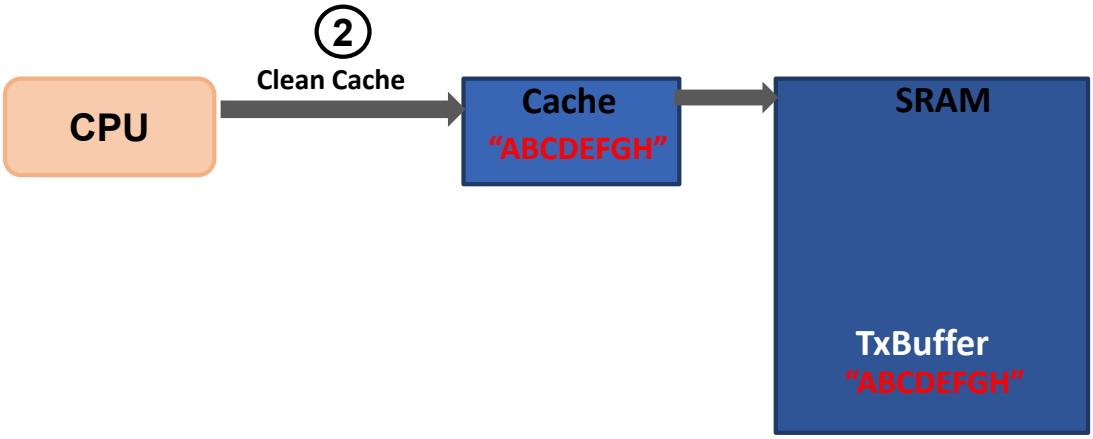
1. The application fills the write data buffer *TxBuffer* (value 'ABCEDFGH'). Due to the default cache policy (Write Back – Write Allocate), the written data may be in the cache.

   Figure 1-3. Populate Write Buffer



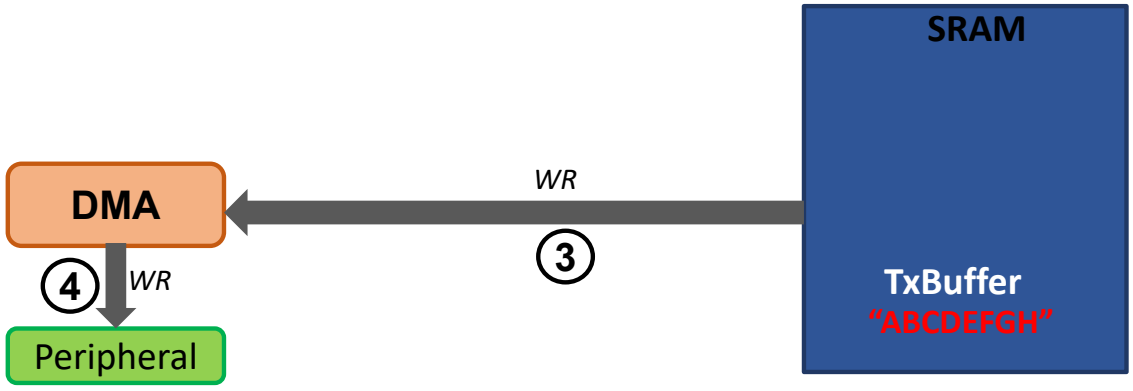
2. Flush the write data buffer *TxBuffer* (value 'ABCDEFGH') to the main memory by calling the clean cache API.

   Figure 1-4. Flush Write Buffer



3. The application submits a request to transfer data from the *TxBuffer* (value 'ABCDEFGH') to the peripheral.

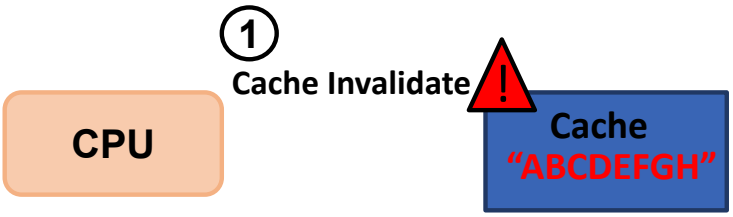
Figure 1-5. Write to Peripheral



To handle the cache coherency discussed in Cache Coherency (DMA writes to SRAM), perform the following steps:

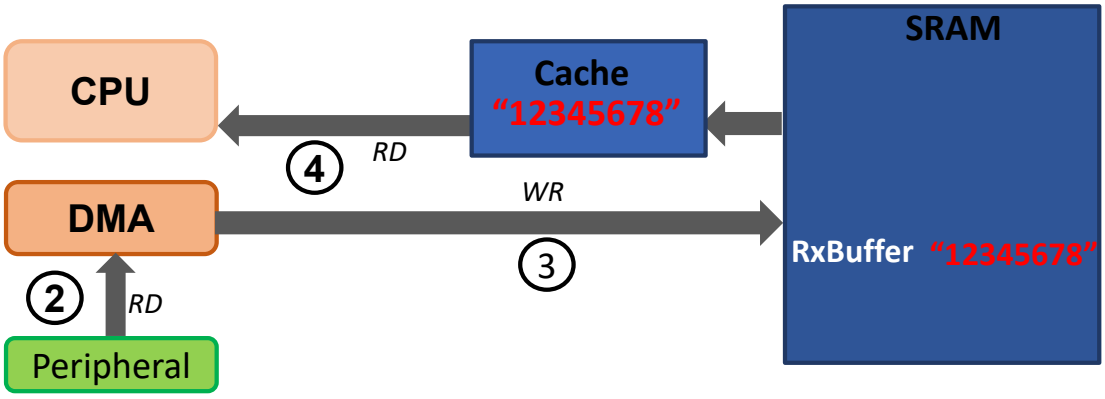
1. The application calls the 'Invalidate cache' API to mark the cache lines as invalid.

Figure 1-6. Invalidate Cache



2. The application submits a request to receive data in the *RxBuffer* (value '12345678') from the peripheral.
3. The DMA populates the *RxBuffer* (with value '12345678') in the SRAM.
4. Because the cache line corresponding to the *RxBuffer* is in an invalid state, a read access by the CPU results in the *RxBuffer* being copied from the main memory into the data cache.

Figure 1-7. Handle Peripheral to Memory Transfer Cache Coherency

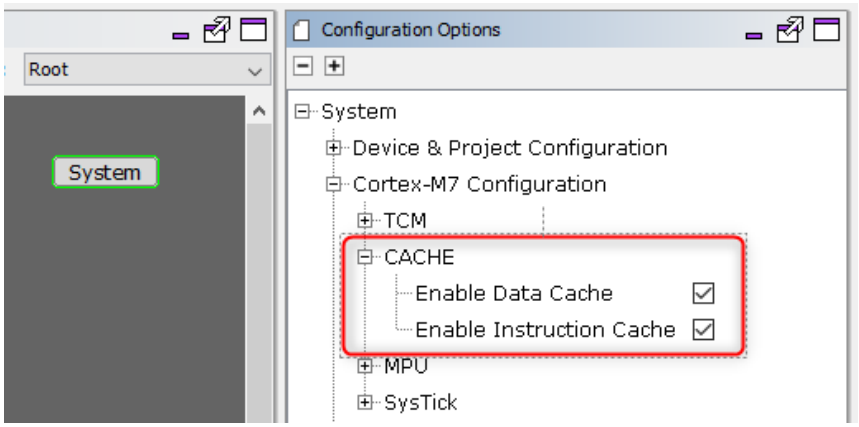


2. Implementation

2.1 Configuration

In an MPLAB Harmony v3 project for the SAM E70 MCU, by default the cache is enabled by the MPLAB Harmony Configurator (MHC). In MHC, the configuration setting can be found under *MHC project graph > System*.

Figure 2-1. MHC Cache Configuration



2.2 CMSIS Data Cache Maintenance APIs

The Cortex Microcontroller Software Interface Standard (CMSIS) provides the following D-Cache maintenance APIs:

Table 2-1. CMSIS Data Cache Maintenace APIs

Name	Description
SCB_EnableDCache (void)	Enables data cache. Invalidates the entire data cache before enabling it.
SCB_DisableDCache (void)	Disables data cache. Cleans the data cache to flush dirty data to the main memory before disabling the cache.
SCB_InvalidateDCache(void)	Invalidate the entire data cache
SCB_InvalidateDCache_by_Addr (uint32_t * addr, int32_t dsize)	Invalidate the data cache line by address.
SCB_CleanDCache(void)	Cleans the data cache.
SCB_CleanDCache_by_Addr (uint32_t *addr, int32_t dsize)	Cleans the data cache line by address.
SCB_CleanInvalidateDCache(void)	Cleans and Invalidates the entire data cache
SCB_CleanInvalidateDCache_by_Addr(uint32_t *addr, int32_t dsize)	Cleans and Invalidates the data cache line by address.

Notes: When using the *cache clean* and *cache invalidate by address* APIs:

- addr – Must be aligned to the cache line size boundary. This means that the DMA buffer address must be aligned to the 32-byte boundary.
- dsize – Must be a multiple of the cache line size. This means that the DMA buffer size must be a multiple of 32-bytes.

2.3 Example

The following code example demonstrates the usage of CMSIS data cache maintenance APIs along with the MPLAB Harmony v3 DMA peripheral library APIs to read and write data over the USART interface.

```
/* Buffers must be aligned to cache line boundaries and must be a multiple of cache line size
(32) */
char __attribute__ ((aligned(32))) TxBuffer[32];
char __attribute__ ((aligned(32))) RxBuffer[32];
int main ( void )
{
    /* Initialize all peripherals and modules */

    /* Fill the TxBuffer with the data to be transmitted.
       The TxBuffer may be in D-cache */
    memcpy((void *)TxBuffer, (const void *)"Microchip", sizeof("Microchip"));

    /* Flush the TxBuffer from D-cache to SRAM */
    SCB_CleanDCache_by_Addr((uint32_t *)TxBuffer, 32);

    /* Submit a DMA request to transfer data in the TxBuffer */
    XDMAC_ChannelTransfer(XDMAC_CHANNEL_0, TxBuffer,
        (const void *) USART1_TRANSMIT_ADDRESS, sizeof("Microchip"));

    /* Invalidate the RxBuffer in D-cache */
    SCB_CleanInvalidateDCache_by_Addr((uint32_t *)RxBuffer, 32);

    /* Submit a DMA request to receive 20 characters in the RxBuffer */
    XDMAC_ChannelTransfer(XDMAC_CHANNEL_1, (const void *) USART1_RECEIVE_ADDRESS,
        RxBuffer, 20);

    while ( true )
    {
        /* Application Code */
    }
    /* Execution should not come here during normal operation */

    return ( EXIT_FAILURE );
}
```

3. References

1. How to Create Non-Cacheable Memory Region on CortexM7 (SAM S70/ E70/ V70/ V71) MCUs Using MPLAB Harmony v3
2. Managing Cache Coherency on Cortex-M7 Based MCUs
3. Usage of XDMAC on SAM S/SAM E/SAM V
4. MPLAB Harmony v3 Quick Docs package provides standalone help pages for users to get started developing applications on Microchip's 32-bit SAM and PIC32 MCUs. Download the `quick_docs repo` and start with the `index.html` file present in the docs folder.
   The online version is available at microchip-mplab-harmony.github.io/quick_docs/.
5. MPLAB Harmony v3 Landing web page:
   www.microchip.com/mplab/mplab-harmony.

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