# AN 15.12

# Migrating from the LAN9115 to the LAN9210

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## OBJECTIVE

The purpose of this application note is to assist Microchip customers, with existing LAN9115 designs, when migrating to the new LAN9210 device. The LAN9210 will require a PCB change, which is necessary to support the HP Auto-MDIX PHY (even if this mode is not used) and the package change. This application note addresses all the differences between the LAN9115 and the LAN9210 devices, making this transition as easy as possible.

### References

- LAN9210 Data Sheet
- Reference Design for the LAN9210
- Reference Design for the LAN9115

### Overview of Changes Required

Figure 1 summarizes the changes needed to migrate from the LAN9115 to the LAN9210.

**TABLE 1: SUMMARY OF CHANGES REQUIRED**

| Change Required | Comments | References |
|---|---|---|
| New PCB | Needed to support footprint change, magnetics and passive component changes | This application note and Reference Designs available at www.microchip.com/. |
| New Magnetics | Needed to Support HP Auto-MDIX | See Application Note 8-13 for list of recommended magnetics. |
| Re-designed passive component network on PHY side of magnetics | Needed to Support Auto-MDIX PHY | This application note and Reference Designs for details. |
| Upgraded drivers | Recognize new device ID and to provide support for the Checksum Offload Engines | Drivers available at www.microchip.com/. |

## HARDWARE CHANGES

### Component Changes

#### MAGNETICS

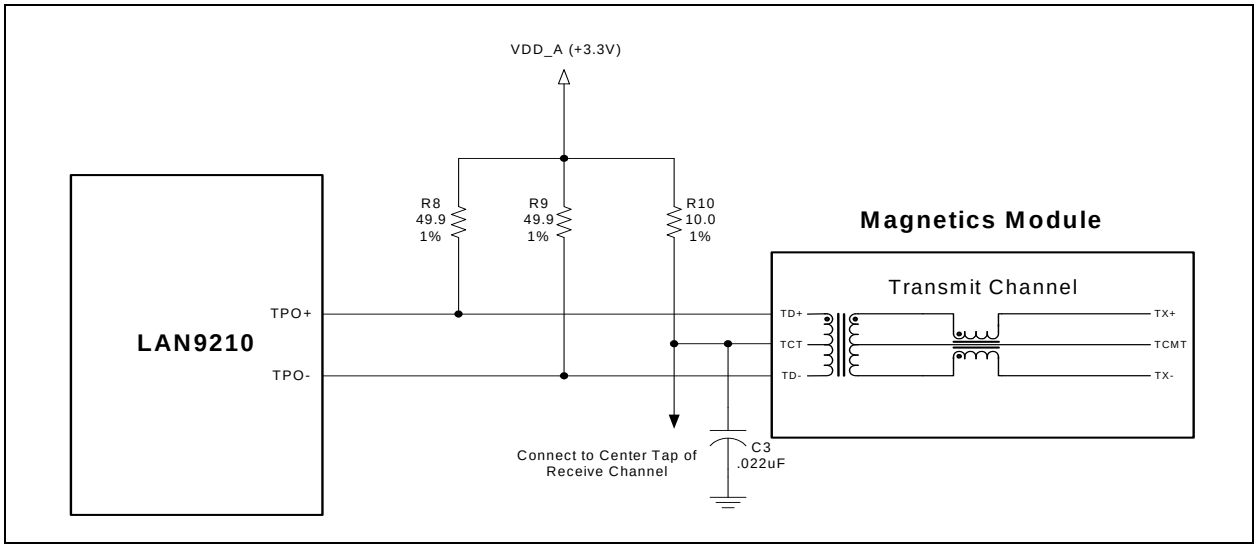
Migrating to the LAN9210 requires different magnetics than those used on the LAN9115. These magnetics have symmetrical channel configurations to allow for the switching of the receive and transmit channels. A list of suggested magnetics for the LAN9210 can be found in Application Note 8-13, entitled “Suggested Magnetics".

## Circuit Changes

### TRANSMIT CIRCUIT

The transmit circuit used by the LAN9210 is almost the same as the one used by the LAN9115. This circuit is shown in Figure 1 below.

**FIGURE 1: LAN9210 TRANSMIT CIRCUIT**




There are only two differences between the transmit circuit for the LAN9210 and the one previously used for the LAN9115:

- The LAN9210 uses magnetics that support HP Auto-MDIX.
- The device-side center tap of the transmit core (TCT) is attached to the device-side center-tap of the receive core (RCT).

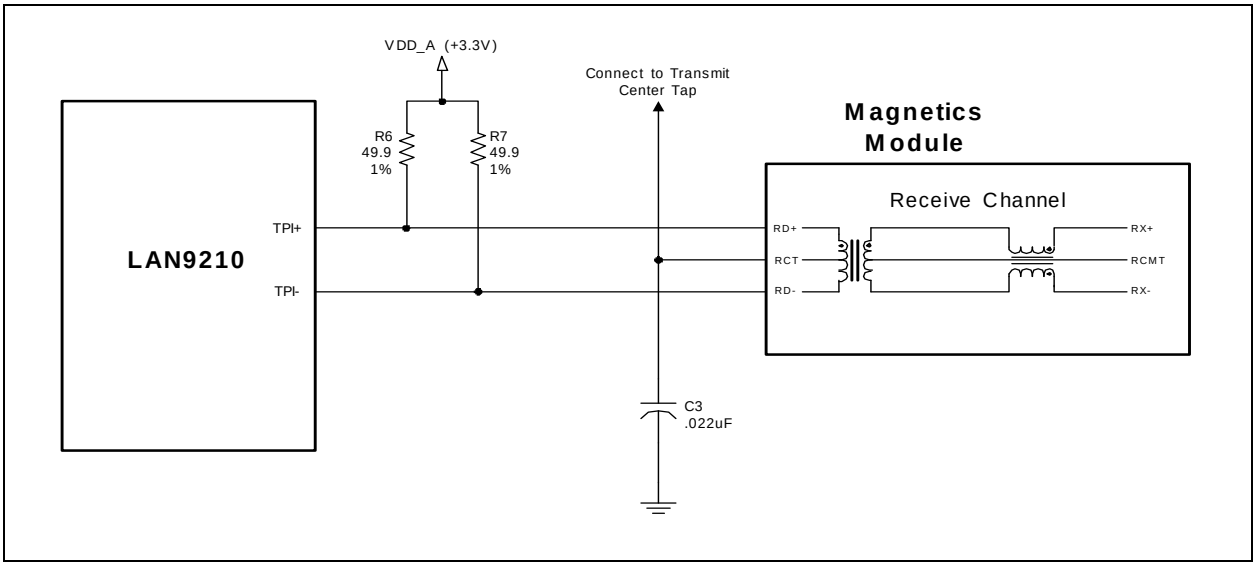
Like the LAN9115, the LAN9210 transmit circuit has the following features:

- A 49.9 ohm, 1% resistor from each side of the twisted pair to VDD_A (+3.3V)
- A 10 ohm, 1% resistor from the transmit center tap to VDD_A (+3.3V).

### RECEIVE CIRCUIT

The receive circuit used by the LAN9210 is slightly different from the one used by the LAN9115. This circuit is shown in Figure 2 below:

**FIGURE 2: LAN9210 RECEIVE CIRCUIT**




The similarities between the LAN9210 and the LAN9115 are as follows:

- Both designs have two 49.9 ohm, 1% resistors between the two signals in the twisted pair.

The differences between the LAN9210 and the LAN9115 are as follows:

- The LAN9115 had two 6.8nf capacitors, one in series with each side of the twisted pair. These are eliminated (shorted) in the LAN9210.
- In the LAN9115, the mid-point between the two 49.9 ohm resistors is tied to the center tap of the magnetics (RCT) and to a 0.01uF bypass capacitor to ground. In the LAN9210, both resistors are tied to VDD_A (+3.3V), and the 0.01uF bypass capacitor has been eliminated. The center-tap of the receive channel of the magnetics is tied to the transmit center tap (TCT) and to a common 0.022uF bypass capacitor to ground.

## Pin Changes

POWER AND GROUND

- The LAN9210 has a single ground (VSS) connection that is located on a 5.9mm x 5.9mm exposed pad on the underside of the device.
- The following LAN9115 power connections have been removed from the LAN9210:

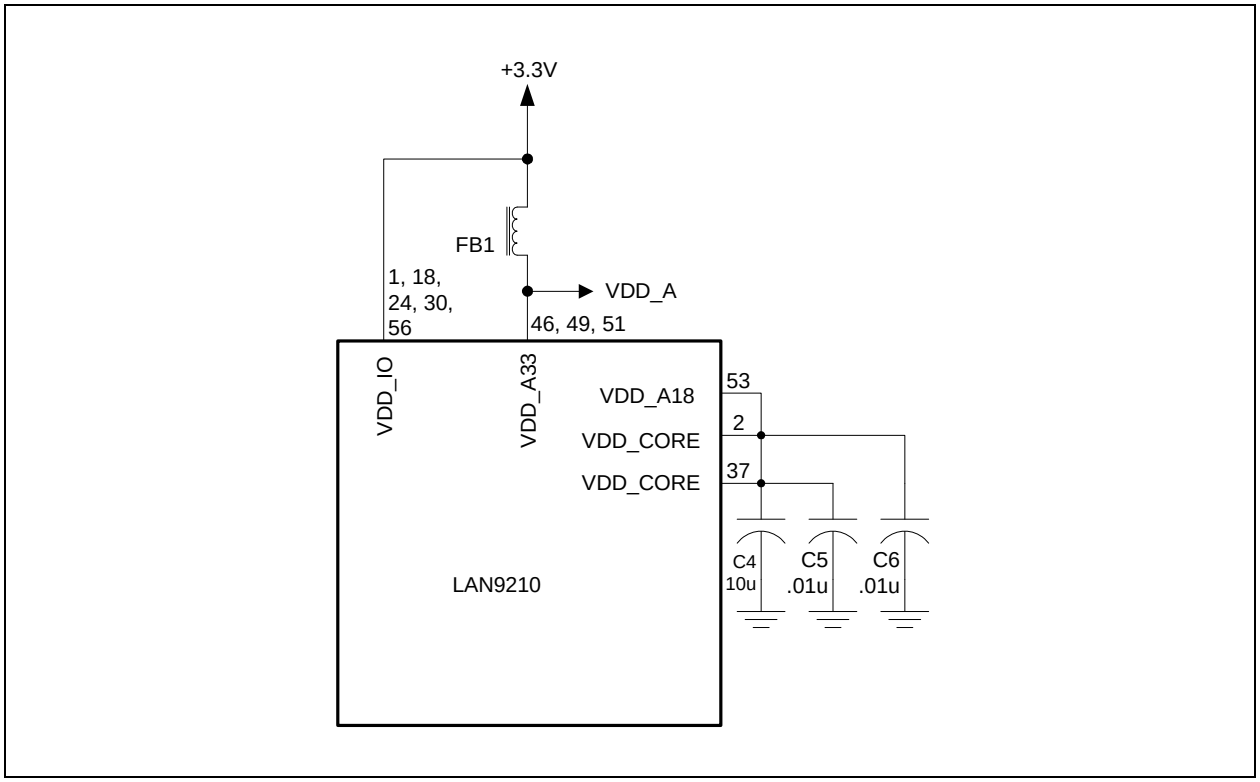
  VREG

  VDD_PLL

  VDD_REF

- The LAN9210 VDD_CORE pins 2 & 37, must still be connected together externally and then tied to a 10uF 0.1-Ohm ESR capacitor, in parallel with a 0.01uF capacitor to Ground next to each pin. In addition, it also needs to be connected externally to the VDD_A18 pin 53 See Figure 3.

**FIGURE 3: LAN9210 POWER CONNECTIONS**




## AMDIX_EN PIN (PIN 52)

This configuration pin allows hardware to enable or disable the HP Auto-MDIX feature. When pulled high, the feature is enabled. If pulled low or left floating, the feature is disabled. This pin can be overridden by the driver via the internal configuration registers.

## TWISTED PAIR INPUT AND OUTPUT PINS (TPI+, TPI-, TPO+, TPO-)

The inputs and outputs will reverse under either of the following conditions:

- HP AMDIX is enabled and the device detects a reversed connection
- A reversed (MDIX) connection is manually enabled by the driver.

## OTHER PIN CHANGES

- The SMI & MII ports are no longer externally available (LAN9115 pins 30, 31, 21-26, 29-33, 36-40, 75). on the LAN9210.
- SPEED_SEL, ATEST and RBIAS pins (74, 9, 10) have been removed.
- Figure 2 details the pin changes between the LAN9115 and LAN9210.

**TABLE 2: PIN CHANGE CROSS-REFERENCE**

| LAN9115 Signal | LAN9115 Pin | LAN9210 Signal | LAN9210 Pin | LAN9115 Signal | LAN9115 Pin | LAN9210 Signal | LAN9210 Pin |
|---|---|---|---|---|---|---|---|
| VDD_A | 81, 85, 89 | VDD_A33 | 46, 49, 51 | RXD[3:0] | 24, 23, 22, 75 | -- | -- |
| VDD_IO | 20, 28, 35, 42, 48, 55, 61, 97 | VDD_IO | 1, 18, 24, 30, 56 | TX_EN | 21 | -- | -- |
| VDD_CORE | 3, 65 | VDD_CORE | 2, 37 | nRESET | 95 | nRESET | 42 |
| VDD_REF | 8 | -- | -- | nRD | 92 | nRD | 15 |
| VDD_PLL | 7 | -- | -- | nWR | 93 | nWR | 16 |
| VREG | 2 | -- | -- | nCS | 94 | nCS | 17 |
| -- | -- | VDD_A18 | 53 | IRQ | 72 | IRQ | 43 |
| VSS_REF | 11 | VSS | Exposed Pad | pme | 70 | PME | 41 |
| VSS_PLL | 4 | VSS | Exposed Pad | FIFO_SEL | 76 | FIFO_SEL | 13 |
| GND_CORE | 1, 66 | VSS | Exposed Pad | SPEED_-SEL | 74 | -- | -- |
| GND_IO | 19, 27, 34, 41, 47, 54, 60, 96 | VSS | Exposed Pad | RBIAS | 10 | -- | -- |
| VSS_A | 77, 80, 86, 88 | VSS | Exposed Pad | -- | -- | AMDIX_EN | 52 |
| A[7:1] | 12 - 18 | A[7:1] | 6 - 12 | ATEST | 9 | -- | -- |
| D[15:0] | 43-46, 49-53, 56-59, 62-64 | D[15:0} | 19-23, 25-29, 31-36 | GPIO[2:0] | 100, 99, 98 | GPIO[2:0] | 5, 4, 3 |
| TX_CLK | 40 | -- | -- | EECLK | 69 | EECLK | 40 |
| TXD[3:0] | 36, 37, 38, 39 | -- | -- | EEDIO | 67 | EEDIO | 38 |
| COL | 33 | -- | -- | nEECS | 68 | EECS | 39 |
| CRS | 32 | -- | -- | EXRES1 | 87 | EXRES1 | 50 |
| MDC | 31 | -- | -- | TPO+, TPO- | 79, 78 | TPO+, TPO- | 45, 44 |
| MDIO | 30 | -- | -- | TPI+, TPI- | 83, 82 | TPI+, TPI- | 48, 47 |
| RX_DV | 29 | -- | -- | XTAL1, XTAL2 | 6, 5 | XTAL1, XTAL2 | 55, 54 |
| RX_CLK | 26 | -- | -- | NC | 71, 73, 84, 90, 91 | NC | 14 |
| RX_ER | 25 | -- | -- | | | | |

## Register Changes

SYSTEM CSR REGISTER CHANGES

ID_REV—Chip ID and Revision (offset 50h)

- Bits 31-16 (Chip ID) have changed to 9210h.

HW_CFG—Hardware Configuration Register (offset 74h)

- Bit 29 has changed from reserved to **FIFO Port Endian Ordering (FPORTEND).** This control bit determines the endianess of RX and TX data FIFO host accesses when accessed through the RX/TX Data FIFO ports, including the alias addresses (any access from 00h to 3Ch). When this bit is cleared, data FIFO port accesses utilize little endian byte ordering. When this bit is set, data FIFO port accesses utilize big endian byte ordering.
- Bit 28 has changed from reserved to **Direct FIFO Access Endian Ordering (FSELEND).** This control bit determines the endianess of RX and TX data FIFO host accesses when accessed using the FIFO_SEL signal. When this bit is cleared, FIFO_SEL accesses utilize little endian byte ordering. When this bit is set, FIFO_SEL accesses utilize big endian byte ordering.
- Bit 24 has changed from reserved to **AMDIX_EN Strap State**. This read-only bit reflects the state of the AMDIX-_EN strap pin (pin 52). This pin can be overridden by PHY Registers 27.15:13.
- Bits 6:5 have changed from **PHY_CLK_SEL** to reserved.
- Bit 4 has changed from **SMI_SEL** to reserved.
- Bit 3 has changed from **EXT_PHY_DET** to reserved.
- Bit 2 has changed from **EXT_PHY_EN** to reserved.

Word_Swap—Word Swap Control (offset 98h)

- This register has been changed from Endian Control to Word Swap Control
- This register controls how words from the host data bus are mapped to the CSRs and Data FIFOs inside the LAN9210. The LAN9210 always sends data from the Transmit Data FIFO to the network so that the low order word is sent first, and always receives data from the network to the Receive Data FIFO so that the low order word is received first.
- If this field is set to 00000000h, or anything except 0xFFFFFFFFh, the LAN9210 maps words with address bit A[1]=1 to the high order words of the CSRs and Data FIFOs, and words with address bit A[1]=0 to the low order words of the CSRs and Data FIFOs. If this field is set to 0xFFFFFFFFh, the LAN9210 maps words with address bit A[1]=1 to the low order words of the CSRs and Data FIFOs, and words with address bit A[1]=0 to the high order words of the CSRs and Data FIFOs.

MAC CSR REGISTER CHANGES

COE_CR—Checksum Offload Engine Control (index Dh)

- This register has been added to the MAC CSR at index Dh.
- The LAN9210 contains two checksum offload engines which offload the calculation of the 16-bit checksum for transmitted and received Ethernet frames. The functionality of the COE is described in the LAN9210 Data Sheet, section 3.6.

PHY REGISTER CHANGES

PHY Identifier 2 (offset 3)

- The default value has changed from C0D1h to C0C3h.

Special Control/Status Indications (offset 27)

- Bit 15 has changed from reserved to **Override AMDIX Strap:**

  0 - AMDIX_EN (pin 52) enables or disables HP Auto MDIX.

  1 - Override pin 52. PHY Register 27.14 and 27.13 determine MDIX function.

- Bit 14 has changed from reserved to **Auto-MDIX Enable.** It is only effective when 27.15 = 1, otherwise it is ignored.

  0 = Disable Auto-MDIX. 27.13 determines normal or reversed connection.

  1 = Enable Auto-MDIX. 27.13 must be set to 0.

- Bit 13 has changed from reserved to **Auto-MDIX State.** It is only effective when 27.15 = 1, otherwise it is ignored.

  **When 27.14 = 0** (manually set MDIX state)

  0 = no crossover (TPO = output, TPI = input)

  1 = crossover (TPO = input, TPI = output)

  **When 27.14 = 1** (automatic MDIX)

  This bit must be set to 0. Do not use the combination 27.15=1, 27.14=1, 27.13=1.

**TABLE 3: PHY REGISTER 27 SUMMARY**

| Bit 15 | Bit 14 | Bit 13 | Result |
|---|---|---|---|
| 0 | X | X | Pin 52 Enables or Disables the HP Auto MDIX function. |
| 1 | 1 | 0 | Override Pin 52, Enable Auto-MDIX |
| 1 | 0 | 0 | Disable Auto-MDIX. Force normal (MDI) connection.<br>TPO = transmit, TPI = receive |
| 1 | 0 | 1 | Disable Auto-MDIX. Force reverse (MDIX) connection<br>TPO = receive, TPI = transmit |
| 1 | 1 | 1 | Illegal combination, do not use. |

## DRIVER SUPPORT

- Drivers are available for the following platforms:

  WinCE 5.0 - XScale (PXA270)

  Linux - XScale (PXA270)

  Linux - SH3

- Please, visit our website for the latest drivers and development support, https://www.microchip.com/.

## APPENDIX A: APPLICATION NOTE REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision Level & Date | Section/Figure/Entry | Correction |
|---|---|---|
| DS00002926A (01-17-19) | Replaces the previous SMSC version, Rev. 0.1 (04-05-13) | |

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