AN1859

PCB Layout Guide for MEC140x/MEC141x

Author: Tom Tse
Microchip Technology Inc.

INTRODUCTION

This application note provides information on design considerations for a printed circuit board (PCB) for the Microchip MEC140x / MEC141x family devices including the MEC1404, MEC1406, MEC1408, MEC1414, MEC1416, MEC1418.

The design of the PCB requires care to provide good supply and ground paths; in addition, other design issues are addressed in this document.

The functional blocks in the MEC140x / MEC141x have different requirements for routing and external connections, which are also outlined in this application note.

Please see References for device-level information such as V_{CC1} power planes, and mechanical package information for the 128-Pin VTQFP and 144-Pin WFBGA.

This document includes the following topics:

Audience

This document is written for a reader that is familiar with hardware design. The goal of this application note is to provide information about sensitive areas of the MEC140x / MEC141x PCB layout.

References

The following documents should be referenced when using this application note. Please contact your Microchip representative for availability.

- Microchip MEC140x / MEC141x Data Sheet / eSPI Addendum
- Microchip MEC140x / MEC141x EVB ASSY. 6757A
- Microchip MPLAB ICD3 In-Circuity Debugger User's Guide (Doc#: DS51766B)
- Microchip AN2137 - PWM Controlled Fan fro MEC140x/MEC141x White Paper
- PCI Local Bus Specification (see www.pcisig.com)
- I^2C-bus specification and user manual, Rev. 6 - 4 April, 2014 or later (see www.nxp.com/documents/user_manual/UM10204.pdf)
- Intel, Enhanced Serial Peripheral Interface (eSPI) Specification (for Client Platform)
- Microchip "eSPI Controller" Specification, DS00002012A

Package Information

The MEC140x / MEC141x device is currently available in the following package:

- MEC140x / MEC141x for 128-pin, VTQFP
- MEC140x / MEC141x for 144-pin, WFBGA

1.0 GENERAL LAYOUT CONSIDERATIONS

This section describes layout considerations for the MEC140x / MEC141x device. This includes the following topics:

- Section 1.1, "Decoupling Capacitors," on page 2
- Section 1.2, "32.768kHz Crystal Oscillator," on page 4
- Section 1.3, "CAP Pins, AVSS/GND Connection," on page 6
- Section 1.4, "BGA Package PCB Layout Considerations," on page 6

1.1 Decoupling Capacitors

This section includes the following topics:

- Section 1.1.1, "MEC140x / MEC141x VTQFP Capacitors," on page 2
- Section 1.1.2, "MEC140x / MEC141x WFBGA Capacitors," on page 3

Decoupling capacitors should be placed as close to the chip as possible to keep series inductance low. When the capacitors are mounted on the bottom side of the PCB, the capacitors are connected to the ground plane from the bottom layer directly using the shortest path to the device. Each VCC pin should have a 0.1 µF capacitor located as close to the pin as possible. Bypass capacitors should be placed close to the supply pins of the MEC140x / MEC141x with short and wide traces.

The MEC140x / MEC141x has an integrated voltage regulator to supply the core circuitry. Decoupling this regulator requires a critical capacitor of 1µF on the CAP pin. ESR of this 1µF capacitor, including the routing resistance, must be less than 100 mOhm.

Capacitors may carry large currents that generate magnetic fields, inducing noise on nearby traces. Sensitive traces such as the 32kHz crystal should be separated by at least five times the trace width from decoupling capacitors when possible.

Connecting decoupling caps to power and ground planes using two vias per pad will reduce series inductance.

- FIGURE 1-1: on page 3 shows decoupling for the MEC140x / MEC141x 128-pin VTQFP.
- FIGURE 1-2: on page 4 shows decoupling for the MEC140x / MEC141x 144-pin WFBGA.

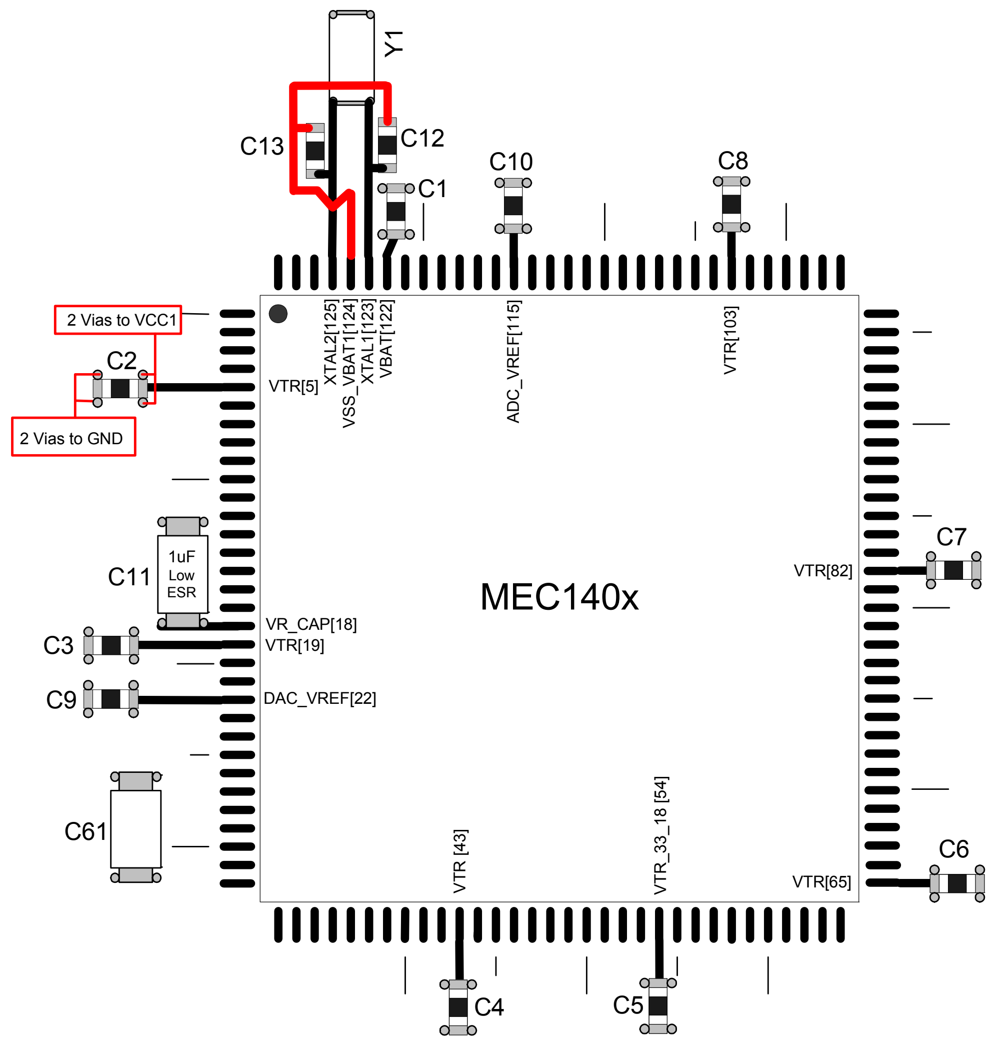
The VCC pin decoupling capacitors can use any typical 16V 10% Ceramic. See also the MEC140x / MEC141x EVB Schematics and Bill of Materials.

1.1.1 MEC140X / MEC141X VTQFP CAPACITORS

- Figure 1-1 shows decoupling for the MEC140x / MEC141x 128-pin VTQFP package.

Note:	The capacitors can use any typical 16V 10% ceramic.

FIGURE 1-1: MEC140X / MEC141X DECOUPLING IN 128-PIN VTQFP PACKAGE



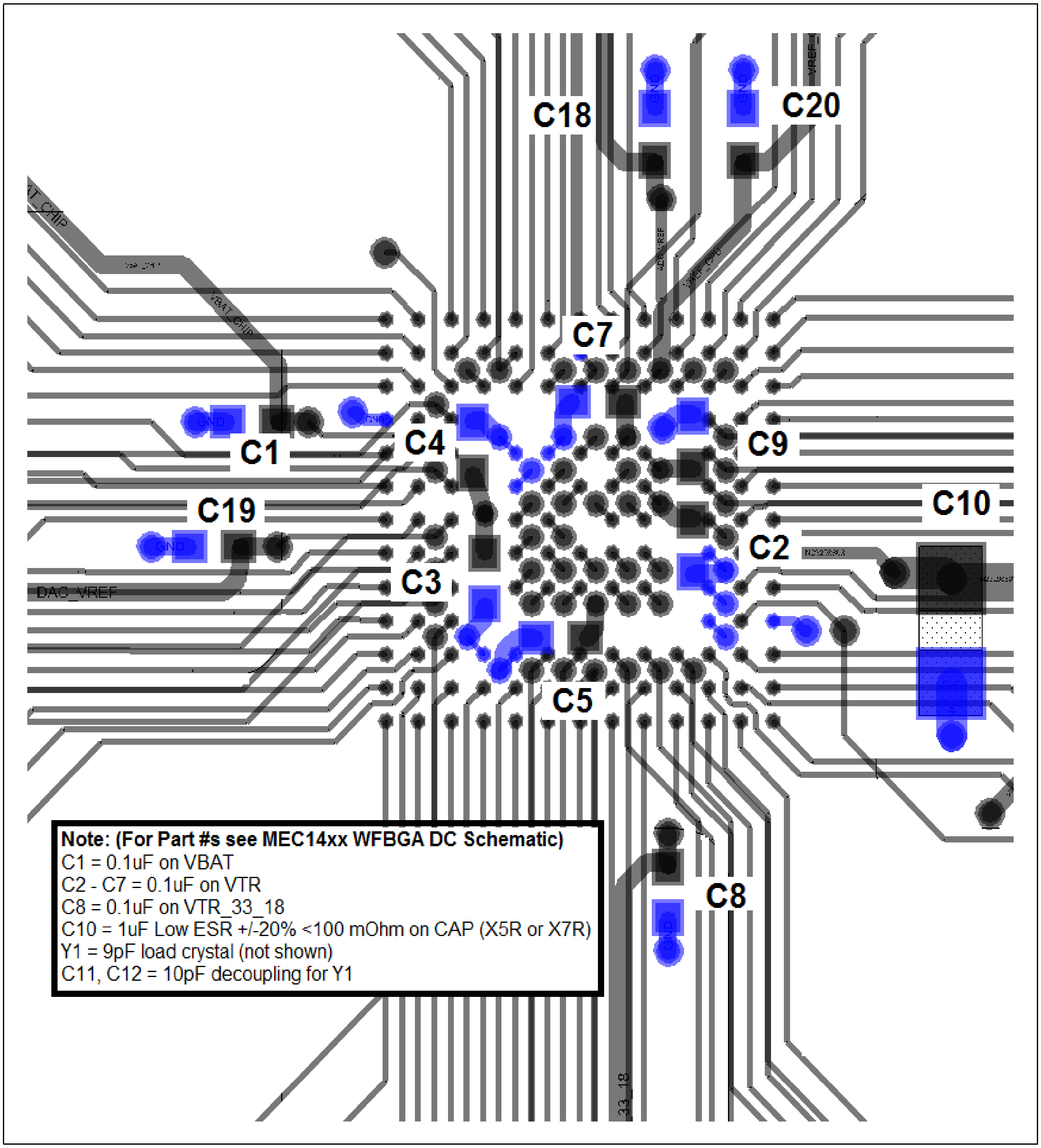
Note: (For Part Numbers see MEC140x EVB Schematic)
C1= 0.1uF on VBAT
C2 – C8 = 0.1uF on VTR
C9 = 0.1uF on DAC_VREF
C10 = 0.1uF on ADC_VREF
C11 = 1uF Low ESR +/-20% <100 mOhm on CAP (X5R or X7R)
Y1 = 9pF load crystal, C12 & C13 are 10pF
C61 = 10uF on VTR- place between MEC140x and VTR source

1.1.2 MEC140X / MEC141X WFBGA CAPACITORS

- Figure 1-2 shows decoupling for the MEC140x / MEC141x 144-pin WFBGA package.

Note:	The capacitors can use any typical 16V 10% ceramic.

FIGURE 1-2: MEC140X / MEC141X DECOUPLING IN 144-PIN WFBGA PACKAGE



1.2 32.768kHz Crystal Oscillator

This section describes specific layout and design considerations for the 32.768kHz crystal oscillator; this can be used to source the internal 32kHz clock domain, in lieu of the silicon oscillator or an external pin. The crystal implementation is required to support the RTC function within the MEC140x / MEC141x.

1.2.1 32.768KHZ CRYSTAL OSCILLATOR LAYOUT

The MEC140x / MEC141x 32kHz crystal oscillator is designed to generate an synchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5 µW typical), stability and minimum jitter using a general purpose parallel resonant 32kHz crystal. For a suggested part number, please see the MEC140x / MEC141x EVB schematic (see References).

This unique low power crystal oscillator drive circuit means that a standard inverter crystal layout should not be used. The design has been characterized to allow a variation of 4pF to 18pF on each pin. Based on the following load capacitance calculation, Microchip recommends 10pf load capacitors with a crystal that has a 9pf Cl rating. Other than these capacitors, no additional external components are required for normal operation of the clock circuit.

$$Effective\ Load\ Capacitance = C1 = \frac{[C11 + Cpin\_xtal2][C12 + Cpin\_xtal1]}{C11 + Cpin\_xtal2 + C12 + Cpin\_xtal1} + Cbrd$$

Where:

- C12 is the cap from pin XTAL1 to ground.
- C13 is the cap from pin XTAL2 to ground.
- Cpin_xtal2 is the pin capacitance of pin XTAL2. This is estimated to be 5pf (Note 1-1).
- Cpin_xtal1 is the pin capacitance of pin XTAL1. This is estimated to be 3pf (Note 1-1).
- Cbrd is estimated at 1.5pF.

Note 1-1 At the time of publication, the MEC140x / MEC141x silicon has not been characterized. Please check with your Microchip FAE for final pin capacitance values after silicon validation is complete. Any variation from the estimates provided here could change the crystal Cl value requirement.

1.2.2 CRYSTAL ACCURACY

The accuracy of the 32kHz input translates directly into accuracy of the internal clock and the functions in the MEC140x / MEC141x using the 32kHz: 32KHZ_OUT, week timer, hibernation timers, and so forth.

The accuracy, with regard to actual error in time can be illustrated as such: +/-1ppm of error in frequency corresponds to 32.768 kHz x 1ppm x 10^{-6} = +/-0.032768 Hz. This translates into ~1 µsec/sec or ~+/-0.086 sec/day.

Based on customer RTC accuracy timer requirements, Microchip recommends using a +/-20ppm crystal. This would equal approximately +/-2 sec/day, other factors discounted.

For arguments sake, it is safe to say that stray capacitance is difficult to calculate exactly. So, as an exercise in completeness, this calculation describes the effect of each picofarad of additional capacitance over/under the crystal C_{load} value:

$$ppm/pF = \frac{C_1\,x\,10^6}{2(C_O + C_L)^2}$$

where C_0 is the shunt capacitance, C_1 is the motional capacitance and C_L is the load capacitance of the chosen crystal (these numbers can be found in the crystal data sheet). For example, using a crystal with C_0 = 0.8pF, C_1 = 0.0019pF, C_L = 12.5pF, we get a shift of 5.37ppm/pF. So, in terms of time, each pF of added/subtracted capacitance is approximately 5.37 x 0.086 = +/-462 msec/day for this particular crystal.

This example is meant to illustrate the magnitude of the potential error. In practice, slight capacitance mismatch does not equate to many seconds a day.

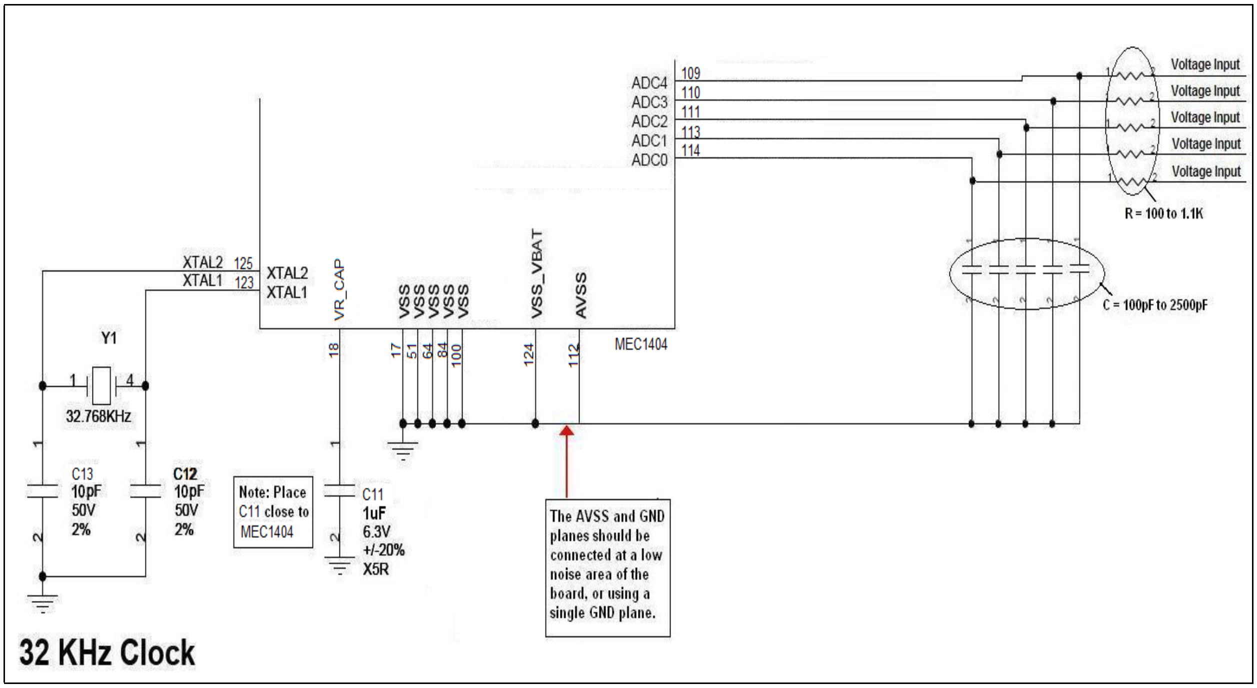
1.2.3 SINGLE ENDED CLOCKING

An external clock source (maximum voltage of 3.3V) may be applied to the XTAL2 pin if the XOSEL bit in Clock Enable Register configures as a single-ended 32.768 kHz clock input (SUSCLK). The XTAL1 pin should be left floating. If an external clock source is used, the designer must ensure that the source is available in all desired power states in which the EC will be active.

1.3 CAP Pins, AVSS/GND Connection

The recommended filtering for the CAP pin on the MEC140x / MEC141x is shown in Figure 1-3, for VTQFP connections. The filtering components shown should be placed close to the device and away from noise sources.

FIGURE 1-3: VTQFP CAP PIN REFERENCE AND AVSS DIRECTLY CONNECTED TO GND



1.4 BGA Package PCB Layout Considerations

The MEC140x / MEC141x devices have BGA lead-free RoHS-Compliant package as follows:

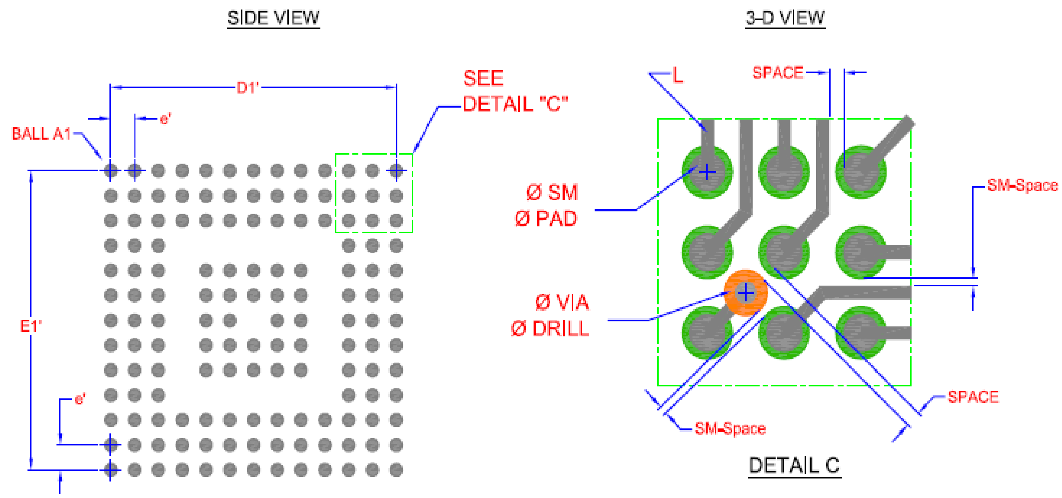
- 144-pin WFBGA: 9mm x 9mm, 0.65mm ball pitch (see Figure 1-4)

Note:	Please refer to the latest data sheet for most up-to-date PCB LAND pattern information.

The following list summarizes BGA routing guidelines, but it is understood that final layout is process- dependent and your design should reflect your needs:

- Through-hole vias technology is not recommended for pitches less than 0.8mm (unless the ball matrix is depopulated in the center)
- NSMD ball pads for pitches 0.8mm – 0.4mm
- Solder Mask to be 1:1 scale of the land size, when routing 0.5mm pitch ball pads
- µVias – next generation PCB technology for tighter pitches
- Eliminate through-hole vias
- Increase routing density & enhance electrical performance
- Decrease routing layers
- Provide fan-out solutions for multiple layers (stacked Vias)

FIGURE 1-4: LAND PATTERN DIMENSIONS, 144-WFBGA, 0.65MM BALL PITCH



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1'/E1'	-	7.80	-
e'	-	0.65	-

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

ROUTING DIMENSIONS	
SYMBOL	b(nom) = 0.25
Ø PAD	0.250
Ø SM	0.350
L (Trace)	0.125
SPACE (Min)	0.135
SM-Space (Min)	0.088
Ø VIA PAD	0.400
Ø DRILL	0.200

PCB LAND PATTERN AND ROUTING

2.0 MISCELLANEOUS CONSIDERATIONS

This section covers a variety of layout topics:

2.1 Strapping Options

Table 2-1 describes the MEC140x / MEC141x strap option pins.

TABLE 2-1: MEC140X / MEC141X STRAP OPTIONS

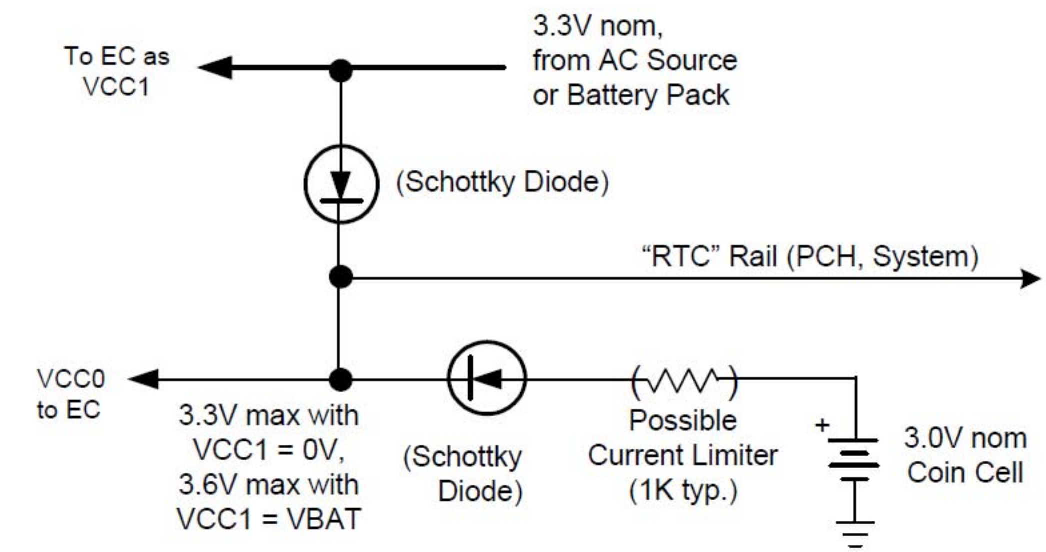
<table>
<tr><th>GPIO</th><th>Strap Name</th><th>Description</th><th>Pull High</th><th>Pull Low</th></tr>
<tr><td rowspan="2">GPIO102 [CR_STRAP]</td><td>Boot source select straps</td><td>This strap option is sampled by the Boot ROM to select firmware loading from Private SPI flash or select by BSS_STRAP.</td><td>Use the BSS_STRAP to determine loading selection.</td><td>Use the Private SPI pins for boot.</td></tr>
<tr><td colspan="4">Note: An external pull-high or pull-low is required for this strapping option.</td></tr>
<tr><td rowspan="2">GPIO123 [BSS_STRAP]</td><td>Shared SPI vs. eSPI Selection</td><td>This strap option is sampled by the Boot ROM to select firmware loading from Shared SPI flash or eSPI flash channel.</td><td>Use the Shared SPI pins for boot.</td><td>Use the eSPI Flash channel for boot.</td></tr>
<tr><td colspan="4">Note: This option is for MEC141x eSPI enabled devices ONLY. Not applicable to MEC140x.</td></tr>
</table>

2.2 Battery Circuit

Please see the Power Sources section of the MEC140x / MEC141x PCS.

For the battery circuity requirement, VCC0 must always be present if VCC1 is present. The following circuit is recommended to fulfill this requirement.

FIGURE 2-1: RECOMMENDED BATTERY CIRCUIT



2.3 LPC Interface

The firmware must configure the GPIO Pin Control Registers for the LPC alternate function, configure the LPC Base Address Register, and activate the LPC block.

2.3.1 VTR_33_18 POWER PIN

The LPC Interface Signals require the VTR_33_18 power pin to be connected to the 3.3V VTR rail. Please also configure the VTR_LPC_ESPI_SEL18 bit 3 at Power Regions Voltage Control Register (0xFC48) accordingly.

2.3.2 HOST RESET SELECT

The platform reset signal that will be used to assert nSIO_RSET is determined by the POWER RESET CONTROL Register (80148h) Bit 1 = 0 - LRESET# pin.

2.3.3 LAD[3:0] /LFRAME#/ LDRQ#/SERIRQ

The AC and DC specifications for these signals are set the same as defined for AD[31:0] in Section 4.2.2 of the "*PCI Local Bus Specification, Rev 2.1*". That section contains the specifications for the 3.3V signaling environment. LAD[3:0] must go high during the TAR phase. The last device driving the LAD[3:0] is responsible to drive the signals high during the first clock of the TAR phase. During the 2nd clock, LAD[3:0] is floated and maintained high by weak pullup resistors (approximately 100 k Ω). These pullups are not included in the MEC140x / MEC141x, but may be included in the chipset.

2.3.4 OTHER SIGNALS

All the other LPC I/F signals are connected to other PCI signals that are already present in the system. The MEC140x / MEC141x use 3.3V signaling for all LPC signals, including the PCI Reset and Clock, therefore the system must drive these signals at 3.3V signaling levels.

2.4 eSPI Interface (MEC141x ONLY)

The firmware must configure the GPIO Pin Control Registers for the eSPI alternate function, configure the eSPI I/O Component Base Address Register, and activate the eSPI block.

2.4.1 VTR_33_18 POWER PIN

The eSPI Interface signals require the VTR_33_18 power pin to be connected to the 1.8V rail. Please also configure the VTR_LPC_ESPI_SEL18 bit 3 at Power Regions Voltage Control Register (0xFC48) accordingly.

2.4.2 HOST RESET SELECT

The platform reset signal that will be used to assert nSIO_RSET is determined by the POWER RESET CONTROL Register (80148h) Bit 1 = 1 - eSPI_PLTRST# pin.

2.4.3 OTHER SIGNALS

All the eSPI I/F signals are connected to other eSPI signals that are already present in the system. The MEC140x / MEC141x use 1.8V signaling for all eSPI signals. Please refer to the Intel Skylake Ultrabook Platform U-Series RVP Customer Reference Board Schematic, Microchip MEC140x / MEC141x Evaluation Board Schematic, and reworks instruction for detailed information.

Few design notes as below:

- LPC_AD0_ESPI_IO0, LPC_AD1_ESPI_IO1, LPC_AD2_ESPI_IO2, LPC_AD3_ESPI_IO3, LPC_FRAME_ESPI_CS#, and LPC_CLK_0_ESPI_CLK signals have 15 ohm series resistor close to each chipset pin and another 15 ohm series resistor close to the MEC141x for eSPI mode.
- GPP_C5/SML0ALERT# (Intel Skylake chipset pin W1) is used as strapping pin to determine either LPC mode (Low) or eSPI mode (High).

2.5 PS/2 Interface

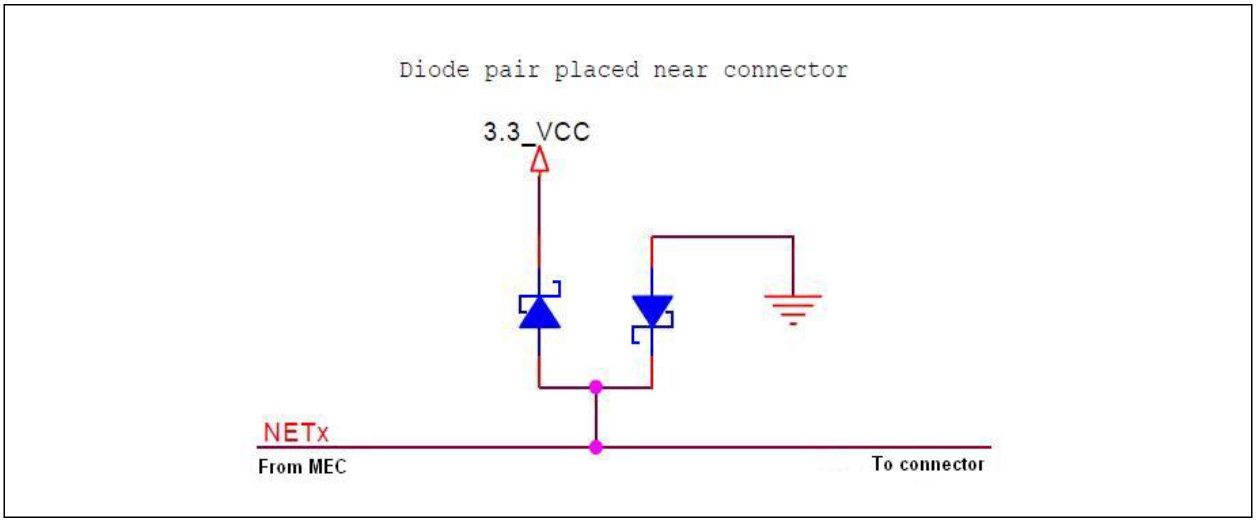
The routing of the PS/2 interface is also not critical, except that it should not be routed next to rapidly switching signals. The Clock and Data pins are Open Drain and require pullup resistors. A small 10 - 100pF (typ) capacitor to ground and 4.7kΩ (typ) pullups are recommended. The power pin of the PS/2 pin should be decoupled with a capacitor that is large enough to adequately filter the supply to PS/2 devices. Unused PS/2 clock and data pins should be pulled up to VCC with a 10kΩ (typ) resistor.

Note: The PS/2 Interface is not 5V tolerant.

2.6 EOS Considerations

For SMBus signals that terminate external to the main system board (for example, Smart Battery) the designer should take care in protecting these signals from EOS (Note 2-1) and ESD (Note 2-2). Please refer to the SMBus 2.0 specification, section 3.1.2.2 for appropriate guidelines. The specification recommends a series protection resistor and an optional ESD transorb on these nets. In addition to the SMBus specification recommendation, past experience shows that using 2 high speed diodes on each SMBus trace (instead of the transorb in the SMBus spec) is an effective way to improve immunity to EOS and ESD events. A Schottky diode pair is a good example. Figure 2-2 shows the suggested circuit implementation for each net that goes to a connector.

FIGURE 2-2: SCHOTTKY DIODE PAIR EXAMPLE



It should also be noted that any other signal that goes to an external connector should also be considered for EOS/ESD susceptibility. For instance, an ID pin (tied to a GPIO) that might seem benign, but is routed near high voltage sources could suffer transient EOS events. A similar protection scheme should be considered for these nets.

Note 2-1 EOS is defined as damage to the part caused by the application of voltages (to any pin) beyond the power supply rails, usually forward biasing internal protection diodes and resulting in high levels of current flow. This typically induces open failures by damaging the metal inside the part. EOS is typically a low voltage, high current situation.

Note 2-2 ESD is the applied reverse bias to the PN junction -- heat due to power dissipation melts the silicon in the part. ESD is typically a high transient voltage spike with low current situation.

2.7 ADC Input Layout Requirement for Regular Sampling

ADC has a large internal resistance.

Every ADC input terminal has a gate switch.

This gate switch is protected by diodes.

It is natural for diodes have leakage current.

At sampling time: (Gate switch closed)

Input voltage is charged and sampled at sample point A.

Sampling time is affected by RC time constant defined by internal resistor and internal capacitor.

In continuous mode, the sampling time is too fast for sample point A to discharge sampled value. In this case, glitch will not be observed.

In one shot mode or in long report mode, the sampling time is long enough for point A to discharge sampled value.

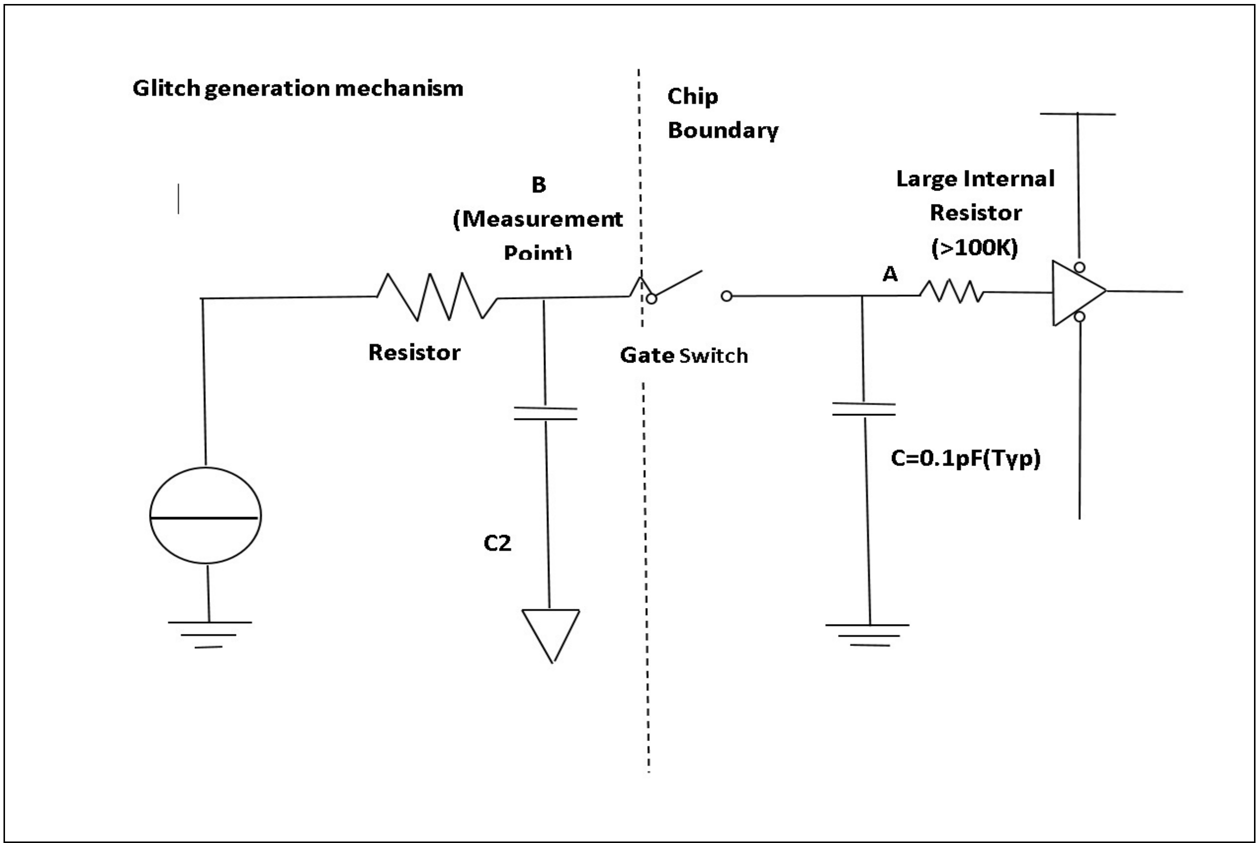
In this case, glitch will be observed on the next sampling point.

If an external capacitor with value between 0.1uF and 0.01uF (point C2) is placed on the input terminal, the charged value at point A will be kept as it is instead of discharging it and then glitch will not be observed.

For high sampling frequencies, it is recommend to set the cut off frequency of the R/C at ½ of the ADC sampling frequency / 10.

Please also refer to the white paper at ww1.microchip.com/downloads/en/AppNotes/00699b.pdf for more information.

FIGURE 2-3: ADC INPUT LOW PASS FILTER



2.8 SPI Flash Interface

The MEC140x / MEC141x SPI flash interface enables the host and embedded controller (EC) access to an external SPI flash device. The MEC140x / MEC141x PCS documentation has more details on signal implementation (see References on page 1). This section describes specific PCB layout design considerations to setup this feature.

Note: The SPI Flash Interface of MEC140x / MEC141x supports 3.3V ONLY. Any lower voltage SPI flashes are not supported and should not be used with the MEC140x / MEC141x.

The standard set of SPI flash signals are designated with “SHD_” for shared connections, for example, SHD_SCLK; for details, see Section 2.8.3, "Shared SPI Flash Interface". MEC140x / MEC141x has an added set of signals for connection to another SPI flash device as private, protected data; these signals are designated with “PVT_,” for example, PVT_SCLK; for details, see Section 2.8.4, "Private SPI Flash Interface". The Private SPI can be used as a crisis recovery interface as it shares pins with the keyboard interface. MEC140x / MEC141x has a third SPI interface as a general SPI interface labeled as “SPI_,” for example, SPI_CLK.

TABLE 2-2: SPI INTERFACE SIGNALS

Generic Pin Signal Name	Pin Signal Function name	MEC140x / MEC141x Pin Number	Pin Function Signal Description
SPICLK	SHD_SCLK	32	Shared SPI Clock
	PVT_SCLK	15	Private SPI Clock
IO0 / MOSI	SHD_IO0 / SHD_MOSI	28	Shared SPI Data I/O 0
	PVT_IO0 / SHD_MOSI	16	Private SPI Data I/O 0
IO1 / MISO	SHD_IO1 / SHD_MISO	29	Shared SPI Data I/O 1
	PVT_IO1 / SHD_MISO	2	Private SPI Data I/O 1
IO2	SHD_IO2	30	Shared SPI Data I/O 2
	PVT_IO2	50	Private SPI Data I/O 2
IO3	SHD_IO3	31	Shared SPI Data I/O 3
	PVT_IO3	46	Private SPI Data I/O 3
SPI_CS#	SHD_CS#	27	Shared SPI Chip Select
	PVT_CS#	14	Private SPI Chip Select

2.8.1 BOOT ROM STRAP OPTION

The Boot ROM will only load code from either the private SPI interface or shared SPI interface or eSPI flash channel.

The Boot ROM will sample the CR_STRAP and BSS_STRAP pins; no hardware is required.

CR_STRAP	BSS_STRAP (MEC141x Only)	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

2.8.2 ESPI FLASH CHANNEL INTERFACE (**MEC141X ONLY**)

The MEC140x / MEC141x Boot ROM firmware selects the eSPI flash channel to load the EC firmware by sampling the CR_STRAP and BSS_STRAP pins during POR.

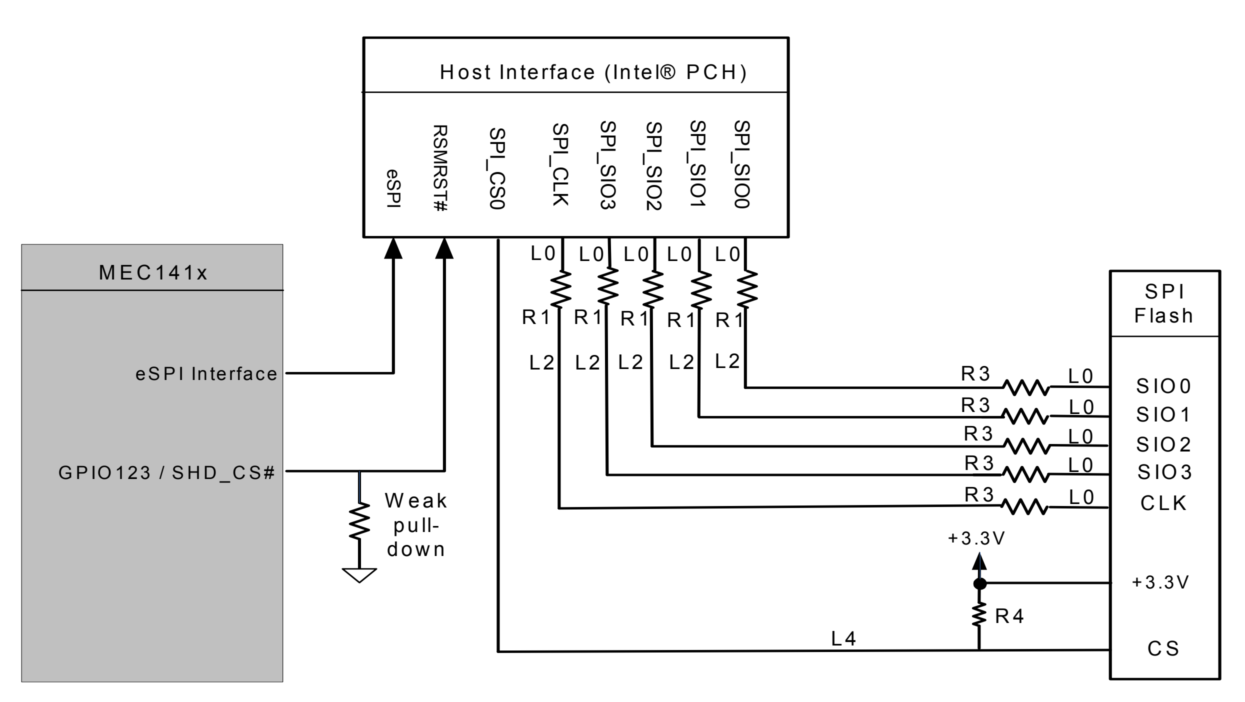
When used with a PC-based core logic, the EC must supply the RSMRST# signal to the core. If the eSPI Flash Channel is used as the source for EC firmware, the **GPIO123/SHD_CS# pin MUST be used as the RSMRST# signal**. A weak-pulldown resistor to ground must be connected to the pin as shown in Figure 2-4. The pull-down both holds RSMRST# low glitch-free during the power-on sequence, as required by the core logic, and informs the Boot ROM in the MEC140x / MEC141x to use the eSPI Flash Channel.

Note: In eSPI flash channel implementation, the SPI flash is connected to Core Logic directly, please refer to its specification for recommended SPI connection guideline, Figure 2-4 is shown as illustration purpose only.

Note: In order for the Core Logic to be controlled by the RSMRST# signal, the PCH Primary Power Rails are required to be powered along with the EC.

Note: If the eSPI Flash Channel is used for booting, the GPIO135/SHD_I02 pin must be used to determine that the primary power rails are stable before RSMRST# can be de-asserted. See the MEC140X/1X eSPI Addendum document for more details.

FIGURE 2-4: MEC140X / MEC141X TOPOLOGY FOR ESPI FLASH CHANNEL



If the EC firmware is sourced from an external SPI Flash device directly to the Shared SPI Flash interface, **the GPIO123/SHD_CS# pin MUST NOT be used as the RSMRST# signal**. Any other GPIO can serve as RSMRST#, if connected to ground with a weak pull-down resistor as shown in Figure 2-5. Once firmware is loaded and executed, it can release RSMRST# by setting the selected GPIO high.

2.8.3 SHARED SPI FLASH INTERFACE

2.8.3.1 Shared SPI Flash Implementation

Figure 2-5 is a topology for implementing a single MEC140x / MEC141x SPI flash for shared SPI flash devices. See Table 2-3 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

Note:	In order for the Core Logic to be controlled by the RSMRST# signal, the PCH Primary Power Rails are required to be powered along with the EC. Otherwise, the isolation circuit will be needed in the Shared SPI implementation.

FIGURE 2-5: MEC140X / MEC141X TOPOLOGY FOR SHARED SPI FLASH DEVICE

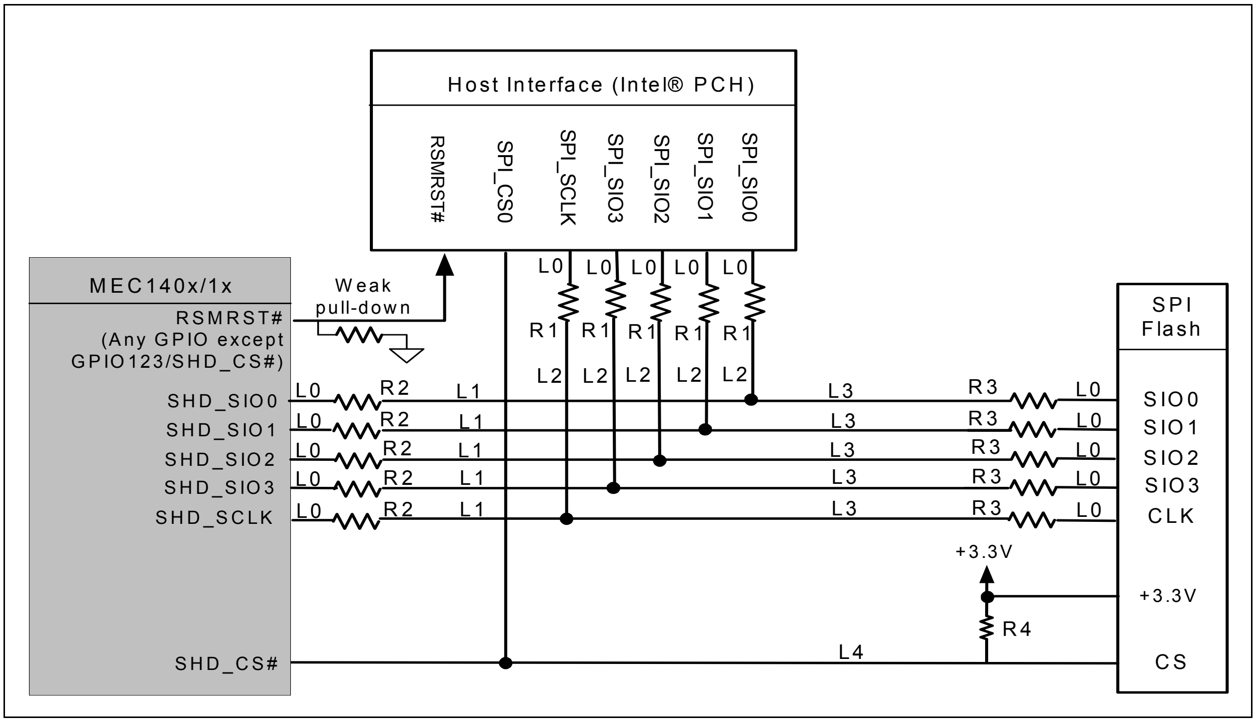


TABLE 2-3: MEC140X / MEC141X SHARED SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between MEC140x / MEC141x, Host/PCH, or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	PCB trace from the MEC140x / MEC141x termination resistor to the PCB trace connection from the SPI flash and Host/PCH.	L1 = L2 = L3 These trace connections can equal 1-inch up to 5-inches. See Note 2-3
L2	PCB trace from the Host/PCH termination resistor to the PCB trace connection from the SPI flash and MEC140x / MEC141x.	
L3	PCB trace from the SPI flash termination resistor to the PCB trace connection from the MEC140x / MEC141x or Host/PCH.	
L4	PCB trace from Host/PCH or MEC140x / MEC141x to SPI flash for chip select.	L4 = L1 + L3 + (2 x L0) or L4 = L2 + L3 + (2 x L0) +/- 0.100 inches.
R1	These resistors are between the PCB trace and the Host/PCH.	25 ohm, see Note 2-1, Note 2-2
R2	These resistors are between the PCB trace and the MEC140x / MEC141x.	15 ohm, see Note 2-1, Note 2-2
R3	These resistors are between the PCB trace and the SPI flash.	15 ohm, see Note 2-1, Note 2-2
R4	Pull-high resistor to +3.3V for SPI CS connections; between the MEC140x / MEC141x or Host/PCH and the SPI flash device. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm, see Note 2-4

Note 2-1 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC140x / MEC141x (-0.3V min. to V_{CC1}+0.3V max).

Note 2-2 Resistor recommendations are based on testing with 180nm PCH and SPI flash drivers. Any change to a driver would require a change to the related termination resistors, see also Note 2-1.

Note 2-3 L1, L2, L3 must be equal to each other. For example, if L1 = 2-inches, then L3 must be 2-inches.

Note 2-4 Per current Intel PCH device specification regarding the SPI0_CS# pin when RSMRST# is low, the Skylake PCH LP is tri-stated with no pull-up or pull-down, so R4 can be 4.7K to 100K range. The Skylake PCH H is tri-stated with wake internal pull-down, so R4 has to be 4.7K to 8K range.

2.8.4 PRIVATE SPI FLASH INTERFACE

Note:	Either Shared SPI or Private SPI interface can support a dedicated SPI chip. The Private SPI is targeted for use as a crisis recovery option since it is muxed with keyscan pins.

2.8.4.1 Private SPI Flash Implementation

Figure 2-6 is a topology for implementing the MEC140x / MEC141x SPI flash for a single private SPI flash device. See Table 2-4 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-6: MEC140X / MEC141X TOPOLOGY FOR PRIVATE SPI FLASH DEVICE

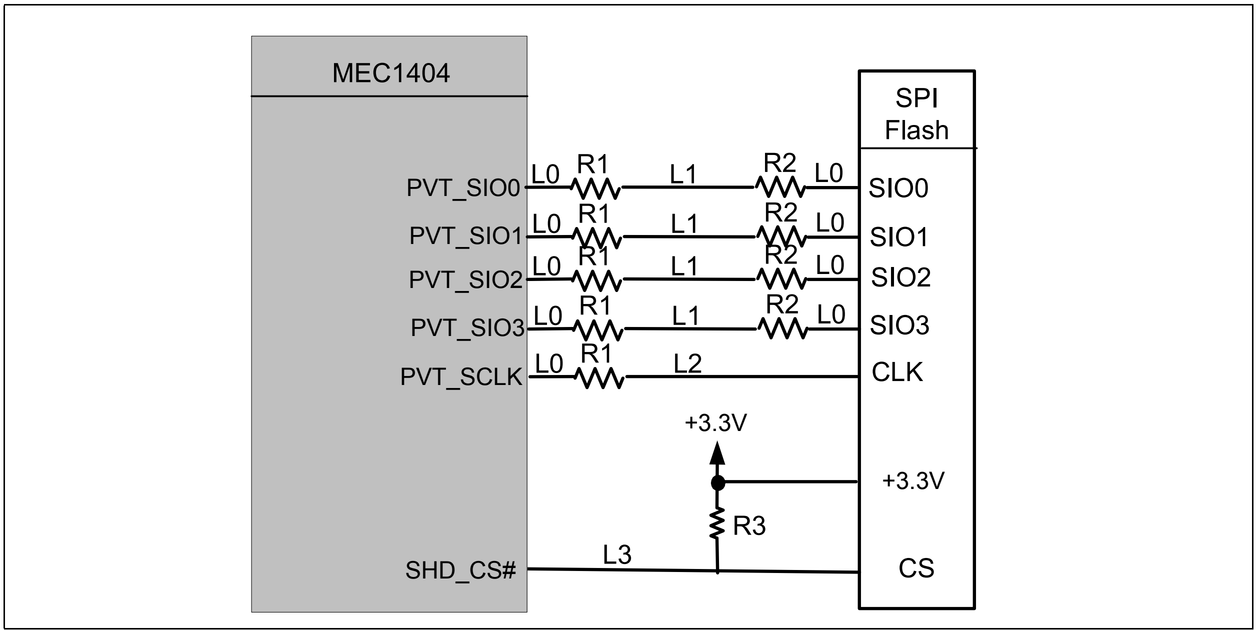


TABLE 2-4: MEC140X / MEC141X PRIVATE SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between MEC140x / MEC141x or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	The PCB trace between terminating resistors on the IO lines.	1-inch to 10-inch
L2	The PCB trace from MEC140x / MEC141x or R1 resistor to SPI flash.	1-inch to 10-inch
L3	PCB trace from MEC140x / MEC141x to SPI flash for chip select.	L3 = L0 + L1
R1	These resistors are between the trace and the MEC140x / MEC141x.	25 ohm, see also Note 2-5
R2	This resistor is on the IO lines between the SPI flash and trace.	45 ohm, see Note 2-5.
R3	This is a Pull-High resistor (to +3.3V) for SPI CS connections. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-5 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC140x / MEC141x (-0.3V min. to V_{CC1} +0.3V max).

2.8.5 SPI FLASH IMPLEMENTATION RECOMMENDATIONS

The following recommendations are for both Shared and Private SPI Flash Implementations.

- The MEC140x / MEC141x SPI memory interface has serial flash device compatibility requirements that are defined in the MEC140x / MEC141x PCS. Please make sure the selected SPI flash meets these requirements.
- SPI_CLK must be 20mils spacing from any other high frequency (>1GHz) signal.
- The SPI flash parts should support operating at 8.5MHz for the ROM code loader, and up to 33MHz clock speed in RAM code loading.
- The designer should follow the SPI interface host design guidelines.
- IBIS models are available to aid in simulating the SPI system topology.
- The chip select CS# signals should have weak pullup resistors to the same power rail as the SPI flash. The pullup resistor value should meet the rise time requirements of the SPI flash.
- EC firmware must configure the MEC140x / MEC141x SPI memory interface to disable mode, which will tri-state the SPI memory interface from MEC140x / MEC141x to the SPI flash, before releasing the RSMRST# signal.
- This configuration requires that the PCH tri-states its SPI flash pins when RSMRST# is asserted.
- The characteristic impedance of the PCB trace should be 50 ohms +/-15% at 50MHz operating frequency.
- Within the SPI flash device, Schmitt trigger inputs are assumed on both the clock line and IO data lines.
- Within the Intel PCH, a Schmitt trigger input is assumed on the IO data lines.
- The output drivers for the SPI flash chip select pins should be programmed as open-drain using the GPIO Pin Control registers.
- The SPI Data IO traces should be length-matched to the CLK lines within 0.100-inch.
- Signal Integrity should be checked for each SPI part on your BOM.

2.8.6 SPI FLASH EXTERNAL PROGRAMMER

The SPI Flash on either Shared or Private SPI Flash interface must be programmed externally using a suitable programmer, such as Dediprog's SF100 (http://www.dediprog.com/pd/spi-flash-solution/sf100).

Provisions for a programming header on each SPI flash are recommended if the SPI is not socketed.

2.9 1MHz Pullup Resistor Requirement

Please refer to the I^2C-bus specification and user manual as indicated in the section References on page 1 for more information.

2.10 5V Tolerant Pins

There are no 5V tolerant pins on the MEC140x / MEC141x.

2.11 1.8V Capability

Please refer to the MEC140x / MEC141x Data Sheet section 2.6 for more information.

Note: The LPC Interface Signals require the VTR_33_18 power pin to be connected to the 3.3V VTR rail. The eSPI Interface signals require the VTR_33_18 power pin to be connected to the 1.8V rail. The GPIO signals on these pins may operate at either 1.8V or 3.3V. Please also configure the VTR_LPC_ESPI_SEL18 bit 3 at Power Regions Voltage Control Register (0xFC48) accordingly.

Note: The SMB00 to SMB04 Ports have the option to be configured for either 3.3V or 1.8V signaling. This selection is determined by the GPIO alternate function mux.

3.0 2-WIRE DEBUG INTERFACE (ICSP)

Please refer to the Microchip ICD User Manual as indicated in the section References on page 1 for more information.

- The Figure 3-1 shows the standard recommended target circuitry.
- The Figure 3-2 shows the circuits that will prevent the debugger from functioning.

TABLE 3-1: ICSP INTERFACE SIGNALS

Pin Signal Function name	MEC140x / MEC141x Pin Number	Pin Function Signal Description
ICSP_MCLR	87	ICSP Master Clear **Note:** This pin requires external 10K pulled high to avoid floating.
ICSP_CLOCK	101	ICSP Clock (shown as PGC in Figure 3-1)
ICSP_DATA	102	ICSP Data (shown as PGD in Figure 3-1)

FIGURE 3-1: STANDARD CONNECTION TARGET CIRCUITRY

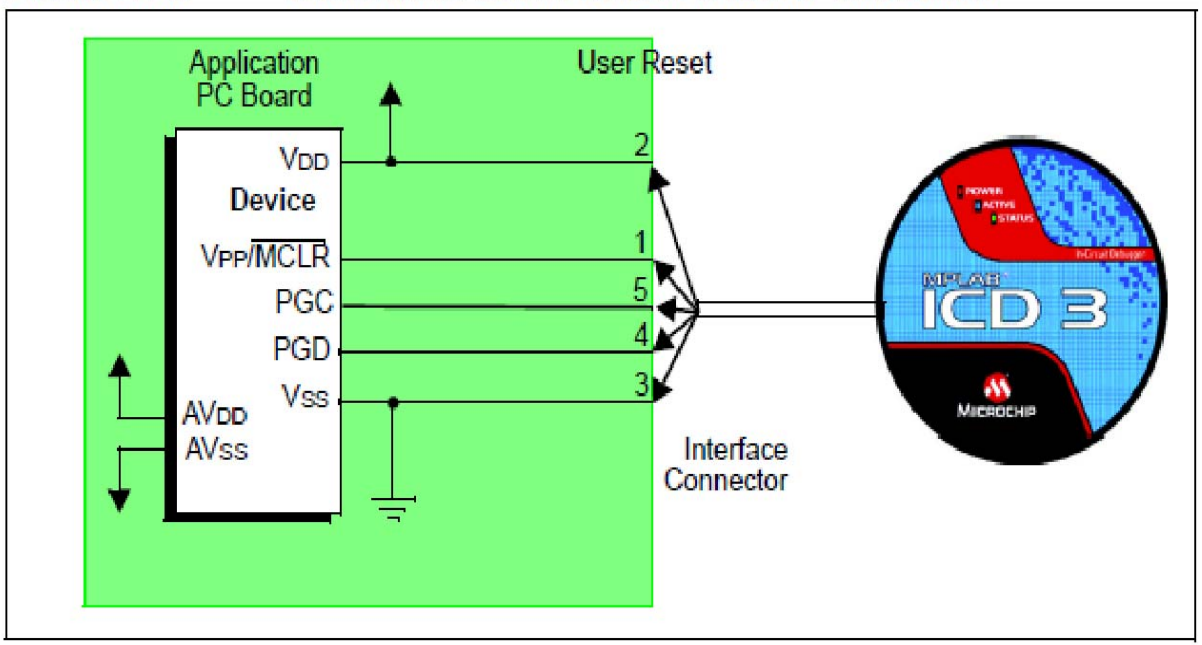
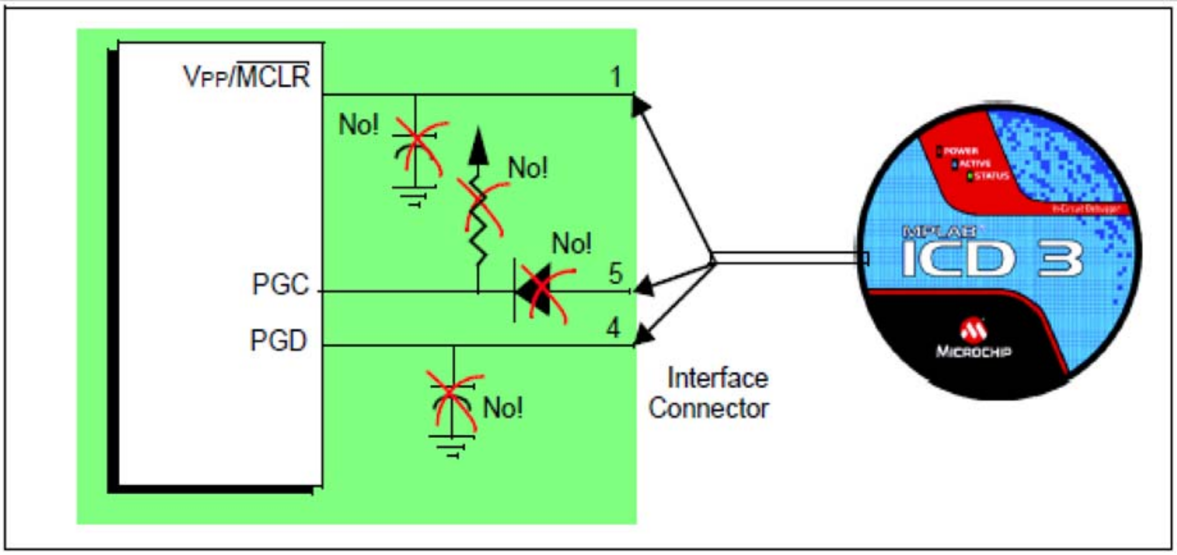


FIGURE 3-2: IMPROPER CIRCUIT COMPONENTS



Specifically, these guidelines must be followed:

- Do not use pull-ups on PGC/PGD – they will disrupt the voltage levels, since these lines have 4.7 kΩ pull-down resistors in the debugger.
- Do not use capacitors on PGC/PGD – they will prevent fast transitions on data and clock lines during programming and debug communications.
- Do not use capacitors on $\overline{\text{MCLR}}$ – they will prevent fast transitions of VPP. A simple pull-up resistor is generally sufficient.
- Do not use diodes on PGC/PGD – they will prevent bidirectional communication between the debugger and the target device.

4.0 PROGRAMMABLE COMPARATORS

MEC140x / MEC141x has two programmable comparators.

Figure 4-1 shows the comparators signals information.

Figure 4-1 show the comparators alternate circuitry in single supply operation.

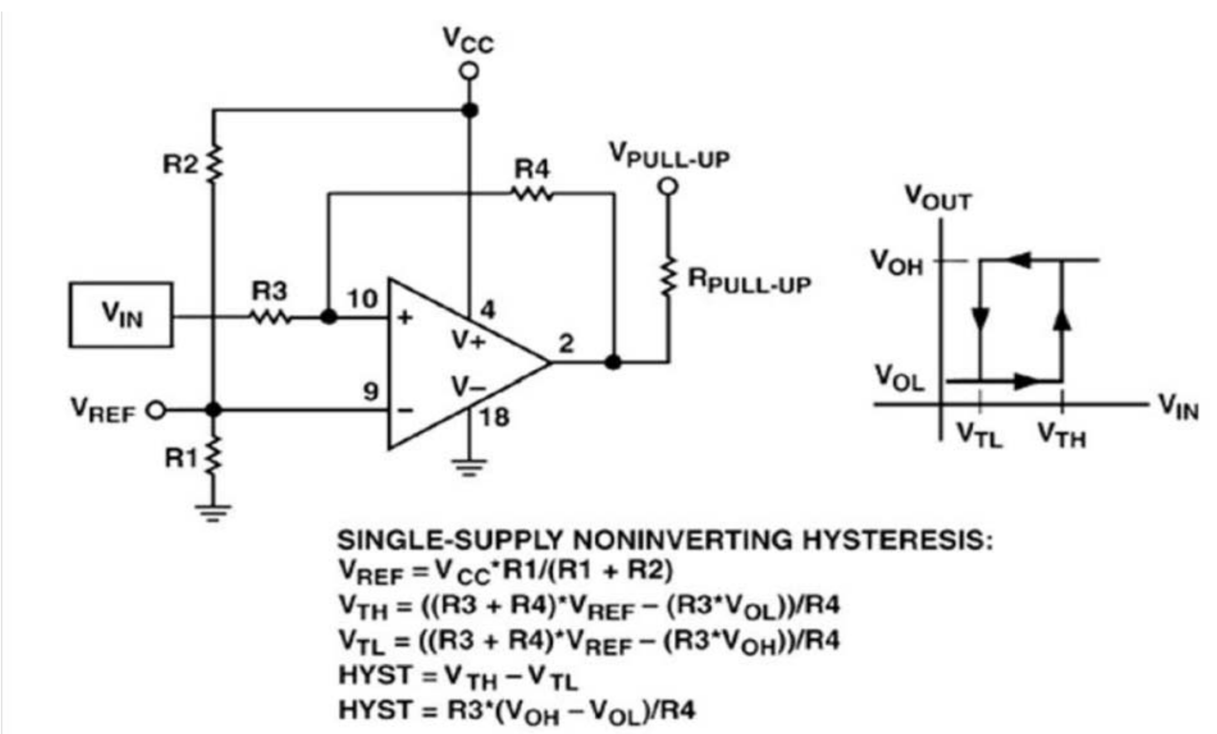
See the additional information that can be used as reference.

- Hysteresis is implemented externally by implementing feedback resistor circuit on VOUT to VIN pin.
- Input voltage range (VIN) from 0 to 3.63V.
- Input threshold range may come from VREF pin or from internal DAC that is configurable from 0 to 3.63V.

TABLE 4-1: COMPARATORS SIGNALS

Pin Signal Function name	MEC140x / MEC141x Pin Number	Pin Function Signal Description
GPIO165/CMP_VREF0	25	Comparator 0 Voltage Reference
GPIO020/CMP_VIN0	20	Comparator 0 Voltage Input
GPIO124/CMP_VOUT0	85	Comparator 0 Voltage Output
GPIO166/CMP_VREF1	26	Comparator 1 Voltage Reference
GPIO021/CMP_VIN1	21	Comparator 1 Voltage Input
GPIO120/CMP_VOUT1	83	Comparator 1 Voltage Output

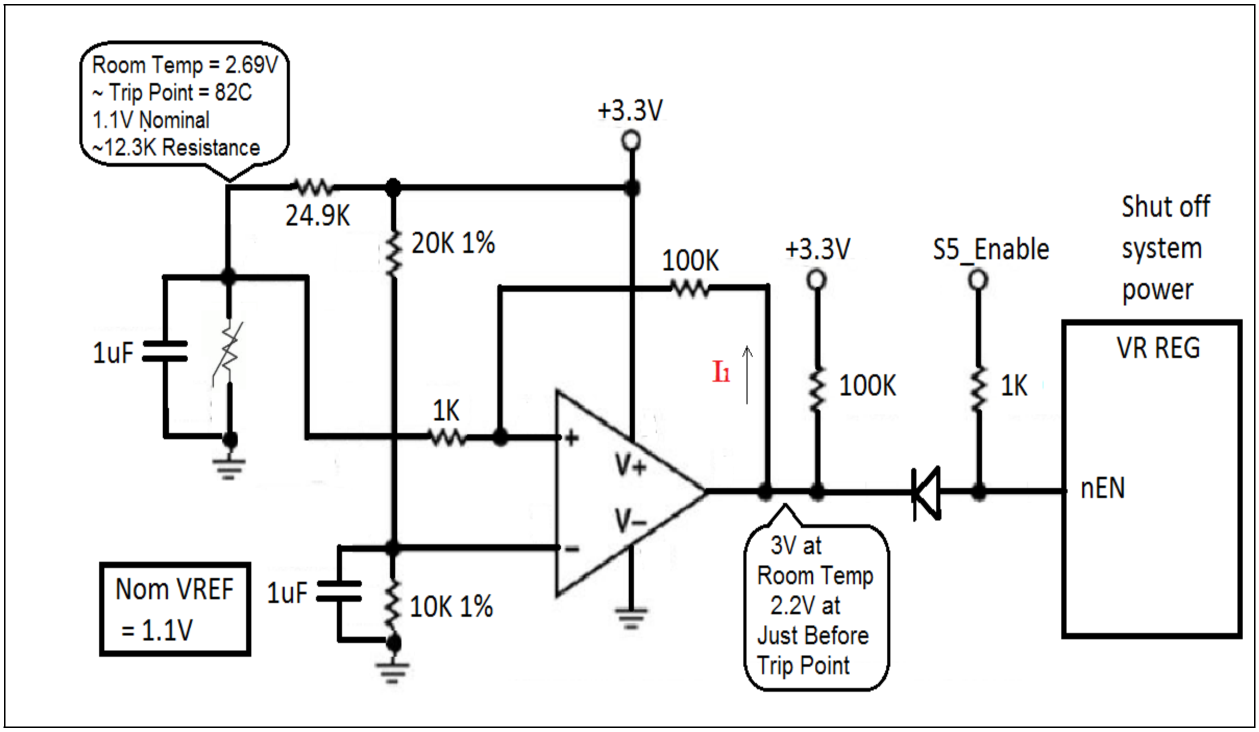
FIGURE 4-1: COMPARATORS IN SINGLE-SUPPLY OPERATION



4.1 Thermistor Application

This section shows the calculation of the nominal hysteresis for the circuitry shown in the Figure 4-2, "Thermistor Application example".

FIGURE 4-2: THERMISTOR APPLICATION EXAMPLE



4.1.1 COMPARATOR VOLTAGE OUTPUT CALCULATION

Use Kirchhoff's Voltage Law with assumption $I_2 = 0$, ideal condition with some small leakage in uAmps region.

EQUATION 1: AT ROOM TEMP

$- 3.3V + I_1 (100K) + I_1 (100K) + I_1 (1K) + 2.69V = 0$

$I_1 (201K) = 0.66V$

$I_1 = 3.3uAmps$

100K x 3.3uAmps = 0.3V

3.3V - 0.3V = 3V at Room Temperature

EQUATION 2: JUST BEFORE TRIP POINT

$- 3.3V + I_1 (100K) + I_1 (100K) + I_1 (1K) + 1.1V = 0$

$I_1 (201K) = 2.2V$

$I_1 = 11uAmps$

100K x 11uAmps = 1.1V

3.3V - 1.1V = 2.2V at Just Before Trip Point

4.1.2 HYSTERESIS CALCULATION

EQUATION 3: JUST BEFORE TRIP POINT

$- 2.2V + I_1(100K) + I_1(1K) + 1.1V = 0$

$I_1 (101K) = 1.1V$

$I_1 = 11uAmps$

$V_{IN} = 11uAmps (1K) +1.1V = 1.111V$

EQUATION 4: AFTER TRIP POINT

$1.1V = 100K / 101K (V_{IN})$

$V_{IN} = 1.089$

As a result, the hysteresis is +/- 11mV, total 22mV between 1.111V to 1.089V.

4.1.3 CONCLUSION

- Based on the 100K and 1K external feedback resistor values chosen, the nominal is +/- 11m and the total of 22mV hysteresis.
- The output of the comparator is ~3V at room temperature.
- The output of the open drain comparator at just before trip point is 2.2V, which is still high enough based on fact of the circuitry.
- Trip point at ~ 82C, based on a typical 100K NTC Thermistor resistance numbers from the thermistor data sheet.

5.0 HOW TO SETUP ADC VOLTAGE STATES TO DISTINGUISH PC MODEL AND PCB TYPES

This section provides general guidelines regarding how to use the ADC input to distinguish the PC models and PCB types in the design as follows:

1. Choose resistor values by taking into account the effects of the ADC input impedance (refer to MEC140x / MEC141x data sheet for more information).
2. Make sure the tolerance of the large resistors are taken into account.
3. Final calculated voltages, taking into account the ADC input impedance and Resistor tolerance, should give the designer a range of voltages for each resistor set, then make sure there is enough voltage separation to distinguish (accounting for anticipated system noise and accuracy of ADC input resolution), recommend a minimum of 250mV between ADC steps for a robust design.
4. Adjust resistor (such as lower value of resistors used, or use a better tolerance if needed) if step 3 is not satisfactory.

5.1 Reference Example

This section shows the calculation and suggestion based on the above guideline.

5.1.1 IDEALIZED CASE

	Pull Down	Pull Up	Ideal Voltage Divider	Gap
1	100K	10K	3V	0.199V
2	100K	17.8K	2.801V	0.203V
3	100K	27K	2.598V	0.197V
4	100K	37.4K	2.402V	0.2V
5	100K	49.9K	2.201V	0.2V
6	100K	64.9K	2.001V	0.193V
7	100K	82.5K	1.808V	0.214V
8	100K	107K	1.594V	0.295V
9	100K	154K	1.299V	0.199V
10	100K	200K	1.100V	

5.1.2 IDEALIZED CASE WITH 3 MOHM INPUT IMPEDANCE

	Pull Down	Pull Up	Ideal Voltage Divider	Gap
1	96.774K	10K	2.991V	0.204V
2	96.774K	17.8K	2.787V	0.207V
3	96.774K	27K	2.58V	0.2V
4	96.774K	37.4K	2.38V	0.203V
5	96.774K	49.9K	2.177V	0.202V
6	96.774K	64.9K	1.975V	0.194V
7	96.774K	82.5K	1.781V	0.214V
8	96.774K	107K	1.567V	0.294V
9	96.774K	154K	1.273V	0.197V
10	96.774K	200K	1.076V	

5.1.3 WITH 1% RESISTORS TOLERANCE - WORST CASE ANALYSIS

	Actual Pull Down with 3 Mohm Input
99%	95.83736689K
100%	96.77419355K
101%	97.71041599K

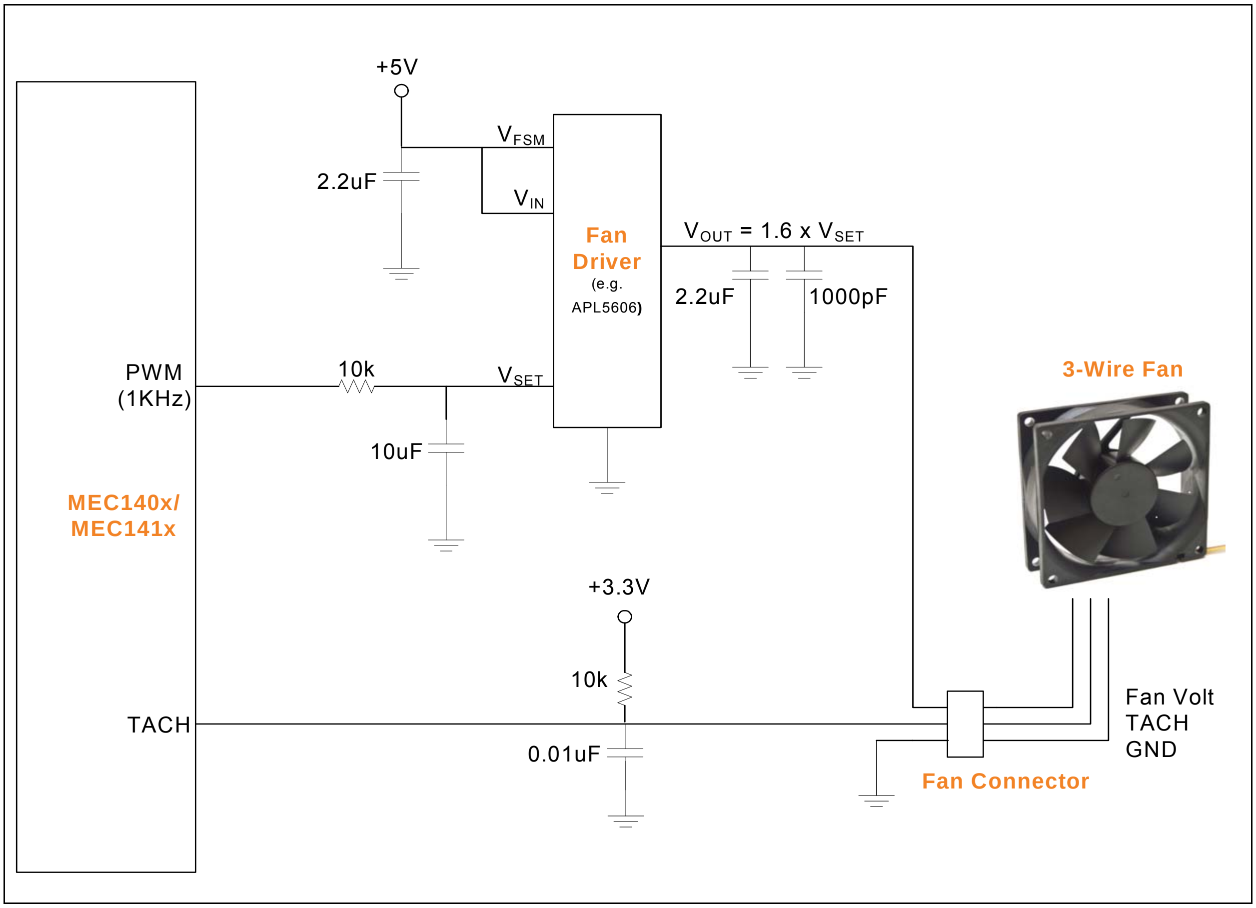
Low Side			High Side			
101% Pull Down w/ 3 Mohm	Low side Pull Up (99%)	High Side Voltage	99% Pull Down w/ 3 Mohm	High Side Pull Up (101%)	Low Side Voltage	GAP
97.71K	9.9K	2.996V	95.837K	10.1K	2.985V	0.19V
97.71K	17.622K	2.796V	95.837K	17.978K	2.779V	0.188V
97.71K	26.73K	2.591V	95.837K	27.27K	2.569V	0.176V
97.71K	37.026K	2.393V	95.837K	37.774K	2.367V	0.175V
97.71K	49.401K	2.192V	95.837K	50.399K	2.163V	0.172V
97.71K	64.251K	1.991V	95.837K	65.549K	1.96V	0.162V
97.71K	81.675K	1.797V	95.837K	83.325K	1.765V	0.182V
97.71K	105.93K	1.583V	95.837K	108.07K	1.551V	0.262V
97.71K	152.46K	1.289V	95.837K	155.54K	1.258V	0.168V
97.71K	198K	1.09V	95.837K	202K	1.062V	

6.0 PWM CONTROLLED 3-WIRE FAN

Pulse Width Modulation (PWM) modules, which produce basically digital waveforms, can be used in many applications as a more efficient and lower power alternative to the traditional 8 bit Digital-to-Analog (D/A) converters using only two inexpensive filter components. A wide variety of microcontroller applications that exist today are better served by utilizing a PWM generated analog output as opposed to an 8 bit D/A converter. One application where using a high resolution PWM has value vs. a traditional 8 Bit DAC is in driving the 3-wire voltage controlled fan in a PC.

The typical schematic of a 3 wire fan drive is shown in Figure 6-1 by PWM.

FIGURE 6-1: 3-WIRE FAN DRIVE BY PWM WITH R/C FILTER



Note:	The DAC should be remained disabled to save ~1mA power.

Please refer to the “*AN2137 - PWM Controlled Fan fro MEC140x/MEC141x*” White Paper for more information.

7.0 MEC140X / MEC141X SHARED SPI FLASH ISOLATION REQUIREMENT

The MEC140x / MEC141x uses the GPIO102/KSO09[CR_STRAP].pin as a strap to determine the boot source (eSPI Flash channel or shared SPI).

There is a new requirement to put isolation on the board if the Shared SPI flash is used so that the SPI_CS# is detected high while RSMRST# is low.

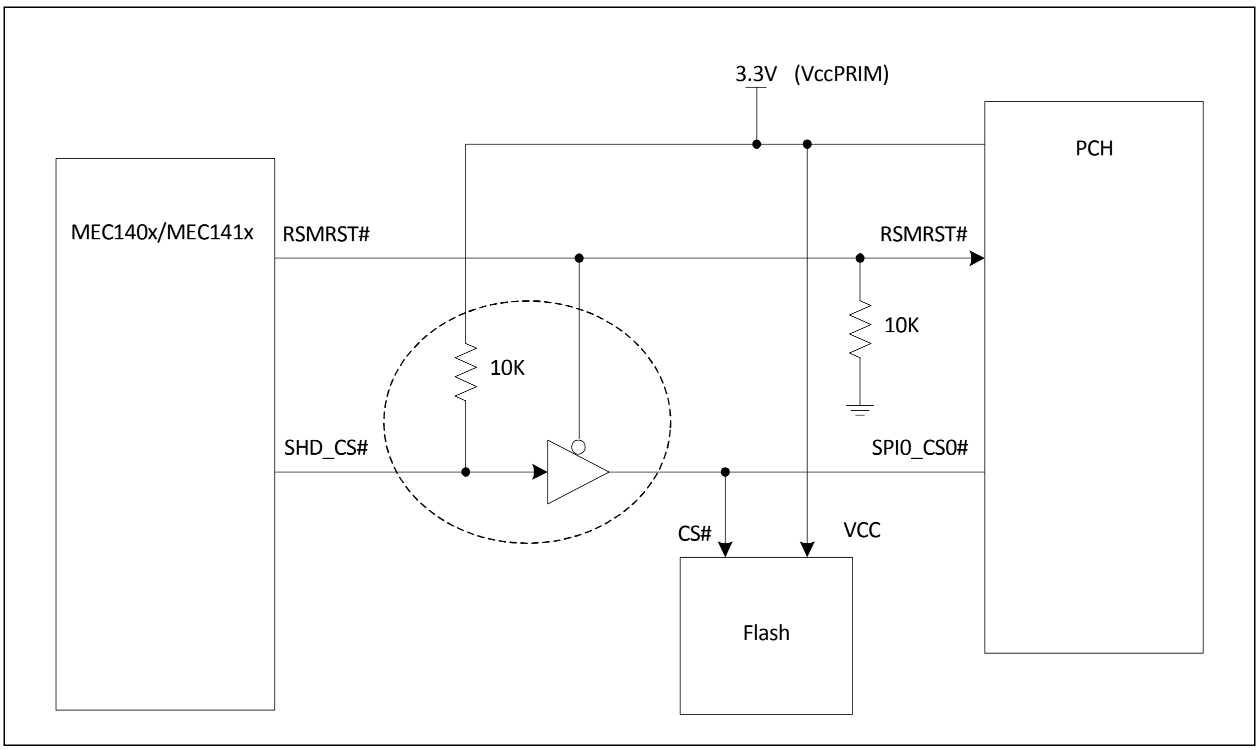
This requirement is due to the following information in the current Intel PCH device specification regarding the SPI0_CS0# pin:

SPI0_CS0# is pulled low instead of high (internally in the PCH)

The “pull” strength is about 1K ohms.

One example of a recommended isolation circuit requires an external tri-state buffer, so that the pull-up for the strap can be of reasonable strength. One possible buffer is the 74LVC1G125 which has a small propagation delay that will not impact the timing of the existing Boot ROM code.

The buffer and pull-up on the SHD_CS# pin is shown in the figure below.



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001859E (03-15-18)	Section 7.0, "MEC140x / MEC141x Shared SPI Flash Isolation Requirement," on page 26	Added section.
	Section 2.7, "ADC Input Lay-out Requirement for Regular Sampling"	Section modified, Figure 2-3, "ADC Input Low Pass Filter" updated.
DS00001859D (09-07-17)	Table 3-1, "ICSP Interface Signals," on page 18	The following note added: "This pin requires external 10K pulled high to avoid floating."
DS00001859C (07-21-16)	References Section 2.1 Section 2.8 Section 6.0 Section 2.8.2	Updated reference information Added Strapping Option section Updated SPI Flash section w/ eSPI info & notes Added PMW controlled 3-wire Fan Added note mentioning GPIO135/SHD_I02 pin
DS00001859B (06-26-15)	All Section 1.1 Section 2.2 Section 2.3 Section 2.10	Added MEC141x family devices Added 144-pin WFBGA package info Updated LPC Section Added eSPI Interface Section Added 1.8V Capability Section
DS00001859A (11-26-14)	Document Release	

ISBN: 9781522427964

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

10/25/17