MIC2202

High Efficiency 2 MHz Synchronous Buck Converter 1 µF Stable PWM Regulator

Features

- Input Voltage Range: 2.3V to 5.5V
- Output Down to 0.5V/600 mA
- 2 MHz PWM Operation
- Stable with 1 µF Ceramic Output Capacitor
- Ultra-Fast Transient Response (up to 500 kHz GBW)
- Internal Compensation
- All Ceramic Capacitors
- >95% Efficiency
- Fully Integrated MOSFET Switches
- Easily Synchronized to External Clock
- SYNCLOCK Feature to Daisy Chain Multiple MIC2202s
- 1% Line and Load Regulation
- Logic Controlled Micropower Shutdown
- Thermal Shutdown and Current Limit Protection
- 10-Lead MSOP and 10-Lead 3 mm x 3 mm VDFN Package Options
- –40°C to +125°C Junction Temperature Range

Applications

- Cellular Phones
- PDAs
- 802.11 WLAN Power Supplies
- FPGA/ASIC Power Supplies
- Dynamically Adjustable Power Supply for CDMA/W-CDMA RF Power Amps
- DSL Modems
- Tape Drives

General Description

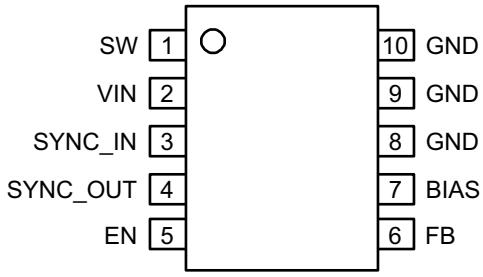
The MIC2202 is a high efficiency 2 MHz PWM synchronous buck regulator. The fast 2 MHz operation along with a proprietary compensation scheme allows the smallest possible external components. The MIC2202 can operate with a 1 µF ceramic output capacitor and a small, low DC-resistance, 2.2 µH inductor, reducing system size, and cost while allowing a high level of efficiency.

The MIC2202 operates from a 2.3V to 5.5V input and features internal power MOSFETs that can supply over 600 mA of output current with output voltages down to 0.5V. The MIC2202 uses a constant 2 MHz Pulse Width Modulation (PWM) control scheme that reduces noise in sensitive RF, audio, and communications applications. Additionally, the MIC2202 can be synchronized to an external clock or multiple MIC2202s can easily be daisy-chained with the SYNCLOCK feature.

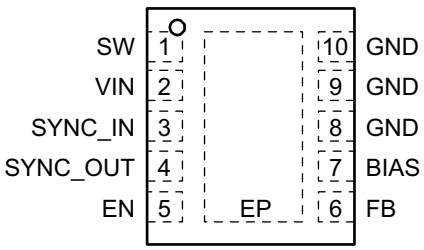
The MIC2202 has a high bandwidth loop (up to 500 kHz) that allows ultra-fast transient response times. This is very useful when powering applications that require fast dynamic response such as CPU cores and RF circuitry in high performance cellular phones and PDAs. The MIC2202 is available in 10-lead MSOP and 10-lead 3 mm x 3 mm VDFN package options with an operating junction temperature range from –40°C to +125°C.

Package Types

MIC2202
10-Lead MSOP (MM)
(Top View)

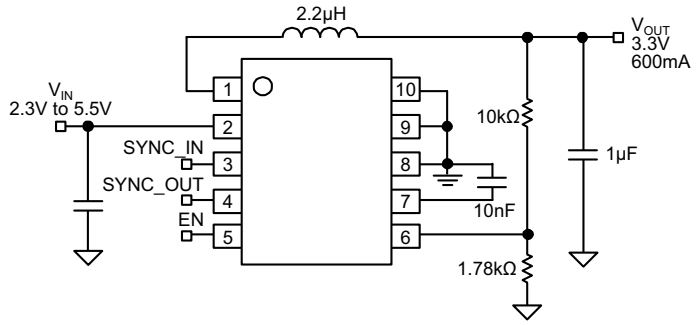


MIC2202
10-Lead VDFN (ML)
(Top View)

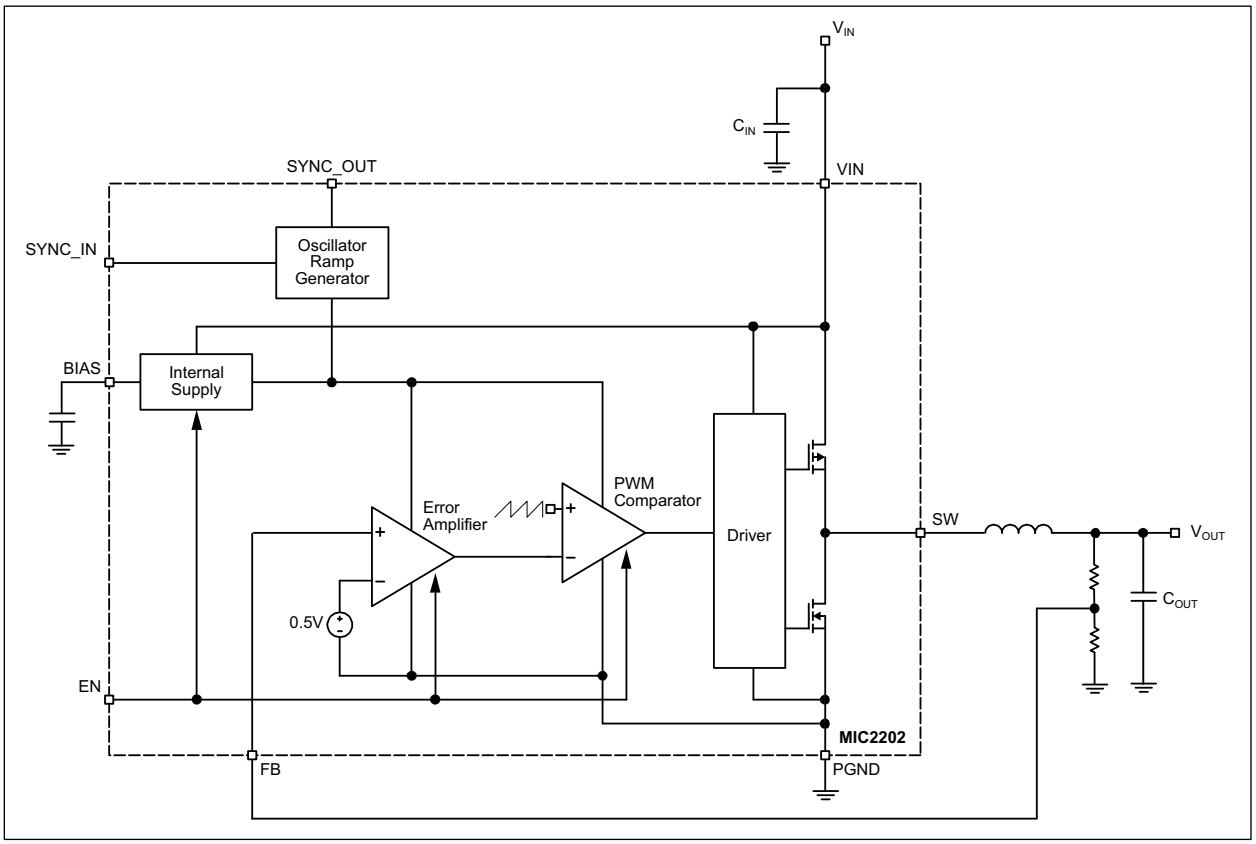


Typical Application Circuit

Adjustable Output Synchronous Buck Regulator



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) ..... –0.3V to +6V
Output Switch Voltage (V_{SW}) ..... –0.3V to +6V
Logic Input Voltage (V_{EN}, V_{SYNC_IN}) ..... –0.3V to V_{IN}
Power Dissipation ..... Note 1
ESD Rating (Note 2) ..... 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN}) ..... +2.3V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The absolute maximum power dissipation is limited by the maximum junction temperature where $P_{D(MAX)} = (T_{J(MAX)} - T_A) \div \theta_{JA}$.

2: Device is ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

T_A = +25°C with V_{IN} = 3.5V unless otherwise noted. **Bold** values valid for –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	V_{IN}	**2.3**	—	**5.5**	V	—
Quiescent Current	I_Q	—	350	450	µA	EN = V_{IN}; V_{FB} = 0.55V (not switching)
		—	0.01	1	µA	EN = 0V
Adjustable Feedback Voltage	V_{FB}	**0.4875**	0.5	**0.5125**	V	—
Output Voltage Line Regulation		—	0.05	0.5	%	V_{OUT} < 2V; V_{IN} = 2.3V to 5.5V, I_{LOAD} = 100 mA
Output Voltage Load Regulation		—	0.1	0.5	%	0 mA < I_{LOAD} < 500 mA
Bias Regulator Output Voltage		2.2	2.32	2.6	V	—
Maximum Duty Cycle	DC_{MAX}	100	—	—	%	V_{FB} = 0.7V
Current Limit	I_{LIM}	**1**	1.8	2.5	A	V_{FB} = 0.7V
Switch ON-Resistance	$R_{DS(ON)}$	—	0.65	0.9	Ω	V_{IN} = 3.5V, I_{SW} = 300 mA; V_{FB} = 0.35V
		—	0.55	0.75	Ω	V_{IN} = 3.5V, I_{SW} = 300 mA; V_{FB} = 0.55V
Enable Input Current	I_{EN}	—	0.01	**1**	µA	—
Sync Frequency Range		**1.6**	—	**2.5**	MHz	—
SYNC_IN Threshold		**0.7**	1	**1.7**	V	—
Sync Minimum Pulse Width		—	10	—	ns	—
SYNC_IN Input Current		—	—	1	µA	—
Oscillator Frequency	f_{OSC}	1.8	2	2.2	MHz	—

ELECTRICAL CHARACTERISTICS (CONTINUED)

T_A = +25°C with V_{IN} = 3.5V unless otherwise noted. **Bold** values valid for –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Threshold		**0.5**	0.9	**1.3**	V	—
Enable Hysteresis		—	20	—	mV	—
Overtemperature Shutdown	T_{SHDN}	—	160	—	°C	—
Overtemperature Shutdown Hysteresis	T_{SD_HYS}	—	20	—	°C	—

Note 1: Specifications for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, MSOP 10-Ld	θ_{JA}	—	115	—	°C/W	—
Thermal Resistance, VDFN 10-Ld	θ_{JA}	—	60	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

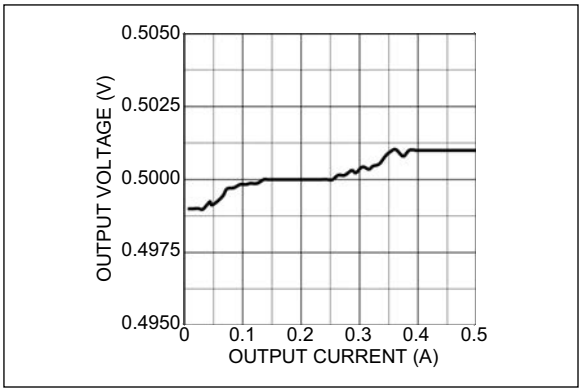


FIGURE 2-1: *Output Voltage vs. Output Current.*

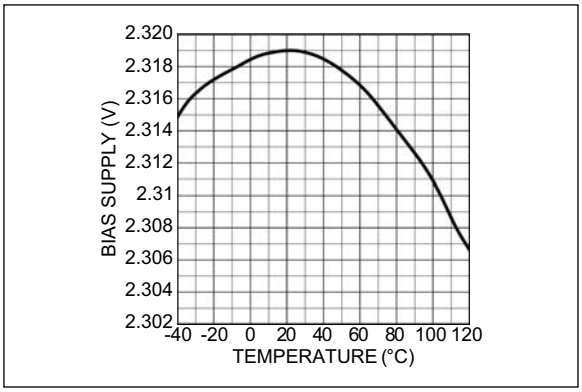


FIGURE 2-4: *Bias Supply vs. Temperature.*

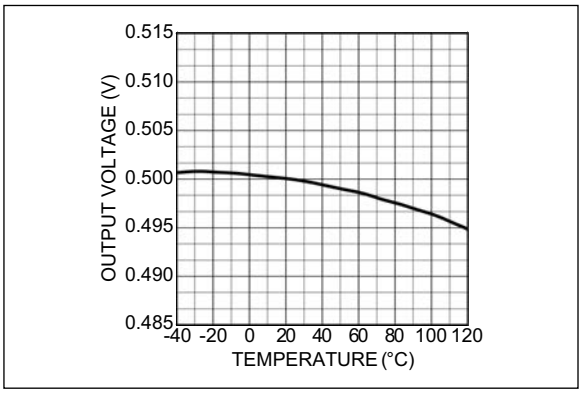


FIGURE 2-2: *Output Voltage vs. Temperature.*

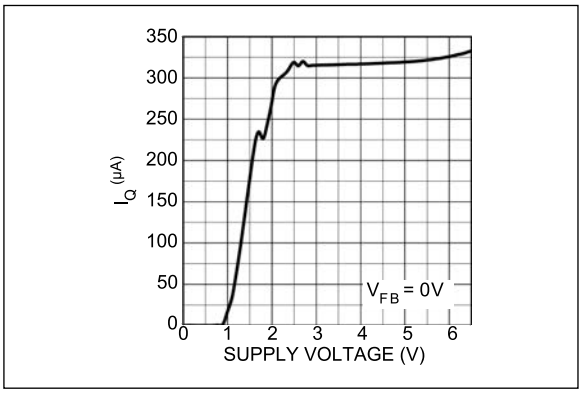


FIGURE 2-5: *Quiescent Current vs. Supply Voltage.*

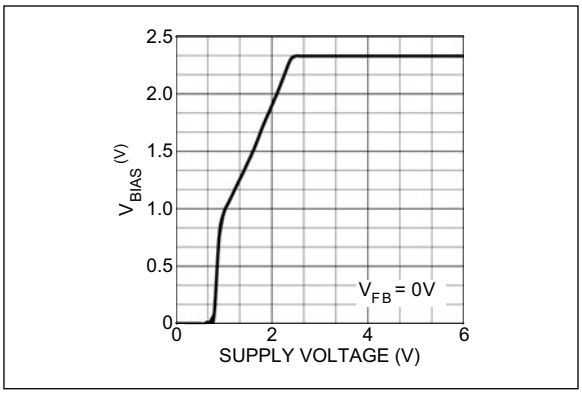


FIGURE 2-3: *V_{BIAS} vs. Supply Voltage.*

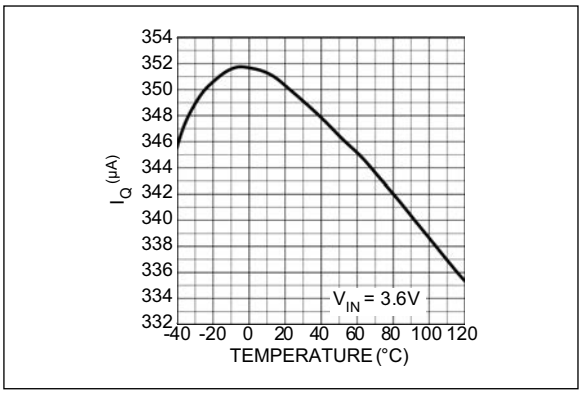


FIGURE 2-6: *Quiescent Current vs. Temperature.*

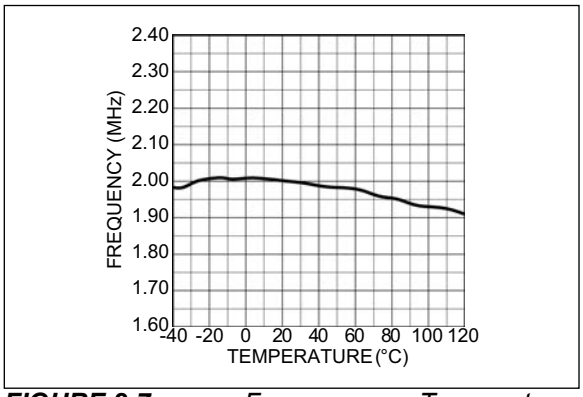


FIGURE 2-7: *Frequency vs. Temperature.*

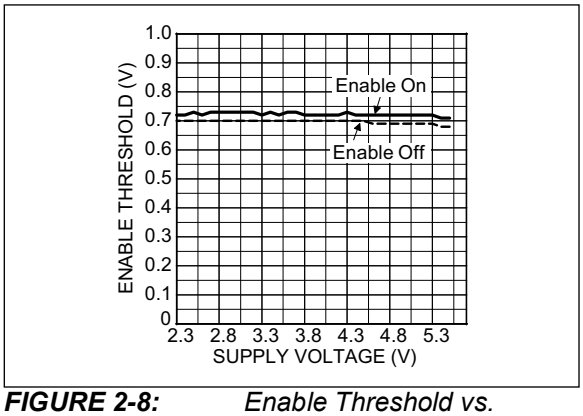


FIGURE 2-8: *Enable Threshold vs. Supply Voltage.*

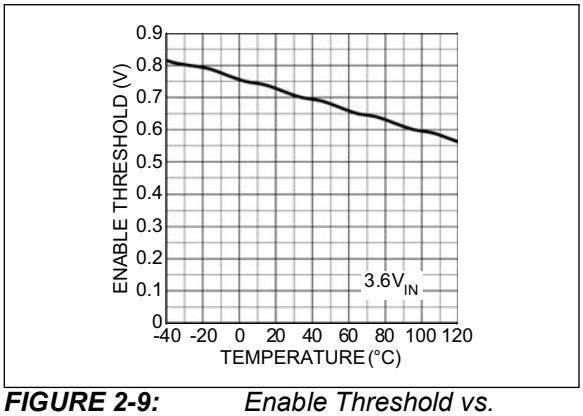


FIGURE 2-9: *Enable Threshold vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SW	Switch (Output): Internal power MOSFET output switches.
2	VIN	Supply Voltage (Input): Requires bypass capacitor to GND.
3	SYNC_IN	Sync the main switching frequency to an external clock.
4	SYNC_OUT	An open collector output.
5	EN	A low level EN will power down the device, reducing the quiescent current to under 1 µA.
6	FB	Input to the error amplifier. Connect to the external resistor divider network to set the output voltage.
7	BIAS	Internal circuit bias supply, nominally 2.3V. Must be decoupled to signal ground with a 0.01 µF capacitor.
8, 9, 10	GND	Ground.
EP	GND	Ground, backside pad.

4.0 FUNCTIONAL DESCRIPTION

4.1 VIN

VIN provides power to the output and to the internal bias supply. The supply voltage range is from 2.3V to 5.5V. A minimum 1 µF ceramic is recommended for bypassing the input supply.

4.2 Enable

The Enable pin provides a logic level control of the output. In the off state, supply current of the device is greatly reduced (typically <1 µA). Also, in the off state, the output drive is placed in a “tri-stated” condition, where both the high side P-Channel MOSFET and the low-side N-Channel are in an off or non-conducting state. Do not drive the enable pin above the supply voltage.

4.3 Sync_In

Sync_In pin enables the ability to change the fundamental switching frequency. The Sync_In frequency has a minimum frequency of 1.6 MHz and a maximum sync frequency of 2.5 MHz.

Careful attention should be paid to not driving the Sync_In pin greater than the supply voltage. While this will not damage the device, it can cause improper operation.

4.4 Sync_Out

Sync_Out is an open collector output that provides a signal equal to the internal oscillator frequency. This creates the ability for multiple MIC2202s to be connected together in a host-client configuration for frequency matching of the converters. A typical 10 kΩ resistor is recommended for a pull-up resistor.

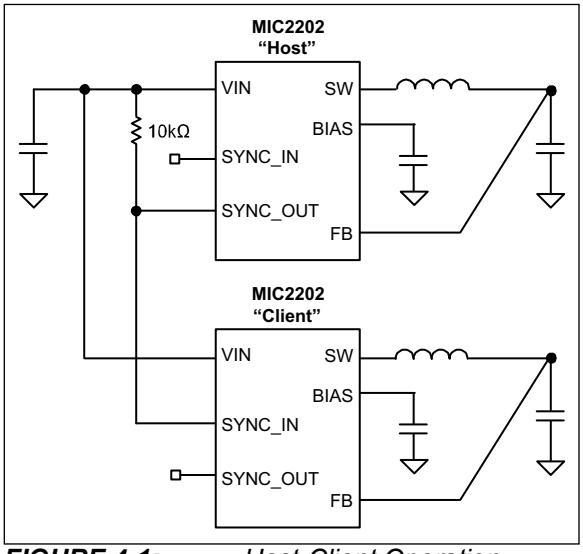


FIGURE 4-1: *Host-Client Operation.*

4.5 Bias

The bias supply is an internal 2.3V linear regulator that supplies the internal biasing voltage to the MIC2202. A 10 nF ceramic capacitor is required on this pin for bypassing. Do not use the bias pin as a supply. The bias pin was designed to supply internal power only.

4.6 Feedback

The feedback pin provides the control path to control the output. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. Refer to the Feedback section in the Applications Information section for more detail.

5.0 APPLICATION INFORMATION

5.1 Input Capacitor

A minimum 1 µF ceramic capacitor is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics, aside from losing most of their capacitance over temperature, also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

5.2 Output Capacitor

The MIC2202 was designed specifically for the use of a 1 µF ceramic output capacitor. This value can be increased to improve transient performance. Because the MIC2202 is voltage mode, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V or Z5U capacitors will cause instability in the device.

Total output capacitance should not exceed 15 µF. Large values of capacitance can cause current limit to engage during start-up. If greater than 15 µF is required, a feed-forward capacitor from the output to the feedback node should be used to slow the start-up time.

5.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC2202 is designed for use with a 1 µH to 4.7 µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their respective data sheets.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations section for a more detailed description.

5.4 Bias Capacitor

A small 10 nF ceramic capacitor is required to bypass the bias pin. The use of low-ESR ceramics provides improved filtering for the bias supply.

5.5 Efficiency Considerations

Efficiency is defined as the amount of useful output power divided by the amount of power consumed.

EQUATION 5-1:

$$\text{Efficiency } \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, which reduces the need for heat sinks and thermal design considerations; it also reduces the consumption of current for battery-powered applications. Reduced current draw from a battery increases the device's operating time, which is critical in handheld devices.

There are two loss terms in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the ON cycle. Power loss is equal to the high-side MOSFET $R_{DS(ON)}$ multiplied by the Switch Current squared. During the OFF cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss. The current required to drive the gates on and off at a constant 2 MHz frequency and the switching transitions make up the switching losses.

Figure 5-1 shows an efficiency curve. The efficiency losses in the non-shaded portion, from 0 mA to 200 mA, are dominated by quiescent current losses, gate drive, and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

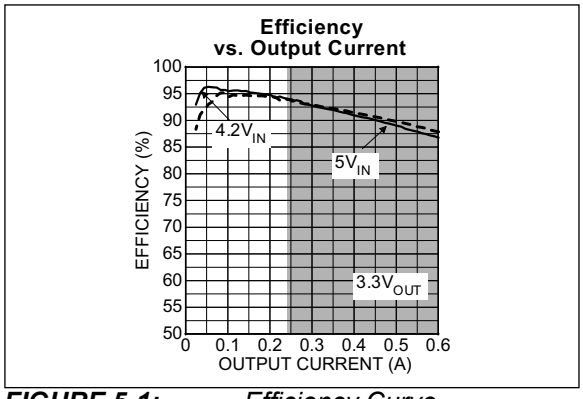


FIGURE 5-1: *Efficiency Curve.*

The shaded region, 200 mA to 500 mA, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source threshold on the internal MOSFETs, reducing the internal $R_{DS(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

EQUATION 5-2:

$$L_{PD} = I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows

EQUATION 5-3:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L_{PD}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductances reduce the peak-to-peak ripple current, which minimize losses. The following graph illustrates the effects of inductance value at light load.

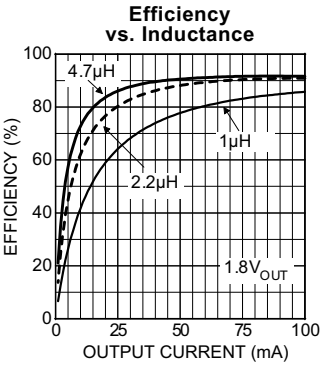


FIGURE 5-2: *Efficiency vs. Inductance.*

5.6 Compensation

The MIC2202 is an internally compensated, voltage mode buck regulator. Voltage mode is achieved by creating an internal 2 MHz ramp signal and using the output of the error amplifier to pulse width modulate the switch node, maintaining output voltage regulation. With a typical gain bandwidth of 500 kHz, the MIC2202 is capable of extremely fast transient responses.

The MIC2202 is designed to be stable with a 2.2 µH inductor and a 1 µF ceramic (X5R) output capacitor.

These values can be interchanged (i.e. 1 µH inductor and a 2.2 µF capacitor). The trade off between changing these values is that with a larger inductor, there is a reduced peak-to-peak current that yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

5.7 Feedback

The MIC2202 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.5V reference voltage and adjusts the output voltage to maintain regulation. To calculate the resistor divider network for the desired output is as follows:

EQUATION 5-4:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

Where:
V_{REF} = 0.5V
V_{OUT} = The desired output voltage.

A 10 kΩ or lower resistor value from the output to the feedback is recommended. Larger resistor values require an additional capacitor (feed-forward) from the output to the feedback. The large high side resistor value and the parasitic capacitance on the feedback pin (~10 pF) can cause an additional pole in the loop. The additional pole can create a phase loss at high frequency. This phase loss degrades transient response by reducing phase margin. Adding feed-forward capacitance negates the parasitic capacitive effects of the feedback pin. A minimum 1000 pF capacitor is recommended for feed-forward capacitance.

Also, large feedback resistor values increase the impedance, making the feedback node more susceptible to noise pick-up. A feed-forward capacitor would also reduce noise pick-up by providing a low impedance path to the output.

5.8 PWM Operation

The MIC2202 is a pulse width modulation (PWM) controller. By controlling the ratio of on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC2202 will run at 100% duty cycle.

The MIC2202 provides constant switching at 2 MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin to ground. Because the low-side N-Channel MOSFET provides the current path during the off cycle, a freewheeling Schottky diode from the switch node to ground is not required.

PWM control provides fixed frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

5.9 Synchronization

Sync_In allows the user to change the frequency from 2 MHz up to 2.5 MHz or down to 1.6 MHz. This allows the ability to control the fundamental frequency and all the resultant harmonics. Maintaining a predictable frequency creates the ability to either shift the harmonics away from sensitive carrier and intermediate frequency bands or to accurately filter out specific harmonic frequencies.

The Sync_Out function pin allows for the ability to be able to sync up multiple MIC2202s in a “daisy-chain”, connecting Sync_Out to Sync_In of the other MIC2202. Synchronizing multiple MIC2202s benefits much in the same way as syncing up one MIC2202. All regulators will run at the same fundamental frequency, resulting in matched harmonic frequencies, simplifying designing for sensitive communication equipment.

6.0 MIC2202YMM WITH 2.2 µH INDUCTOR AND 1 µF OUTPUT CAPACITOR

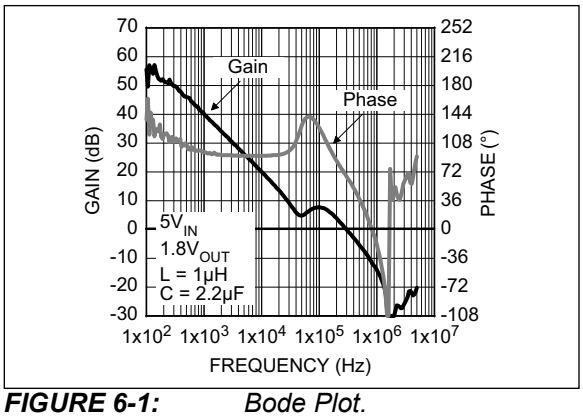


FIGURE 6-1: *Bode Plot.*

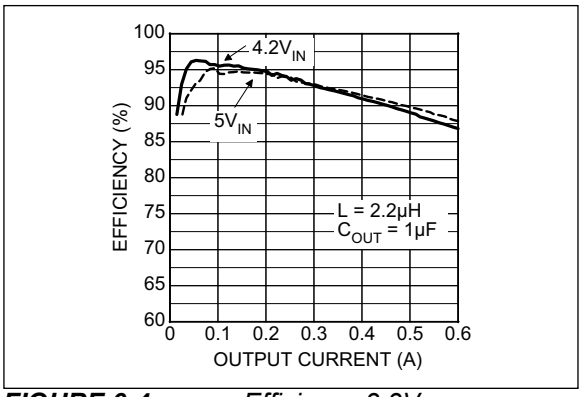


FIGURE 6-4: *Efficiency 3.3V_{OUT}.*

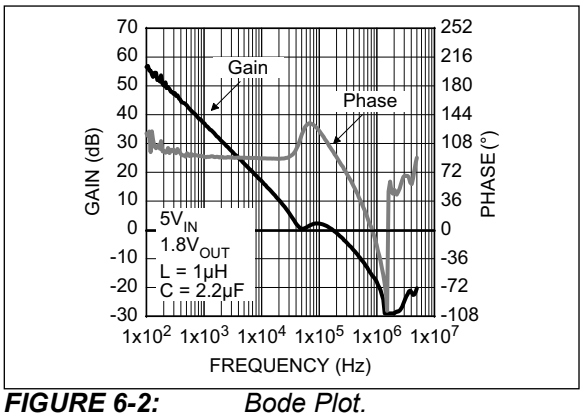


FIGURE 6-2: *Bode Plot.*

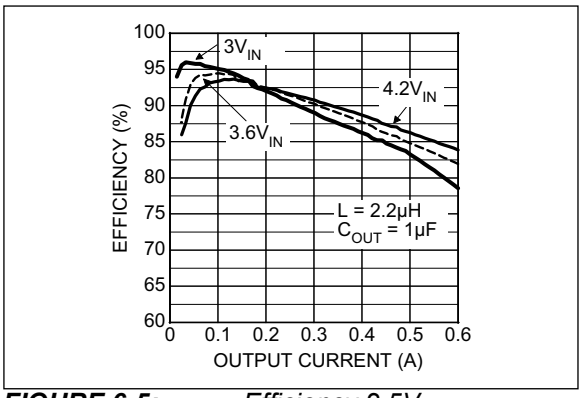


FIGURE 6-5: *Efficiency 2.5V_{OUT}.*

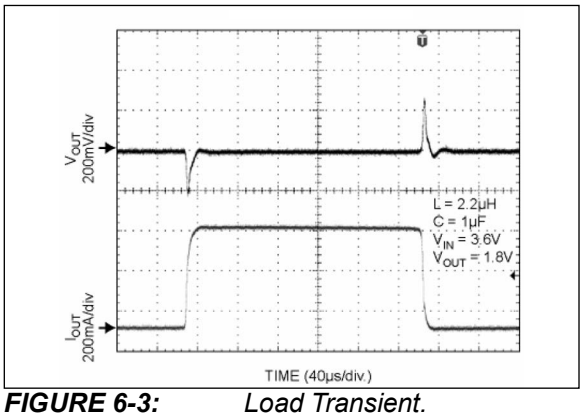


FIGURE 6-3: *Load Transient.*

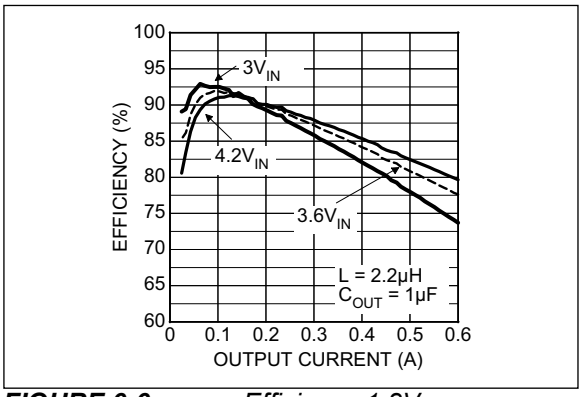


FIGURE 6-6: *Efficiency 1.8V_{OUT}.*

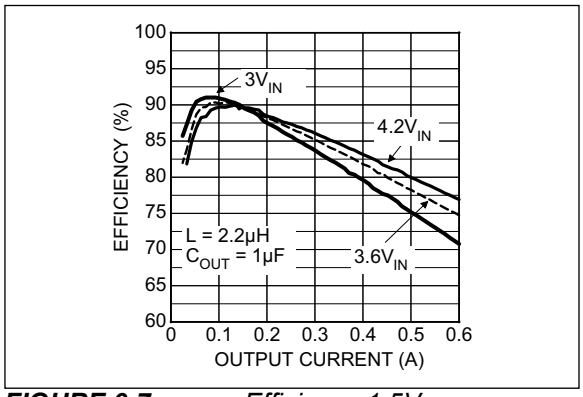


FIGURE 6-7: *Efficiency 1.5V_{OUT}.*

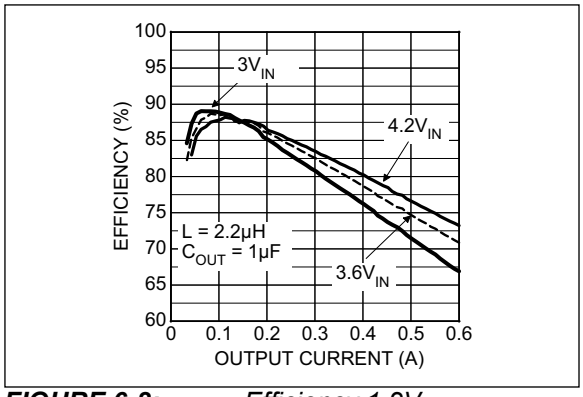


FIGURE 6-8: *Efficiency 1.2V_{OUT}.*

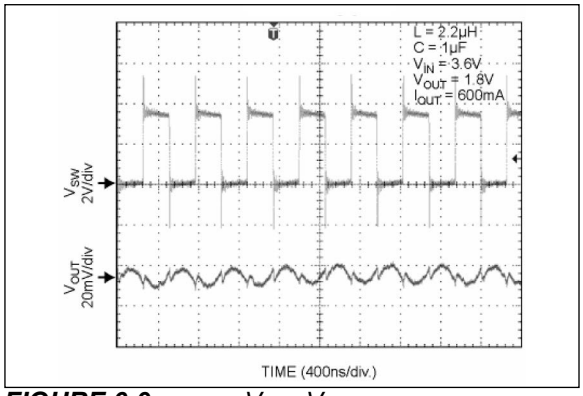


FIGURE 6-9: *V_{SW}-V_{RIPPLE}.*

7.0 MIC2202YMM WITH 2.2 µH INDUCTOR AND 1 µF OUTPUT CAPACITOR SCHEMATIC

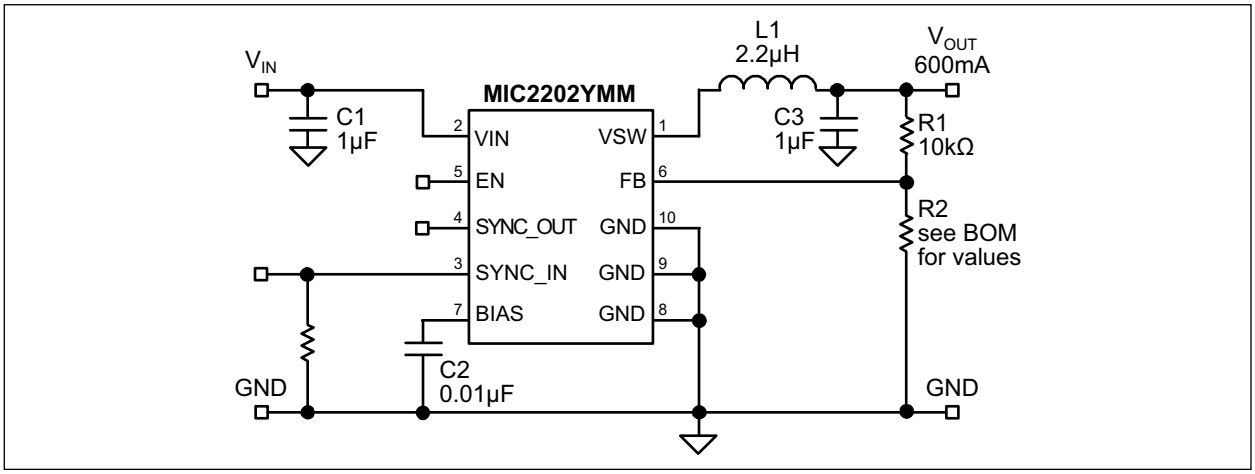


TABLE 7-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1, C3	06036D105MAT2	AVX	1 µF Ceramic Capacitor X5R, 6.3V, Size 0603	2
	GRM185R60J105KE21D	Murata		
C2	0201ZD103MAT2	AVX	10 nF Ceramic Capacitor 6.3V, Size 0201	1
	GRM033R10J103KA01D	Murata	10 nF Ceramic Capacitor 6.3V, Size 0202	
L1	LQH32CN2R2M53K	Murata	2.2 µH Inductor 97 mΩ (3.2 mmx2.5 mmx1.55 mm)	1
	CDRH2D14-2R2	Sumida	2.2 µH Inductor 94 mΩ (3.2 mmx3.2 mmx1.55 mm)	
R1	CRCW04021002F	Vishay-Dale	10 kΩ 1%, Size 0402	1
R2	CRCW04021781F	Vishay-Dale	1.78 kΩ 1%, Size 0402, For $3.3V_{OUT}$	1
	CRCW04022491F		2.49 kΩ 1%, Size 0402, For $2.5V_{OUT}$	
	CRCW04023831F		3.83 kΩ 1%, Size 0402, For $1.8V_{OUT}$	
	CRCW04024991F		4.99 kΩ 1%, Size 0402, For $1.5V_{OUT}$	
	CRCW04027151F		7.15 kΩ 1%, Size 0402, For $1.2V_{OUT}$	
	CRCW04021002F		10 kΩ 1%, Size 0402, For $1V_{OUT}$	
	N/A	—	Open, For $0.5V_{OUT}$	—
U1	MIC2202YMM	Microchip	2 MHz High Efficiency Synchronous Buck Regulator	1

8.0 MIC2202YMM WITH 1 µH INDUCTOR AND 2.2 µF OUTPUT CAPACITOR

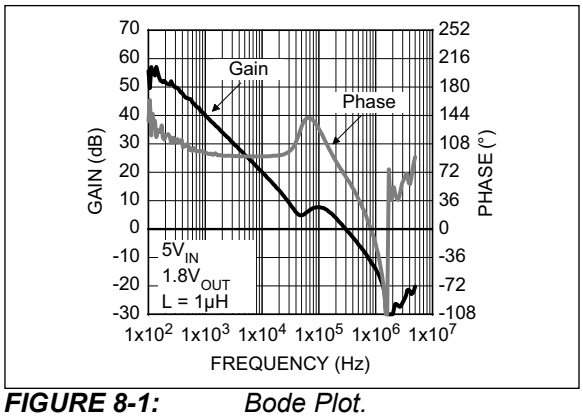


FIGURE 8-1: *Bode Plot.*

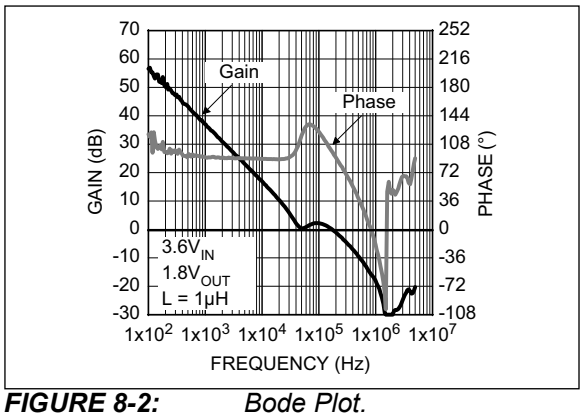


FIGURE 8-2: *Bode Plot.*

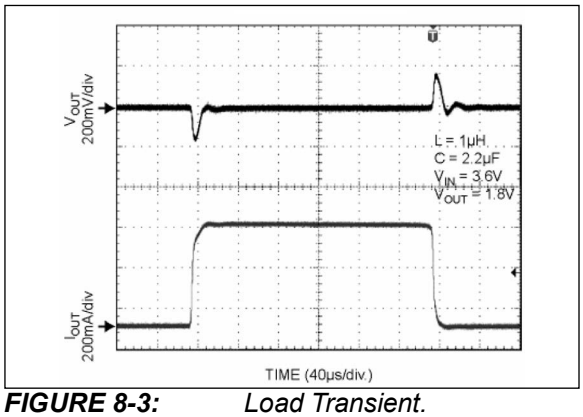


FIGURE 8-3: *Load Transient.*

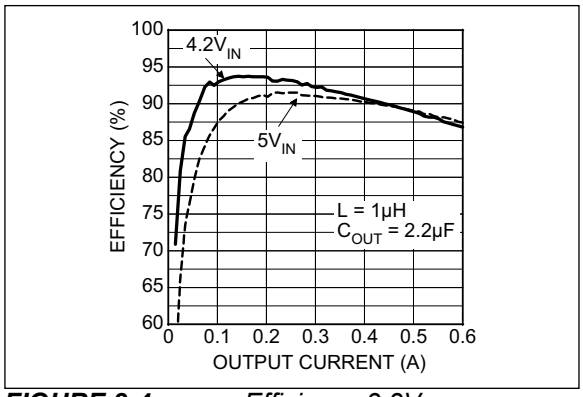


FIGURE 8-4: *Efficiency 3.3V_{OUT}.*

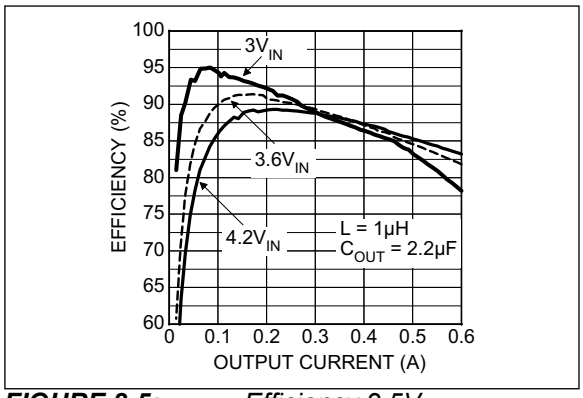


FIGURE 8-5: *Efficiency 2.5V_{OUT}.*

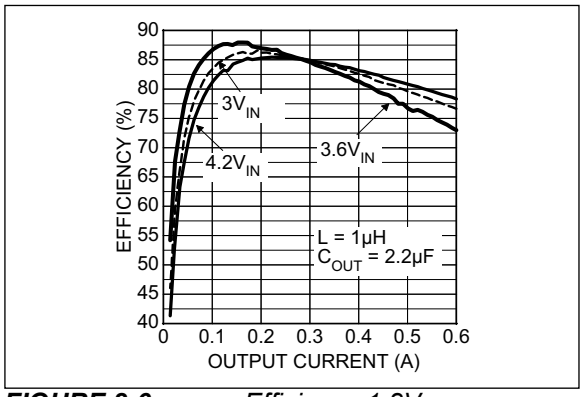


FIGURE 8-6: *Efficiency 1.8V_{OUT}.*

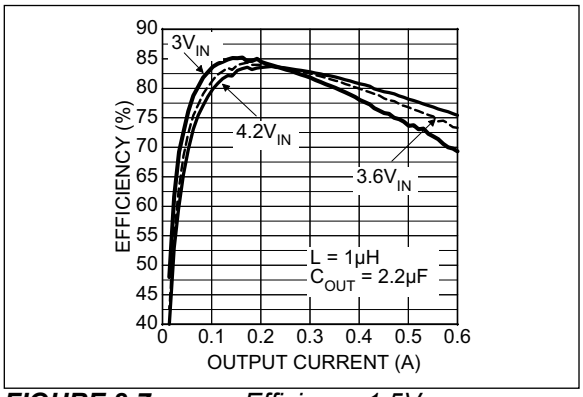


FIGURE 8-7: *Efficiency 1.5V_{OUT}.*

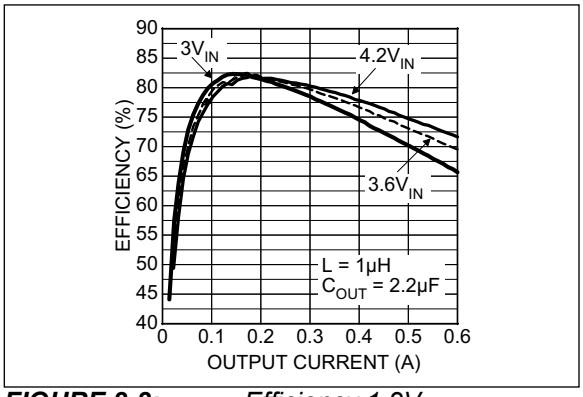


FIGURE 8-8: *Efficiency 1.2V_{OUT}.*

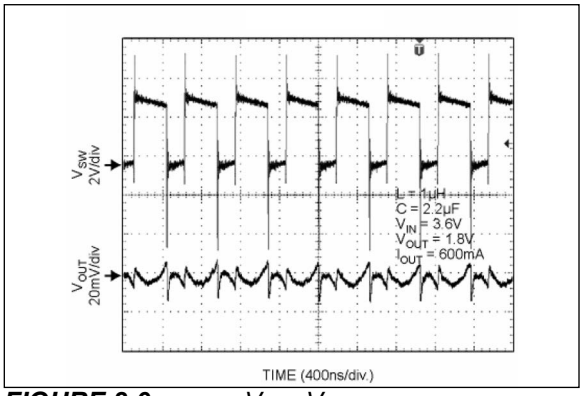


FIGURE 8-9: *V_{SW}-V_{RIPPLE}.*

9.0 MIC2202YMM WITH 1 µH INDUCTOR AND 2.2 µF OUTPUT CAPACITOR SCHEMATIC

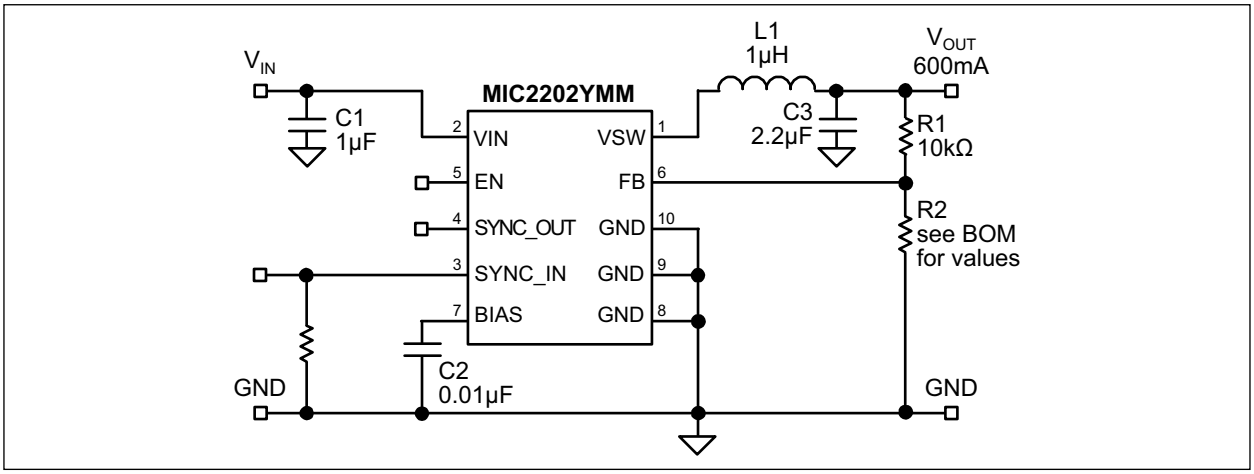


TABLE 9-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1	06036D105MAT2	AVX	1 µF Ceramic Capacitor X5R, 6.3V, Size 0603	1
	GRM185R60J105KE21D	Murata		
C2	0201ZD103MAT2	AVX	10 nF Ceramic Capacitor 6.3V, Size 0201	1
	GRM033R10J103KA01D	Murata	10 nF Ceramic Capacitor 6.3V, Size 0202	
C3	06036D225MAT2	AVX	2.2 µF Ceramic Capacitor X5R, 6.3V, Size 0603	1
	GRM033R10J103KA01D	Murata		
L1	LQH32CN1R0M53K	Murata	1 µH Inductor 60 mΩ (3.2 mmx2.5 mmx1.55 mm)	1
	CDRH2D14-1R5	Sumida	1.5 µH Inductor 63 mΩ (3.2 mmx3.2 mmx1.55 mm)	
R1	CRCW04021002F	Vishay-Dale	10 kΩ 1%, Size 0402	1
R2	CRCW04021781F	Vishay-Dale	1.78 kΩ 1%, Size 0402, For $3.3V_{OUT}$	1
	CRCW04022491F		2.49 kΩ 1%, Size 0402, For $2.5V_{OUT}$	
	CRCW04023831F		3.83 kΩ 1%, Size 0402, For $1.8V_{OUT}$	
	CRCW04024991F		4.99 kΩ 1%, Size 0402, For $1.5V_{OUT}$	
	CRCW04027151F		7.15 kΩ 1%, Size 0402, For $1.2V_{OUT}$	
	CRCW04021002F		10 kΩ 1%, Size 0402, For $1V_{OUT}$	
	N/A	—	Open, For $0.5V_{OUT}$	—
U1	MIC2202YMM	Microchip	2 MHz High Efficiency Synchronous Buck Regulator	1

10.0 MIC2202YMM WITH 4.7 µH INDUCTOR AND 1 µF OUTPUT CAPACITOR

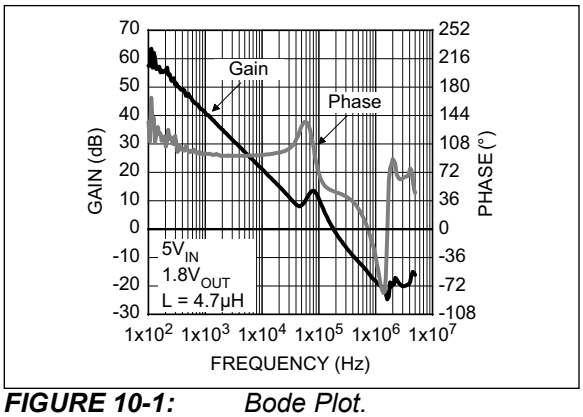


FIGURE 10-1: *Bode Plot.*

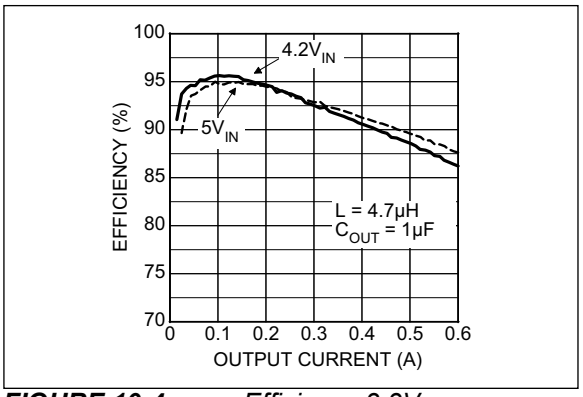


FIGURE 10-4: *Efficiency 3.3V_{OUT}.*

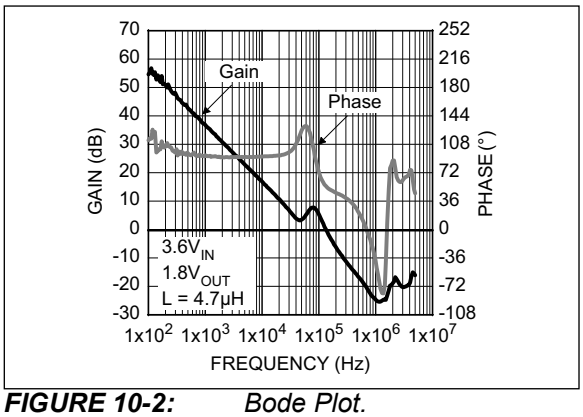


FIGURE 10-2: *Bode Plot.*

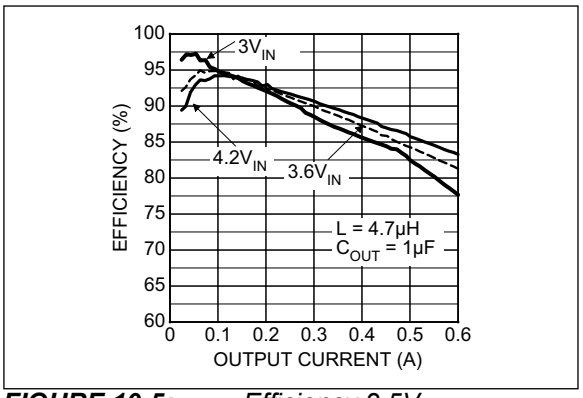


FIGURE 10-5: *Efficiency 2.5V_{OUT}.*

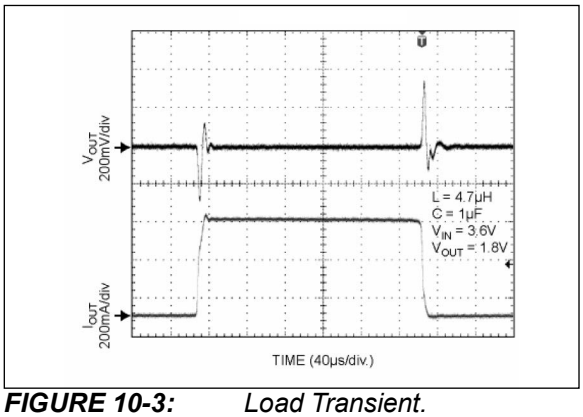


FIGURE 10-3: *Load Transient.*

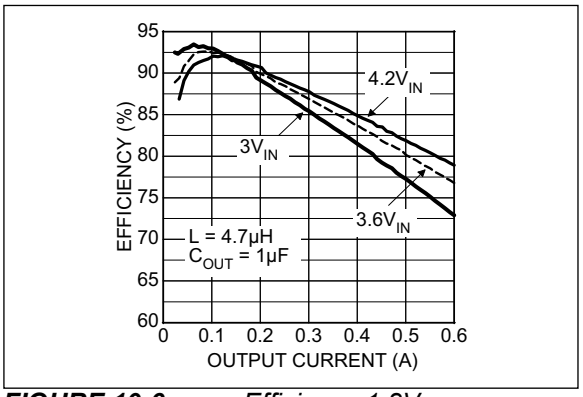


FIGURE 10-6: *Efficiency 1.8V_{OUT}.*

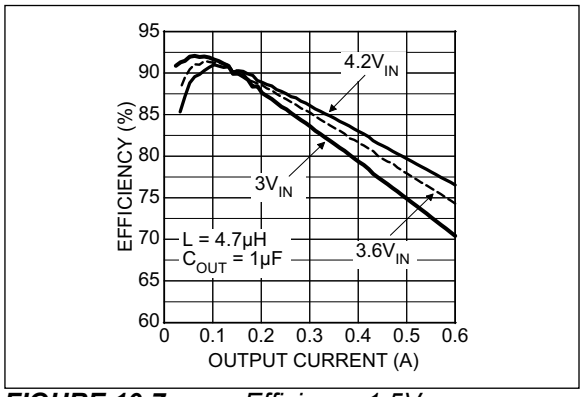


FIGURE 10-7: *Efficiency 1.5V_{OUT}.*

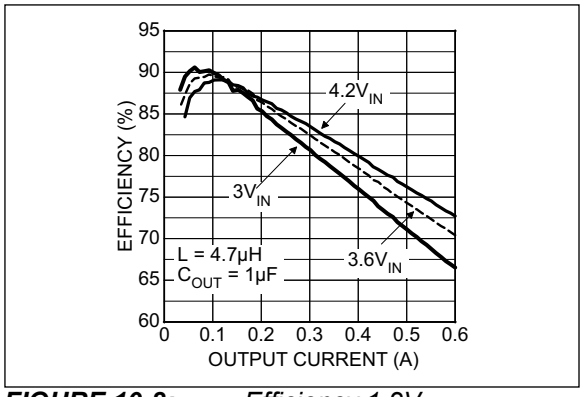


FIGURE 10-8: *Efficiency 1.2V_{OUT}.*

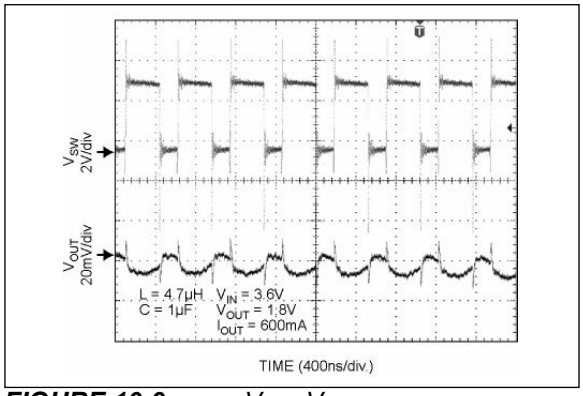


FIGURE 10-9: *V_{SW}-V_{RIPPLE}.*

11.0 MIC2202YMM WITH 4.7 µH INDUCTOR AND 1 µF OUTPUT CAPACITOR SCHEMATIC

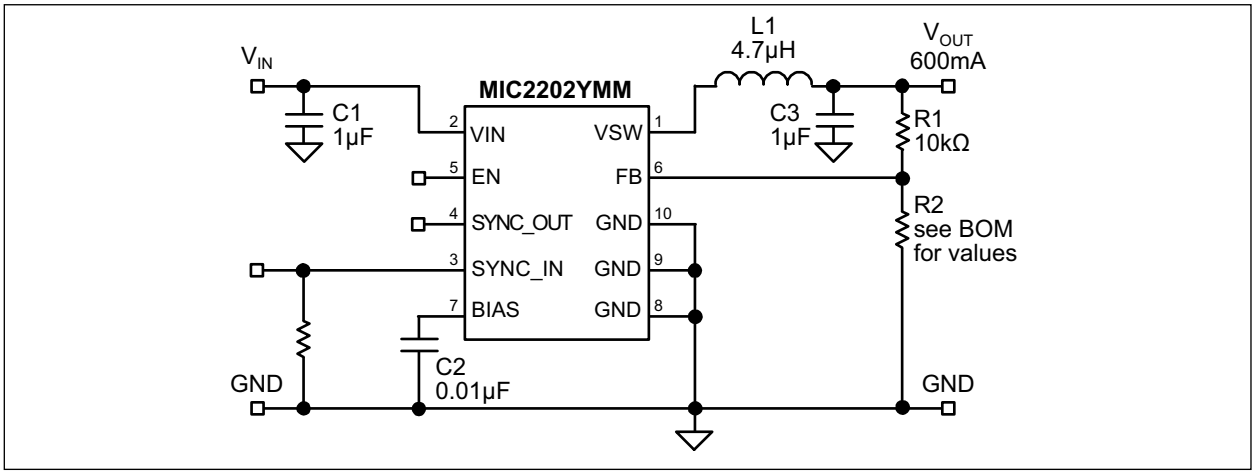


TABLE 11-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1, C3	06036D105MAT2	AVX	1 µF Ceramic Capacitor X5R, 6.3V, Size 0603	2
	GRM185R60J105KE21D	Murata		
C2	0201ZD103MAT2	AVX	10 nF Ceramic Capacitor 6.3V, Size 0201	1
	GRM033R10J103KA01D	Murata	10 nF Ceramic Capacitor 6.3V, Size 0202	
L1	LQH32CN4R7M53K	Murata	4.7 µH Inductor 150 mΩ (3.2 mmx2.5 mmx1.55 mm)	1
	CDRH2D14-4R7	Sumida	4.7 µH Inductor 169 mΩ (3.2 mmx3.2 mmx1.55 mm)	
R1	CRCW04021002F	Vishay-Dale	10 kΩ 1%, Size 0402	1
R2	CRCW04021781F	Vishay-Dale	1.78 kΩ 1%, Size 0402, For 3.3V_{OUT}	1
	CRCW04022491F		2.49 kΩ 1%, Size 0402, For 2.5V_{OUT}	
	CRCW04023831F		3.83 kΩ 1%, Size 0402, For 1.8V_{OUT}	
	CRCW04024991F		4.99 kΩ 1%, Size 0402, For 1.5V_{OUT}	
	CRCW04027151F		7.15 kΩ 1%, Size 0402, For 1.2V_{OUT}	
	CRCW04021002F		10 kΩ 1%, Size 0402, For 1V_{OUT}	
	N/A	—	Open, For 0.5V_{OUT}	—
U1	MIC2202YMM	Microchip	2 MHz High Efficiency Synchronous Buck Regulator	1

12.0 MIC2202YMM WITH 1 µH INDUCTOR AND 4.7 µF OUTPUT CAPACITOR

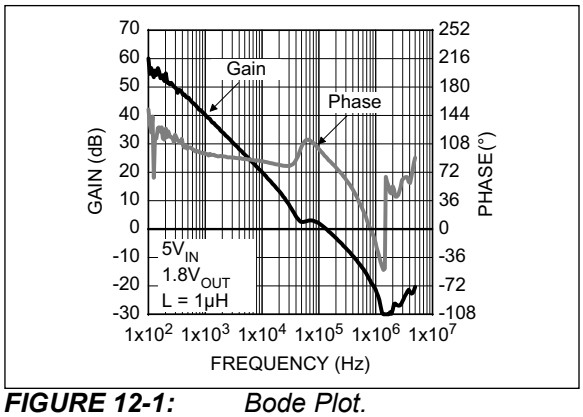


FIGURE 12-1: *Bode Plot.*

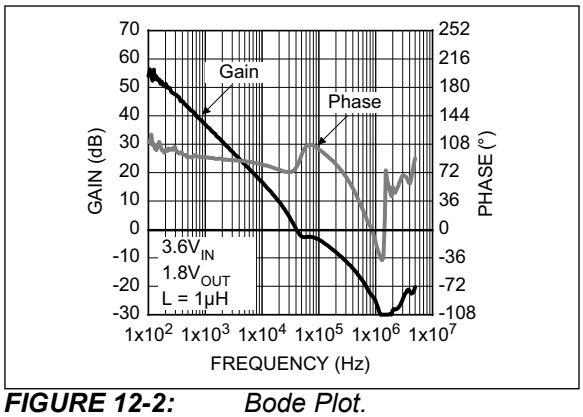


FIGURE 12-2: *Bode Plot.*

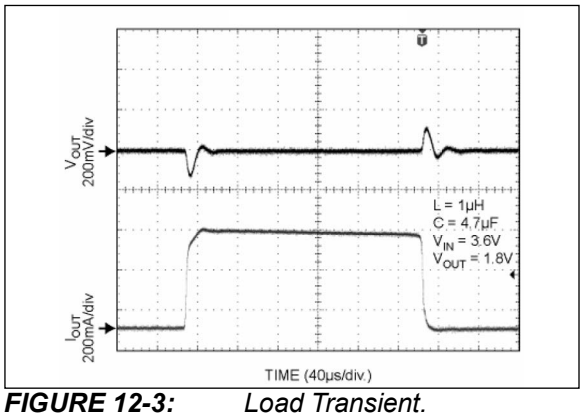


FIGURE 12-3: *Load Transient.*

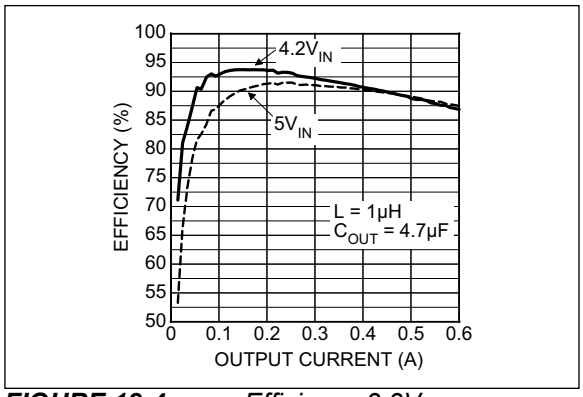


FIGURE 12-4: *Efficiency 3.3V_{OUT}.*

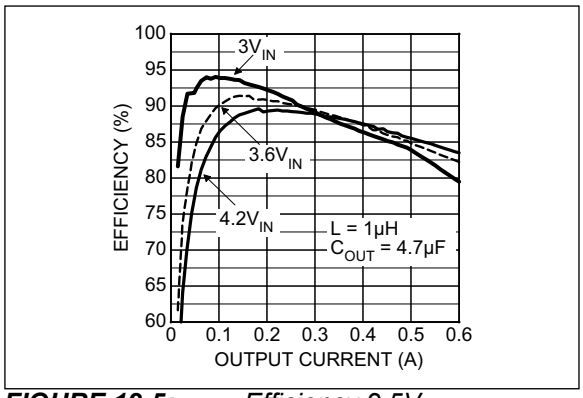


FIGURE 12-5: *Efficiency 2.5V_{OUT}.*

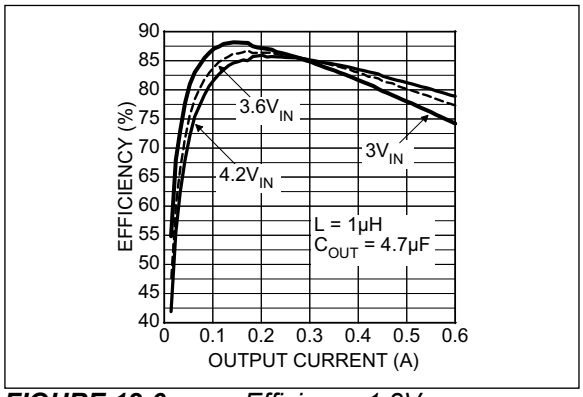


FIGURE 12-6: *Efficiency 1.8V_{OUT}.*

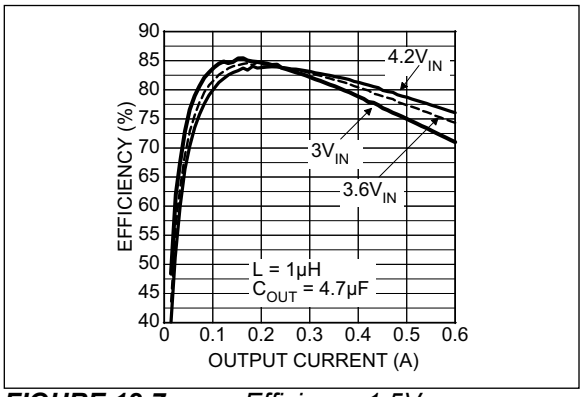


FIGURE 12-7: *Efficiency 1.5V_{OUT}.*

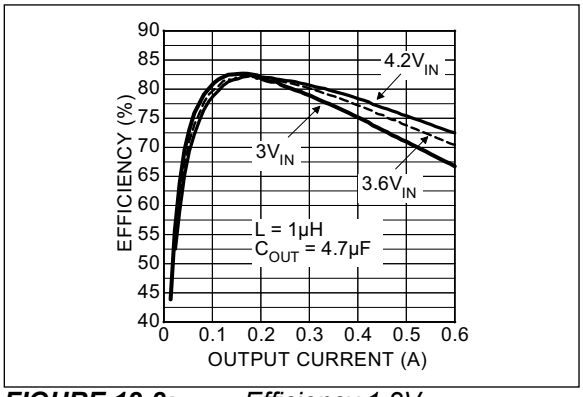


FIGURE 12-8: *Efficiency 1.2V_{OUT}.*

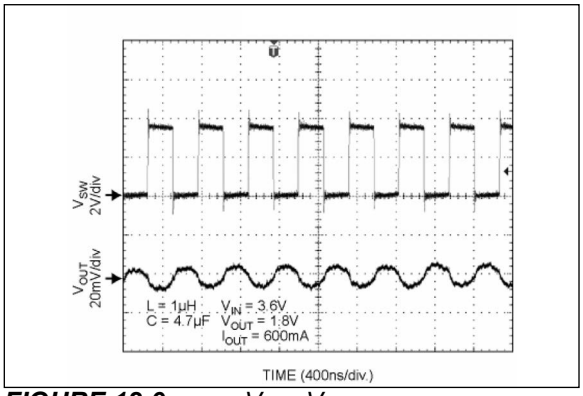


FIGURE 12-9: *V_{SW}-V_{RIPPLE}.*

13.0 MIC2202YMM WITH 1 µH INDUCTOR AND 4.7 µF OUTPUT CAPACITOR SCHEMATIC

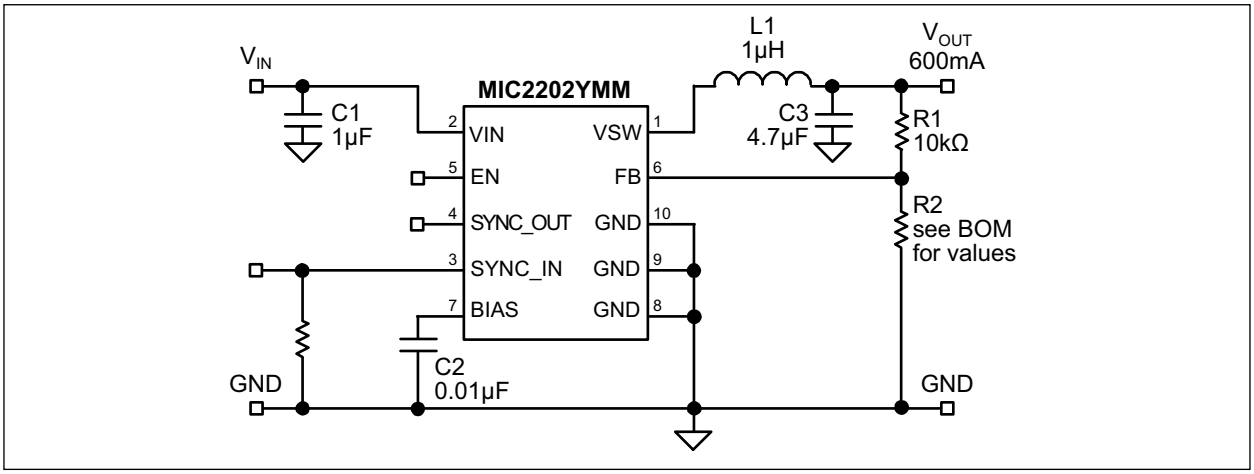


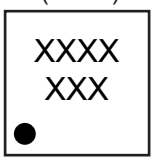
TABLE 13-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1	06036D105MAT2	AVX	1 µF Ceramic Capacitor X5R, 6.3V, Size 0603	1
	GRM185R60J105KE21D	Murata		
C2	0201ZD103MAT2	AVX	10 nF Ceramic Capacitor 6.3V, Size 0201	1
	GRM033R10J103KA01D	Murata	10 nF Ceramic Capacitor 6.3V, Size 0202	
C3	06036D475MAT2	AVX	4.7µF Ceramic Capacitor 4V, Size 0201	1
	GRM033R10J103KA01D	Murata	4.7µF Ceramic Capacitor 6.3V, Size 0202	
L1	LQH32CN1R0M53K	Murata	1 µH Inductor 60 mΩ (3.2 mmx2.5 mmx1.55 mm)	1
	CDRH2D14-1R5	Sumida	1.5 µH Inductor 63 mΩ (3.2 mmx3.2 mmx1.55 mm)	
R1	CRCW04021002F	Vishay-Dale	10 kΩ 1%, Size 0402	1
R2	CRCW04021781F	Vishay-Dale	1.78 kΩ 1%, Size 0402, For $3.3V_{OUT}$	1
	CRCW04022491F		2.49 kΩ 1%, Size 0402, For $2.5V_{OUT}$	
	CRCW04023831F		3.83 kΩ 1%, Size 0402, For $1.8V_{OUT}$	
	CRCW04024991F		4.99 kΩ 1%, Size 0402, For $1.5V_{OUT}$	
	CRCW04027151F		7.15 kΩ 1%, Size 0402, For $1.2V_{OUT}$	
	CRCW04021002F		10 kΩ 1%, Size 0402, For $1V_{OUT}$	
	N/A	—	Open, For $0.5V_{OUT}$	—
U1	MIC2202YMM	Microchip	2 MHz High Efficiency Synchronous Buck Regulator	1

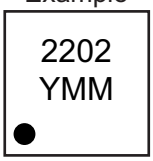
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

10-Lead MSOP* (Front)

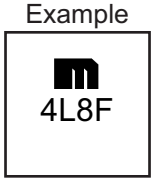


Example



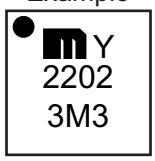
10-Lead MSOP* (Back)

Example



10-Lead VDFN*

Example

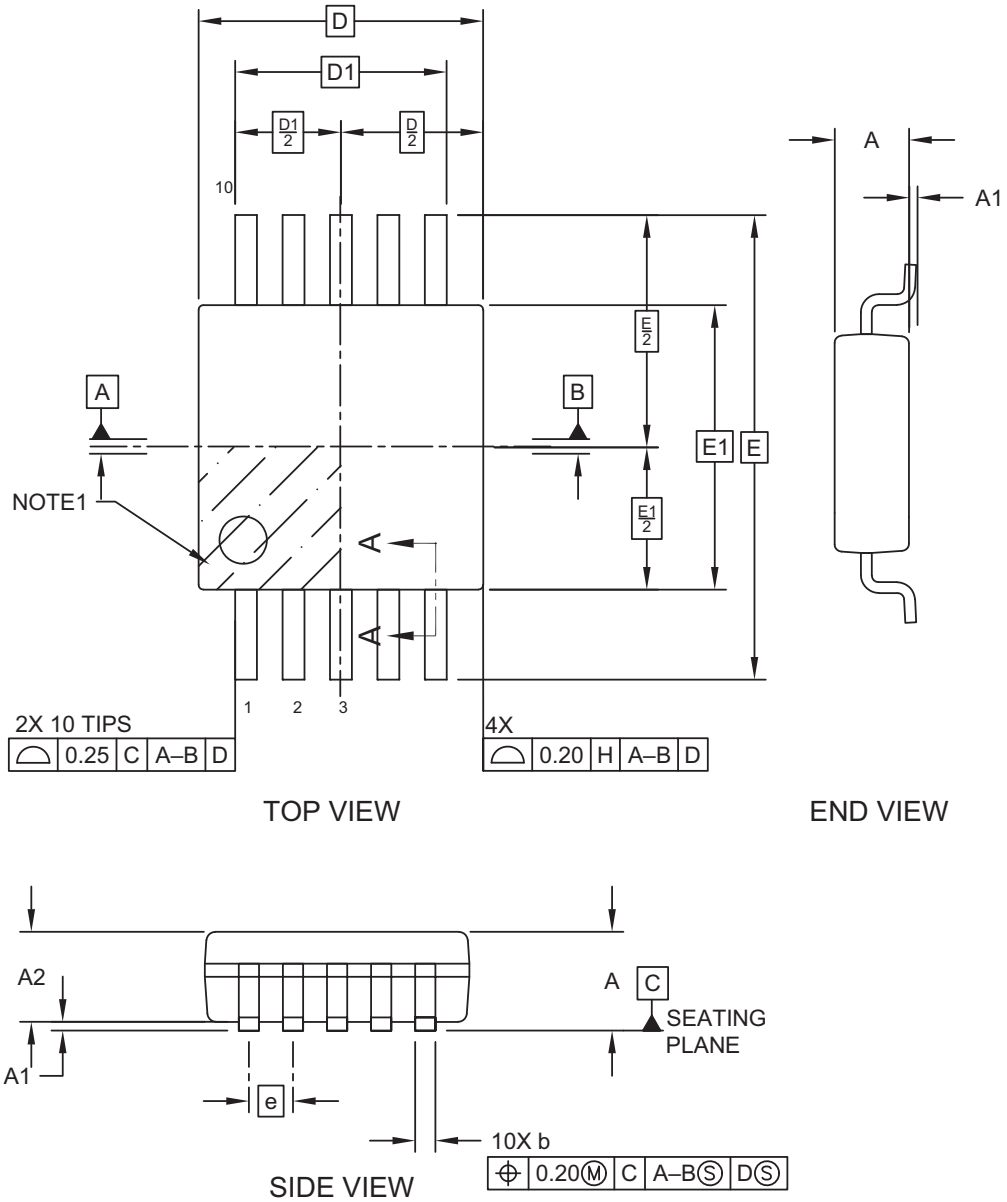


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

10-Lead Plastic Micro Small Outline Package (DQA)- 3x3x1.0 mm Body [MSOP]

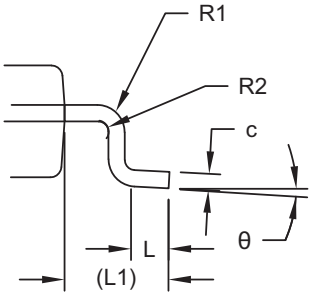
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



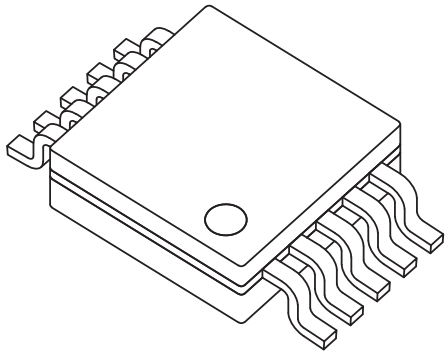
Microchip Technology Drawing C04-01081 Rev A Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (DQA)- 3x3x1.0 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A–A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.94	1.02	1.10
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.91	0.92	0.95
Overall Length	D		3.00 BSC	
Molded Package Length	D1		2.23 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.16	0.23	0.30
Terminal Thickness	c	0.13	0.15	0.23
Footprint	L	0.40	0.55	0.70
Terminal Length	L1		0.95 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	θ	0°	3°	6°

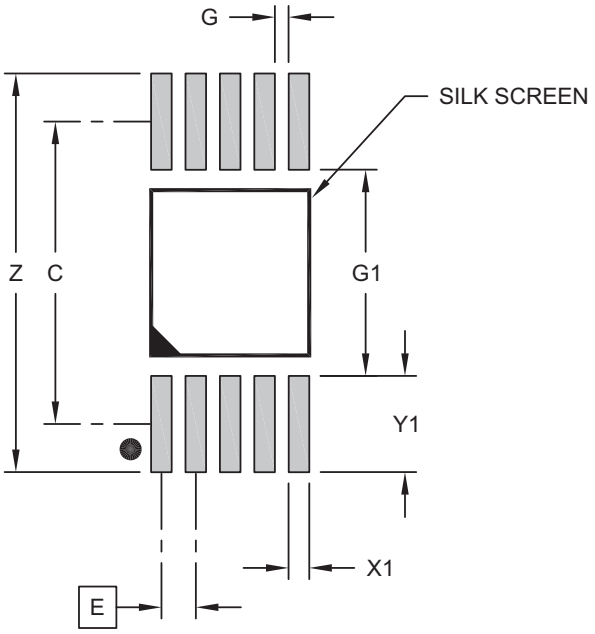
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-01081 Rev A Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (DQA)- 3x3x1.0 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			6.06
Contact Pad Width (X10)	X1	0.28	0.30	0.32
Contact Pad Length (X10)	Y1	1.24	1.26	1.28
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

Notes:

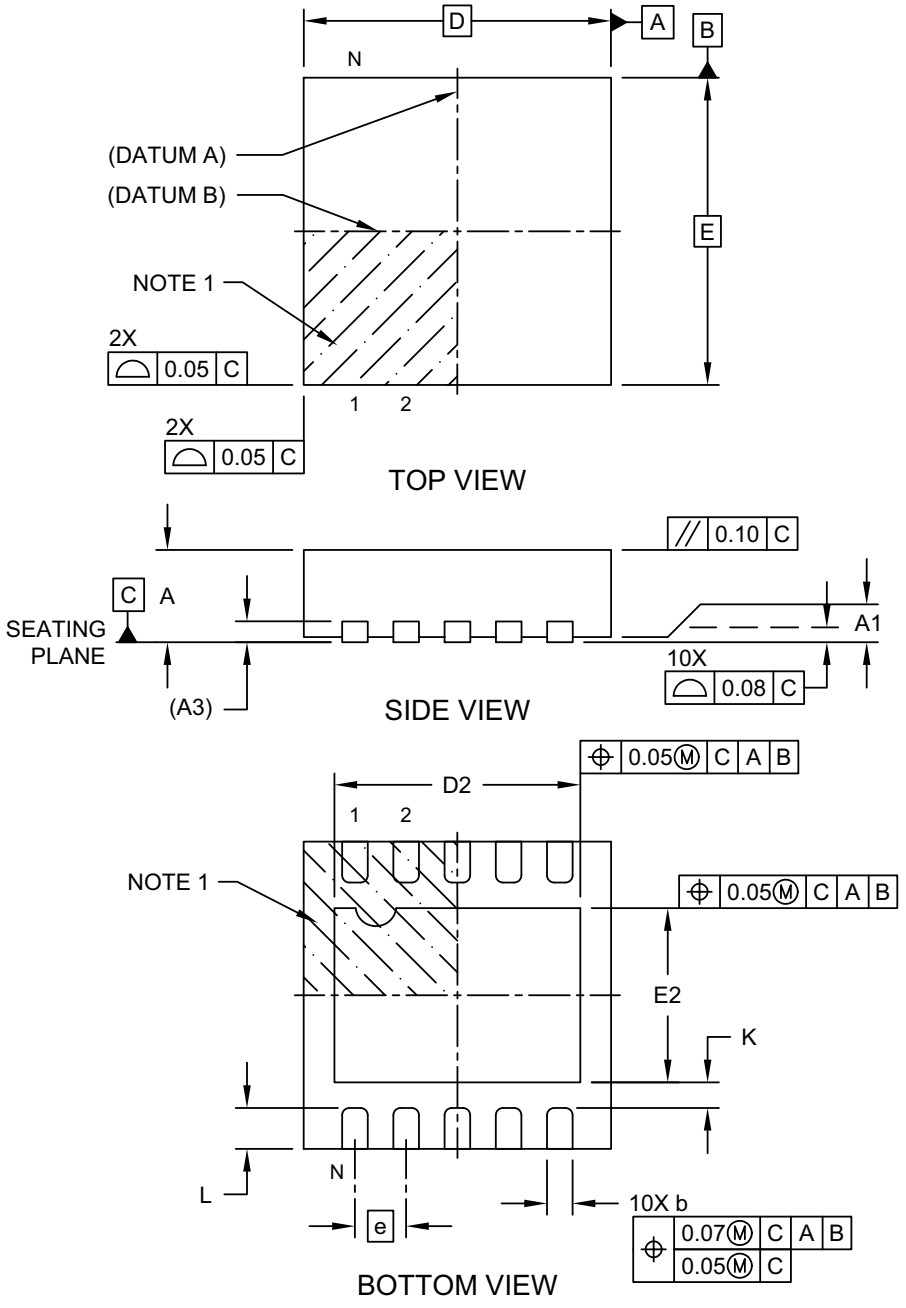
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-03081 Rev A

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN]

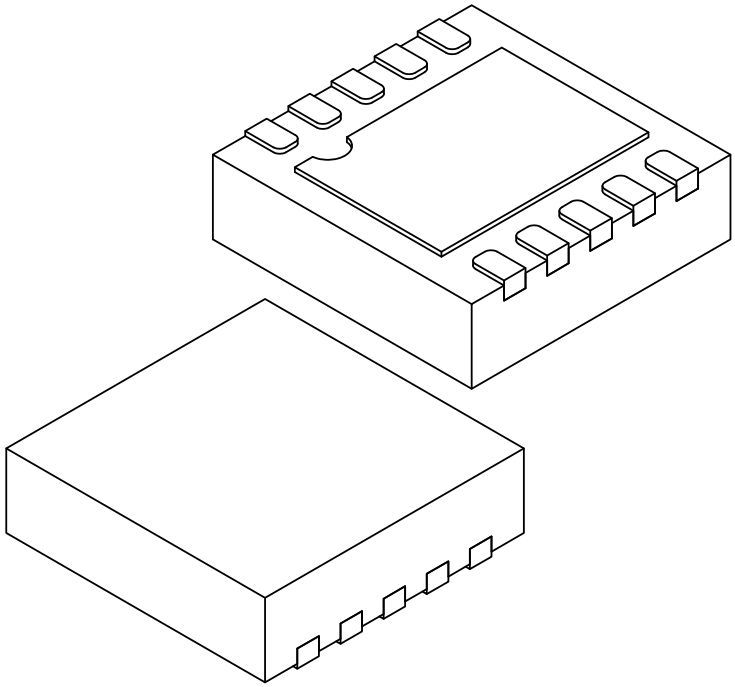
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1019-JFA Rev B Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.35	2.40	2.45
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.65	1.70	1.75
Terminal Width	b	0.17	0.22	0.27
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

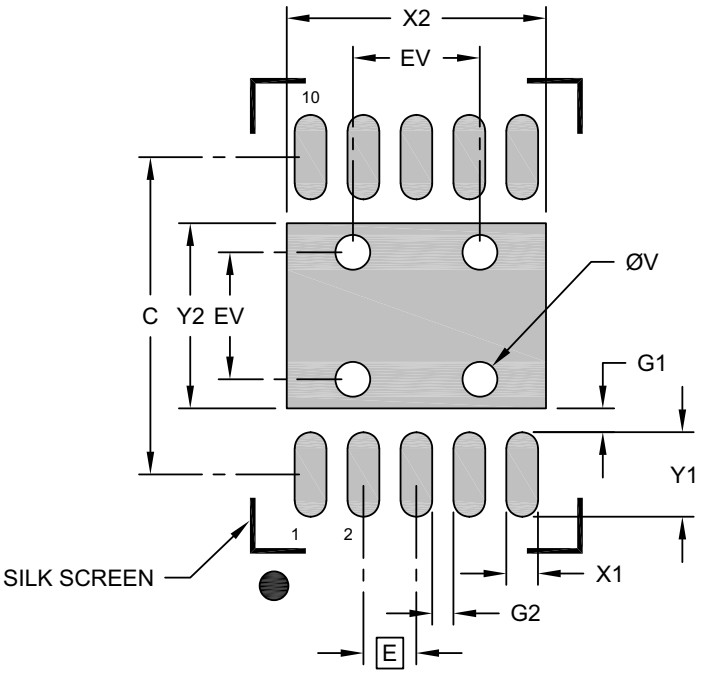
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1019-JFA Rev B Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.45
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C		3.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.80
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3019-JFA Rev B

APPENDIX A: REVISION HISTORY

Revision A (April 2025)

- Converted Micrel document MIC2202 to Microchip data sheet DS20007004A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	X	XX	-XX
Device	Temp. Range	Package	Media Type

Device:	MIC2202:		High Efficiency 2 MHz Synchronous Buck Converter 1 µF Stable PWM Regulator
Temperature Range:	Y	=	–40°C to +125°C
Package:	MM	=	10-Lead MSOP
	ML	=	10-Lead VDFN
Media Type:	<blank>	=	100/Tube
	TR	=	2,500/Reel (MM only)
	TR	=	5,000/Reel (ML only)

Examples:

a) MIC2202YMM:

MIC2202, –40°C to +125°C Temp. Range, 10-Lead MSOP, 100/Tube

b) MIC2202YMM-TR:

MIC2202, –40°C to +125°C Temp. Range, 10-Lead MSOP, 2,500/Reel

c) MIC2202YML:

MIC2202, –40°C to +125°C Temp. Range, 10-Lead VDFN, 100/Tube

d) MIC2202YML-TR:

MIC2202, –40°C to +125°C Temp. Range, 10-Lead VDFN, 5,000/Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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