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Demystifying Microchip's Adaptive Constant-On-Time Control and Ripple Injection Circuit Design

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INTRODUCTION

In the realm of power converters, control loops assume a pivotal role in influencing the performance of switching regulators (see Figure 1). Ongoing efforts to enhance power supply designs have catalyzed the evolution of control techniques. Microchip's Hyper Speed Control®, also recognized as Adaptive Constant-On-Time control, stands out among these innovative control methods, boasting advancements in tighter regulation, improved transient response, ease of design, and cost-effectiveness. This application note will cover the complexities of these advancements, detail their operational mechanisms, and provide design consideration insights specific to buck converters.

Voltage Mode Control (VMC), Current Mode Control (CMC), and Hysteretic Mode Control are three prominent methodologies employed in buck converters. VMC operates by adjusting the duty cycle based on the comparison between the output voltage and a reference voltage, offering simplicity and stability under steady-state conditions but exhibiting limitations in response time to external changes. In contrast, CMC modulates the duty cycle based on the inductor current, providing inherent current limiting for improved transient response, wider adaptability to input voltage variations, and enhanced noise immunity. However, CMC's design complexity and susceptibility to subharmonic oscillations and limitations in very low duty cycle operation must be considered. Hysteretic Mode Control, also known as On-Off Control or bang-bang control, toggles the power switch based on the comparison between the output voltage and predefined thresholds (as illustrated in Figure 2). It provides fast transient response with simplicity and robustness.

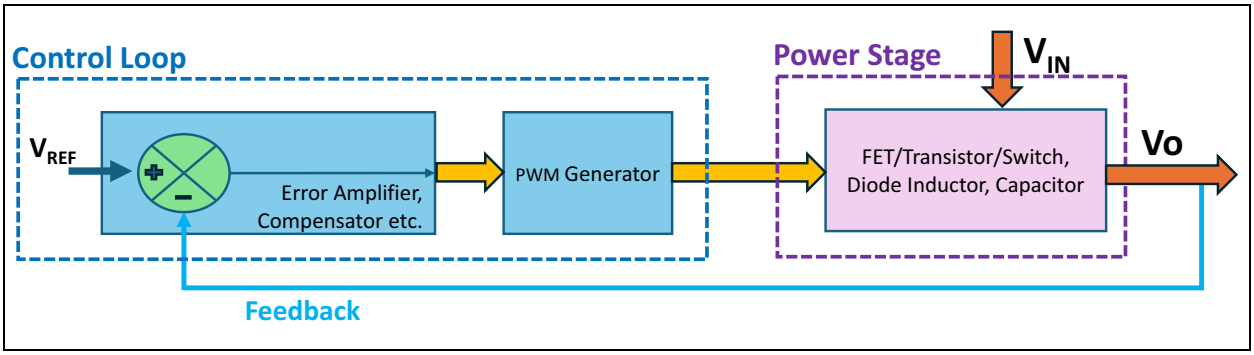


FIGURE 1: *Power Stage and Control Loop.*

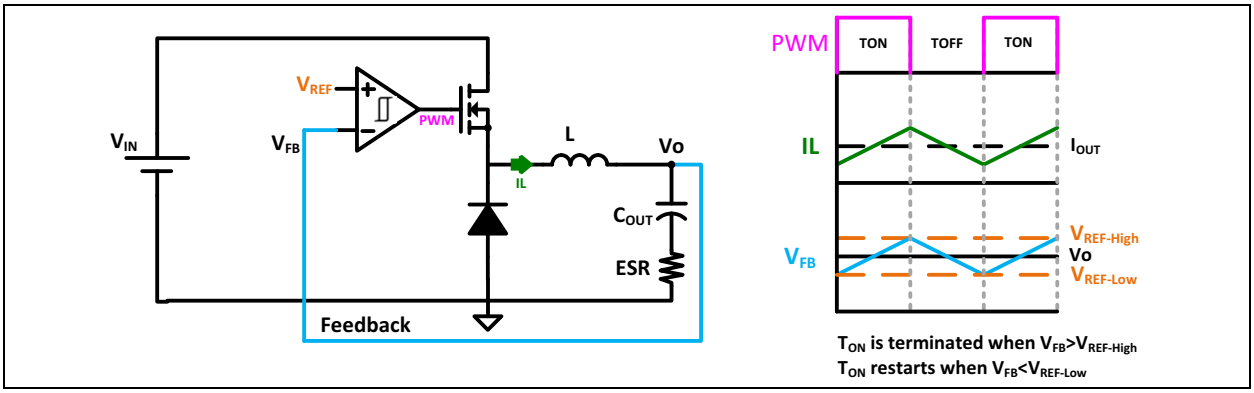


FIGURE 2: *Hysteretic Control Scheme.*

Constant-On-Time (COT) control stands out as an effective method for implementing hysteretic control. It offers a robust and straightforward approach, making it well-suited for various power electronics applications. COT control operates by maintaining a constant on-time for the power switch, which results in self-adjusting switching frequencies based on input voltage and load conditions. This adaptability ensures stable performance across varying operational parameters. Due to its simplicity, reliability, and versatility, COT control has gained widespread popularity and is commonly used in numerous power supply designs and voltage regulation systems. Its widespread use highlights its effectiveness as a control methodology in modern power electronics applications.

This application note begins with the **basic working principle of COT control** and then explores its advanced version, **Microchip's Hyper Speed Control® (ACOT control)**. With the primary objective of assisting in the d**esign process of Microchip's buck converters** (such as **Buck PWM controllers**, **Integrated FET regulators**, **Buck Power modules**, **and PMICs**), the key topics covered are:

- Basics of Constant-On-Time (COT) Control and Adaptive Constant-On-Time (ACOT) Control.
- Stabilizing the Control Loop using Output Ripple (Type 1)
  - Abnormal Switching Behavior and Critical ESR
- Ripple Injection Circuit Design for ACOT stabilization:
  - Using a Feed-Forward Capacitor (Type 2).
  - Using R-C from SW Node and Feed-Forward Capacitor (Type 3).
  - Ripple Injection from Dedicated Pin (Type 4).
- Flow chart of Step-by-Step Guide for Ripple Injection Design techniques.
- Control Loop Gain Analysis and strategies for optimizing transient response.
  - Transient Response with ACOT Control vs. Fixed-Frequency controls.
  - Detailed analysis of Feedback Ripple vs. Transient Response.
- Design Example: Type 3 Ripple Injection Design, detailing the process from design calculations to bench test results.
- A quick overview of Microchip's Analog Design Tools (Speed Up Control Loop Design with Microchip Analog Design Tools) to streamline circuit development.

1.0 CONSTANT-ON-TIME (COT) CONTROL

Understanding the fundamental operating principles is important as we delve into the design considerations of Constant-On-Time (COT) converters. Figure 3 illustrates the block diagram of COT control in a buck converter application. The buck converter is comprised of the High-Side (HS) and Low-Side (LS) switches, typically MOSFETs, along with the output filter (inductor and output capacitors), input capacitors, and the control stage.

The control stage includes comparators, an SR flip-flop (SR latch), a Constant ON time generator, and a Minimum OFF time generator. It is important to note that on-time and off-time are always referenced to the high-side switch operation. Moreover, the Constant ON time generator consists of a threshold comparator, a constant current source (I_T), a capacitor (C_{TON}), and a capacitor discharge switch (QN). The interaction between the constant current source and capacitor value determines the generation of T_{ON} (on-time).

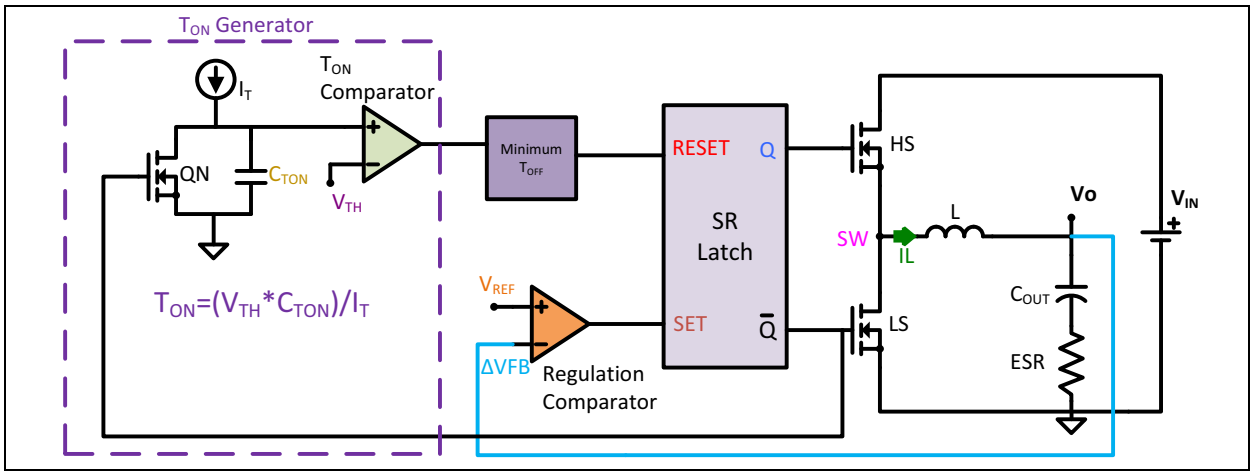


FIGURE 3: *Block Diagram of the COT Control Scheme.*

1.1 Basic Working Principle

First, the operation of the T_{ON} generator block will be examined. This block comprises of a comparator with its inverting terminal biased at a fixed threshold (V_{TH}) and its noninverting terminal connected to the positive side of the C_{TON} capacitor. A constant current source (I_T) charges the capacitor. When the voltage across the capacitor surpasses V_{TH}, the output of the T_{ON} generator switches to a high state; conversely, when the voltage falls below V_{TH}, the output switches to a low state. Refer to Figure 4 for the overall operation of the COT control method.

ON Time: The ON time begins when the high-side FET (HS) turns on. This occurs when the output voltage (or any derivatives of it) falls to the level of V_{REF} of the regulation comparator. Q = 1, hence $\overline{Q}$ = 0 when the high-side FET is on, which makes QN off and allows C_{TON} to get charged by I_T until it reaches the V_{TH} threshold level. Consequently, the T_{ON} generator's output remains low, maintaining the SR latch in a high-state where Q = 1 and HS is turned on (with $\overline{Q}$ = 0, indicating the low-side FET (LS) is off). The on-state of HS increases the inductor current (I_L) and output voltage (V_{OUT}), persisting until the fixed on-time expires.

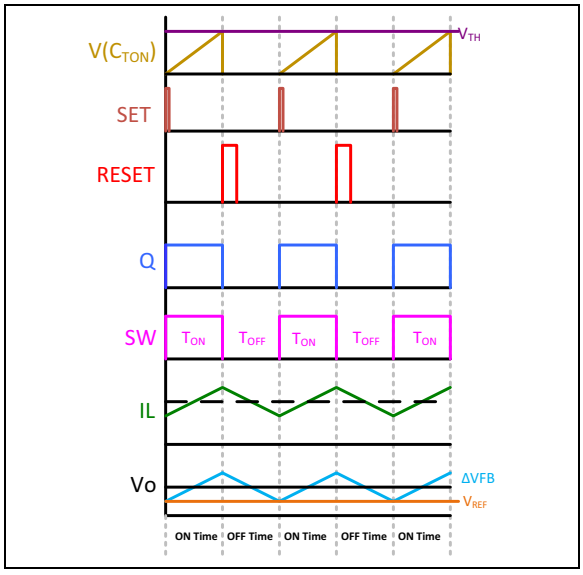


FIGURE 4: *Timing Diagram of the COT Control Scheme.*

OFF Time: The OFF time begins when the fixed on-time expires. Once C_{TON} charges to V_{TH}, the T_{ON} generator's output becomes high, triggering a reset signal to the SR latch. This transition sets Q = 0 and $\overline{Q}$ = 1. Consequently, HS is turned off and LS is turned on, causing the inductor current and output voltage to ramp down. Additionally, with $\overline{Q}$ = 1, the C_{TON} discharge FET (QN) is activated, discharging C_{TON} to prepare it for the next charging cycle. The OFF time continues until the output voltage (or any derivatives of it) drops to the level of V_{REF} (the threshold set at the noninverting terminal of the regulation comparator).

The minimum T_{OFF} block is introduced to ensure that the bootstrap capacitor (not shown in the block diagram) has sufficient time to charge, especially during scenarios involving very high duty cycle operation. Bootstrap capacitors are crucial for the proper turn-on of the high-side FET and are charged (mostly from VDD or an auxiliary regulated power rail of the converter IC) only during the low-side FET's on-time (T_{OFF}).

Maintaining a significant ripple (typically between 20 - 200 mV) at the feedback is crucial for the effective operation of COT control. However, relying solely on output capacitor ripple proves impractical in many cases. Hence, a key objective of this application note is to thoroughly explore various techniques for introducing ripple into the feedback loop.

While COT control boasts simplicity, robustness, and fast response, frequency variation can be substantial in response to changes in input voltage and, to a lesser degree, load. Furthermore, COT may exhibit relatively poor line regulation because it senses the valley of the ripple for regulation purposes and the amplitude of the ripple is highly dependent on the input voltage. These two drawbacks are highlighted in Figure 5.

This is where Microchip's Adaptive Constant-On-Time (ACOT) control emerges as a solution, effectively mitigating the challenges associated with frequency deviations and inadequate voltage regulation encountered with the conventional COT control method.

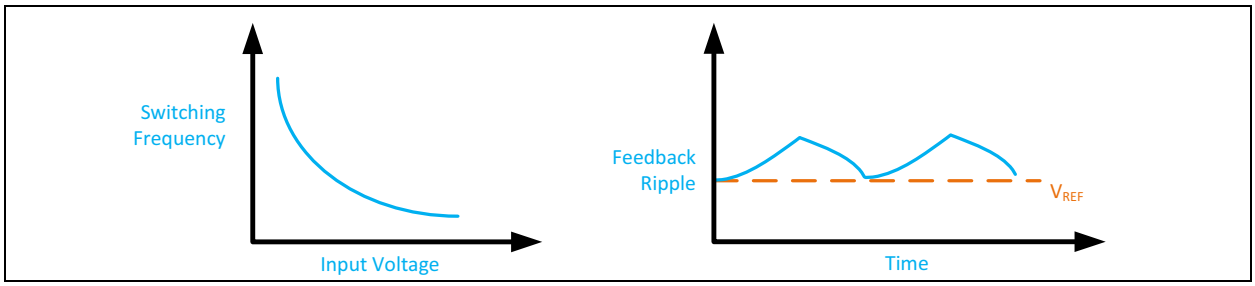


FIGURE 5: *Drawbacks of Basic COT Control Scheme.*

2.0 ADAPTIVE CONSTANT-ON-TIME (ACOT) CONTROL

Microchip's Adaptive Constant-On-Time (ACOT) control represents an improved version of the traditional COT method, addressing two key aspects. Firstly, ACOT employs improvements in the T_{ON} generator to emulate a fixed-frequency converter. Secondly, enhancements in the regulation comparator section improve line and load regulation.

2.1 Advancements in T_{ON} Generator

In ACOT, as illustrated in Figure 6, the T_{ON} generator incorporates additional feedback from both the input voltage and the switching (SW) node voltage. Specifically, the constant current source becomes a function of the input voltage ($I_T = K1 \bullet V_{IN}$, where K1 = constant) and the threshold of the T_{ON} generator comparator becomes a function of the output voltage ($V_{TH} = K2 \bullet V_O$, where K2 = constant). These enhancements enable ACOT to function similarly to a constant-frequency converter and alleviate frequency variation issues.

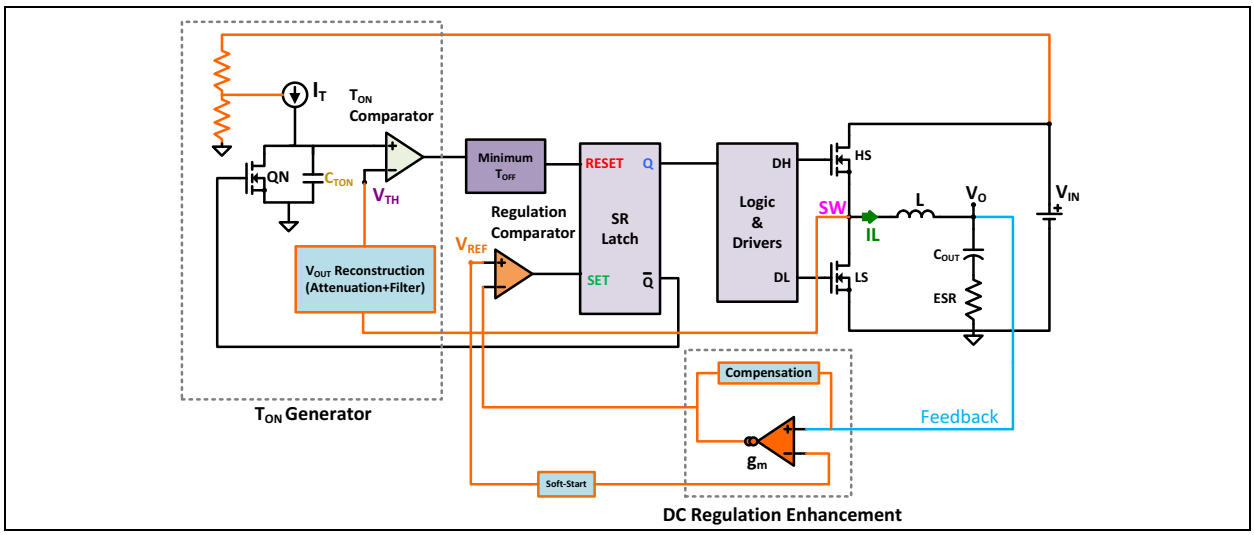


FIGURE 6: *Block Diagram of Adaptive-COT Control Scheme.*

For a basic COT, T_{ON} (On time) can be expressed as:

EQUATION 1:

$$T_{ON} = \frac{V_{TH} \bullet C_{TON}}{I_T}$$

When it comes to ACOT, substituting $V_{TH} = K1 \bullet V_O$ and $I_T = K2 \bullet V_{IN}$ into Equation 1, it results the following:

EQUATION 2:

$$T_{ON} = \frac{(K1 \bullet V_O) \bullet C_{TON}}{K2 \bullet V_{IN}} = \frac{K \bullet V_O \bullet C_{TON}}{V_{IN}}$$

Where:

K = K1/K2

Additionally, for a buck converter, it is known that (T_{SW} = Switching period):

EQUATION 3:

$$T_{ON} = \frac{V_O}{V_{IN}} \bullet T_{SW}$$

Combining Equations 2 and 3, results in:

EQUATION 4:

$$\frac{V_O}{V_{IN}} \bullet T_{SW} = \frac{V_O}{V_{IN}} \bullet C_{TON} \bullet K$$

Hence:

EQUATION 5:

$$T_{SW} = C_{TON} \bullet K$$

This derivation signifies that ACOT maintains a constant frequency (theoretically, in steady state condition) regardless of input or output voltage variations, as the switching period is solely dependent on the T_{ON} generator capacitor and a few constants. However, a slight frequency variation is to be expected due to many factors, such as T_{ON} generator component tolerances, duty cycle variations due to power stage losses, line transients, load transients, etc.

2.2 DC Regulation Enhancements

Basic COT control regulates the valley of the feedback ripple, which leads to poor line regulation due to the dependency of the feedback ripple amplitude on the input voltage. The deviation of the average feedback voltage in response to input voltage variations is illustrated in Figure 7. V_{FB1}(avg) represents the average feedback voltage for a lower input voltage, while V_{FB2}(avg) represents the average feedback voltage for a higher input voltage.

Microchip has incorporated special blocks in ACOT to directly regulate the average feedback voltage instead of regulating the valley of the feedback ripple. The DC regulation enhancement block is a significant addition to Microchip's ACOT control, effectively eliminating the inherent line regulation issues of basic COT control.

Figure 8 illustrates the interaction of the DC regulation enhancement block and main regulation comparator with waveforms (before and after the DC regulation enhancement block).

The DC regulation enhancement block consists mainly of an operational transconductance amplifier (g_m) and a discrete compensation circuit. Its key functions include forwarding all the AC ripple and providing gain for the DC component. As shown in Figures 6 and 8, the DC regulation enhancement block is placed prior to regulation comparator in the feedback network. This arrangement ensures that the output voltage is regulated to the average of the feedback ripple, thereby improving DC regulation in ACOT.

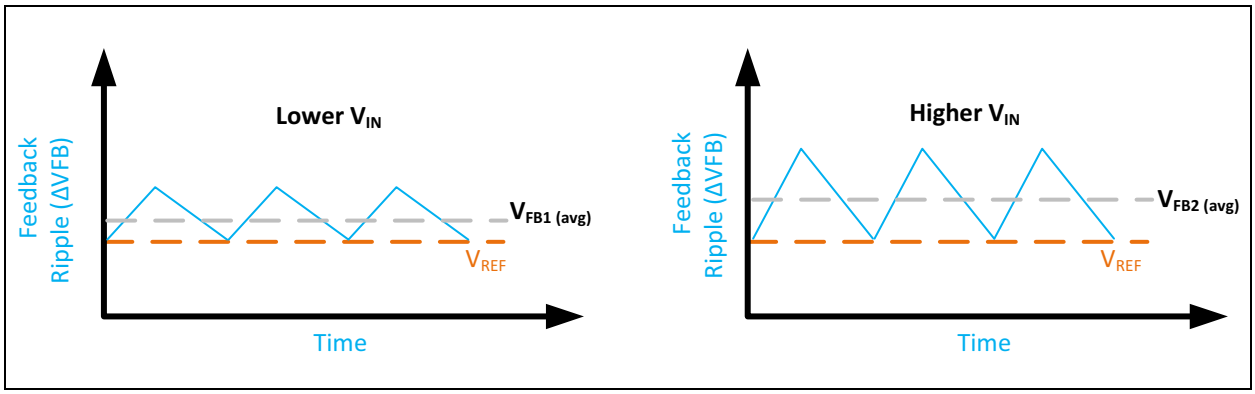


FIGURE 7: *Poor Line Regulation in Basic COT Control.*

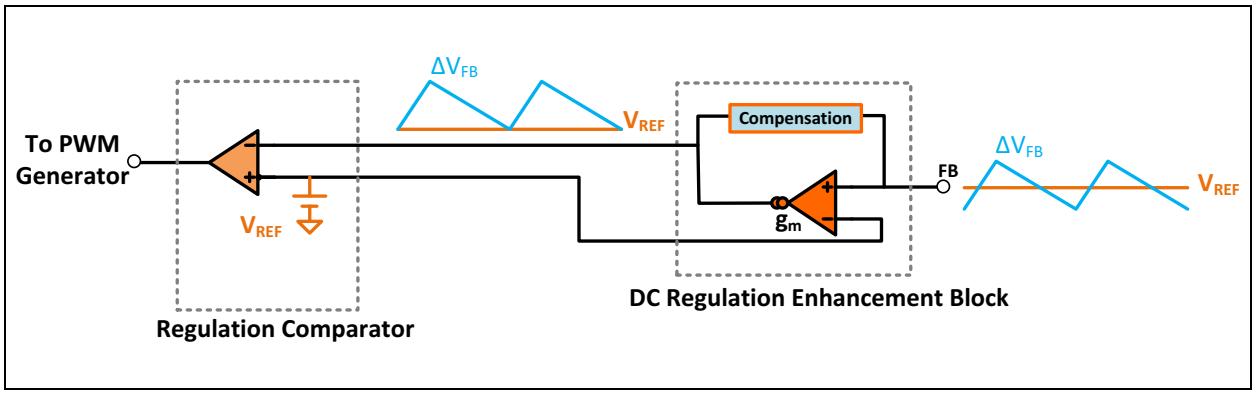


FIGURE 8: *DC Regulation Enhancement in ACOT Control.*

3.0 STABILIZING THE CONTROL LOOP USING OUTPUT RIPPLE (TYPE 1)

In COT or ACOT, the presence of ripple in the feedback signal is crucial for ensuring the proper operation and regulation of the power converter. This ripple enables the control circuitry to adjust the duty cycle of the power switch, facilitating precise regulation. In simpler terms, COT, ACOT, or any other form of hysteretic control relies on the ripple in the feedback as the ramp signal to the comparator for PWM generation.

In a buck converter, the output ripple primarily arises from two main factors: the output capacitance and its Equivalent Series Resistance (ESR). The output capacitance serves to store and release energy during the switching cycle, helping to smooth variations in the output voltage. However, due to the finite charging and discharging times of the output capacitor, small fluctuations in output voltage occur, resulting in ripple. Typically, this ripple amplitude (depicted as ΔVo_Cout in Figure 9) is minimal and is out of phase with inductor current, making it unsuitable for feedback control purposes. ΔVo_Cout can be calculated using Equation 6.

EQUATION 6:

$$\Delta Vo\_Cout = \frac{\Delta I_L}{8 \bullet F_{SW} \bullet Cout}$$

Where:

- F_{SW} = Switching Frequency
- $Cout$ = Output Capacitance
- ΔI_L = Inductor Ripple Current

However, the ESR of the output capacitor introduces further voltage fluctuations (depicted as ΔVo_ESR in Figure 9) due to the inductor current ripple. If the ESR is high enough, it can naturally provide a significant amount of ripple at the output which is also in phase with inductor current. Note that the parasitic inductance ripple in discussion was ignored, assuming that the layout is good and capacitor Equivalent Series Inductance (ESL) is not abnormally high.

For ease of reference, we have assigned type numbers to different control loop designs. This method, where the output ripple is used for the feedback ripple, is designated as **type 1**.

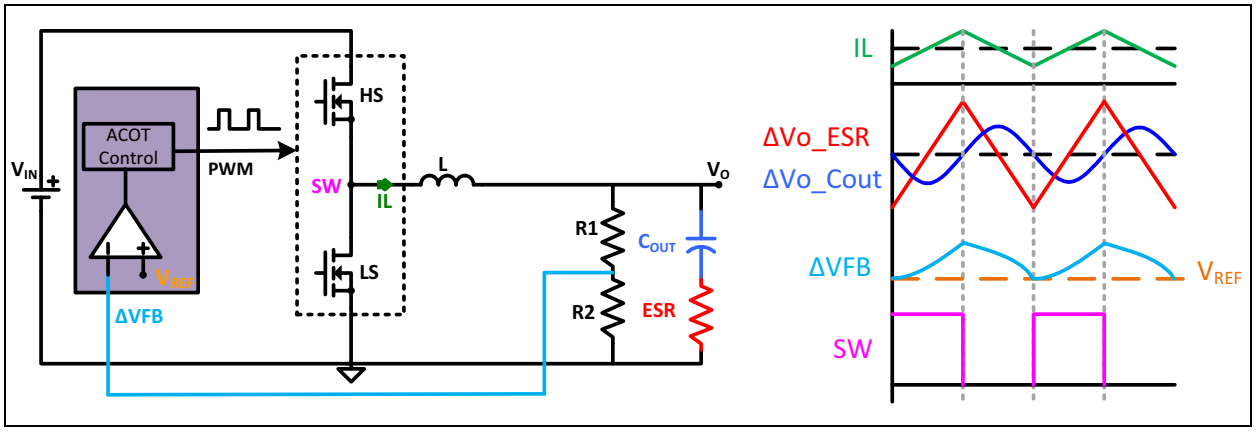


FIGURE 9: *Capacitive Ripple (ΔVo_Cout) and ESR Ripple (ΔVo_ESR) in Output Capacitor.*

Multi-layer ceramic capacitors (MLCC), aluminum electrolytic, tantalum, and polymer capacitors are commonly used in DC/DC switching regulator circuits. A quick comparison can be seen in Table 1. Electrolytic capacitors, in particular, have higher ESR values, contributing to a larger output ripple. **Thus, if an application can tolerate a substantial amount of ripple at the output, simply using a high ESR capacitor may suffice for stable operation of a COT or ACOT converter.**

TABLE 1: COMPARISON OF CAPACITOR TECHNOLOGIES

Technology	ESR	ESL	Voltage Stability	Temperature Stability	Capacitance/Unit Volume
Aluminum Electrolytic	Highest	Highest	Good	Lowest	High
Tantalum	Medium	Medium	Best	Good	High
Polymer Solid	Low	Low	Best	Good	High
Multilayer Ceramic	Lowest	Lowest	Poor	Good	Medium

Equation 7 explains how to calculate the required ESR for a given inductor ripple current (ΔI_L), reference voltage (V_{REF}), output voltage (V_O), and feedback ripple voltage (ΔVFB).

EQUATION 7:

$$ESR = \frac{\Delta VFB \bullet V_O}{\Delta I_L \bullet V_{REF}}$$

3.1 Abnormal Switching Behavior and Critical ESR

Figures 10 and 11 depict the steady-state waveforms of inductor current (I_L), capacitive ripple voltage (ΔVo_Cout), ESR ripple (Vo_ESR), feedback ripple voltage, and the switching node. These figures illustrate cases with larger and smaller ESR values, respectively. In Figure 10, the ESR ripple dominates the capacitive ripple and the converter operates normally. However, when the ESR ripple is insufficient to dominate the capacitive ripple, as shown in Figure 11, erratic switching behavior occurs. In this scenario, the high side FET is immediately turned back on after minimum OFF time, resulting in double pulsing and significant fluctuations in inductor current and output voltage.

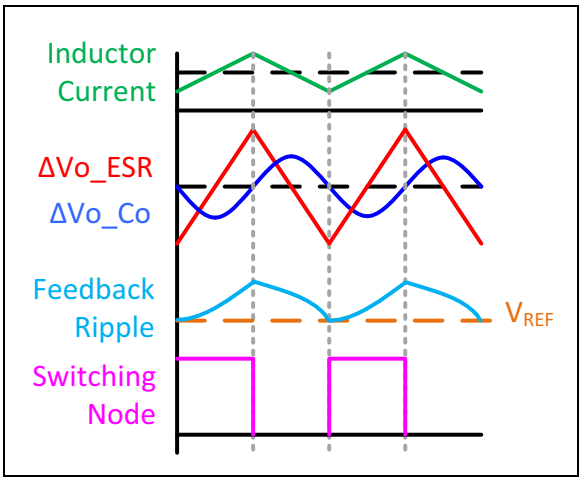


FIGURE 10: *Feedback Ripple in Phase with I_L.*

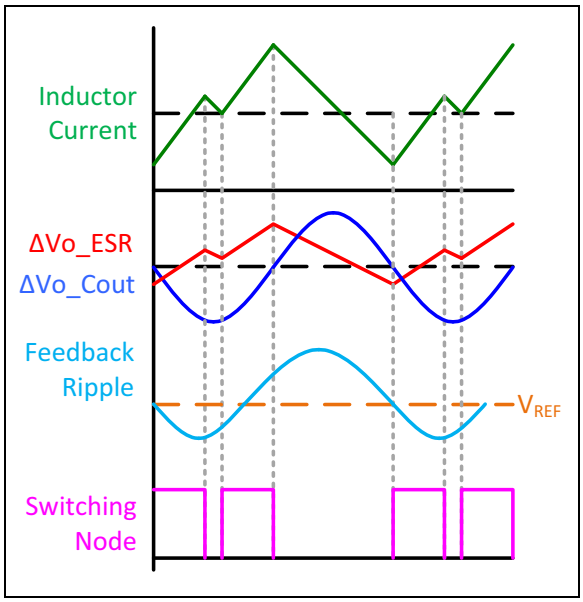


FIGURE 11: *Feedback Ripple out of Phase with I_L.*

As shown in Figure 10, during the HS FET ON time if the positive slope of ΔVo_ESR is greater than or equal to the negative slope of ΔVo_Cout, the output voltage (Vo) will consistently remain higher than the reference voltage (V_{REF}). This condition ensures normal operation. Conversely, Figure 11 shows the situation where the ESR ripple slope is less than the capacitive ripple slope during the HS FET ON time, resulting in abnormal switching. We could call the ESR value when both slopes match as the **critical ESR,** because below the critical ESR value, the abnormal switching begins. To derive the equation for the critical ESR value, we can follow the steps outlined below.

When the high side FET is ON, the slope of Vo_ESR can be expressed as shown in Equation 8.

EQUATION 8:

$$\frac{\Delta Vo\_ESR}{\Delta t} = ESR \bullet \frac{\Delta I_L}{\Delta t} = ESR \bullet \frac{V_{IN} - V_O}{L}$$

The slope of ΔVo_Cout can be calculated as shown in Equation 9.

EQUATION 9:

$$\frac{\Delta Vo\_Cout}{\Delta t} = \frac{\Delta I_L}{2} \bullet \frac{1}{Cout} = \frac{V_{IN} - V_O}{2 \bullet L \bullet Cout} \bullet T_{ON}$$

Combine Equations 8 and 9 to get the critical value of ESR:

EQUATION 10:

$$ESR = \frac{T_{ON}}{2Cout}$$

In other words, the stability criteria when the ESR ripple is sufficient for the feedback ripple (Type 1) can be expressed as:

EQUATION 11:

$$ESR \bullet Cout > T_{ON}/2$$

One crucial takeaway from this discussion is that, if the feedback ripple deviates from being in phase with the inductor current or falls outside of the recommended amplitude range, it can lead to **abnormal switching behavior**, laying the groundwork for potential failure. **This is true regardless of the source of feedback ripple**.

The Type 1 method is the simplest control loop scheme for ACOT, as it does not require any additional components beyond the parasitic components. However, it has the drawback of needing a substantial amount of output ripple, which also needs to be in phase with the inductor current, requiring a large output capacitor ESR. Since a large output ripple is undesirable in many applications, the following sections present other control loop types that reduce dependence on the output ripple.

4.0 RIPPLE INJECTION CIRCUIT DESIGN

For Microchip ACOT buck converter devices, it is advisable to maintain a ripple ramp at the feedback with a peak-to-peak amplitude within the range of **20 - 200 mV** (or as specified in the device data sheet), and the ripple waveform should be in phase with the inductor current. Throughout this application note, this peak-to-peak amplitude will be denoted as **ΔVFB**. Given the significance of this ripple, various possibilities to ensure adequate ripple in the feedback will be examined. While some situations may naturally provide sufficient ripple without the need for additional components, there is a high likelihood that extra ripple will need to be introduced with the assistance of additional components when output capacitors with very low ESR are used. This process is termed **"Ripple Injection"** as it involves introducing ripple when an adequate amount is not naturally present in the feedback signal.

4.1 Using a Feed-Forward Capacitor (Type 2)

Large output voltage ripple is undesirable for most applications, as modern systems demand a clean output from the power supply. A common approach to reducing ripple is to select a low ESR output capacitor. However, when the output ripple amplitude decreases due to low ESR, relying solely on the ESR ripple method can become problematic. In such cases, where medium output ripple is present (more than 20 - 40 mV or the minimum limit specified in the device data sheet), introducing a feed-forward capacitor (CFF) can be beneficial. The CFF is placed in parallel with the top feedback resistor (as illustrated in Figure 12) and can effectively enhance the feedback output ripple. As illustrated in Figure 13 (AC gain without CFF) and Figure 14 (AC gain and phase boost with CFF), the feed-forward capacitor directs high-frequency ripple to the FB pin, ensuring a phase boost around the middle of the relevant bandwidth. This method effectively manages feedback ripple if enough output ripple is present.

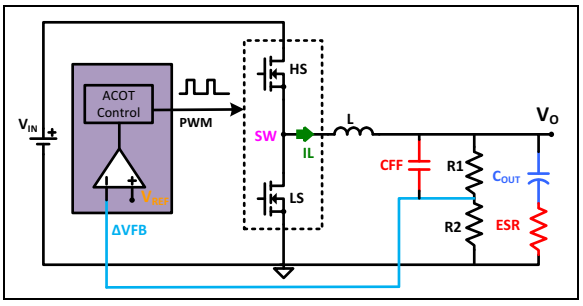


FIGURE 12: *Feed-Forward Capacitor (CFF) Placement.*

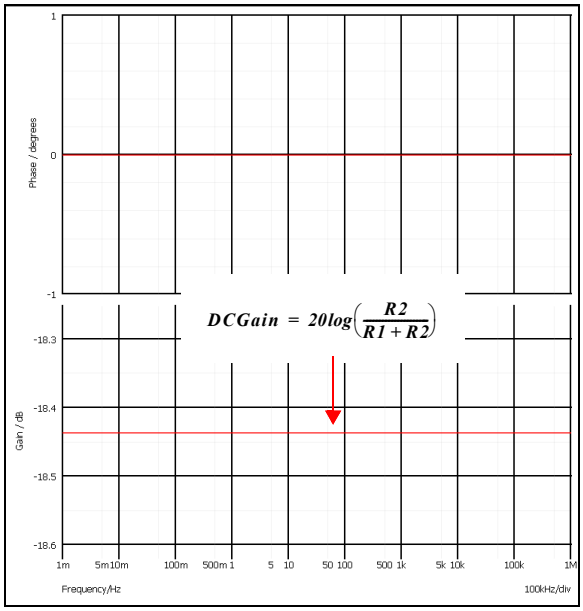


FIGURE 13: *Feedback Gain without CFF.*

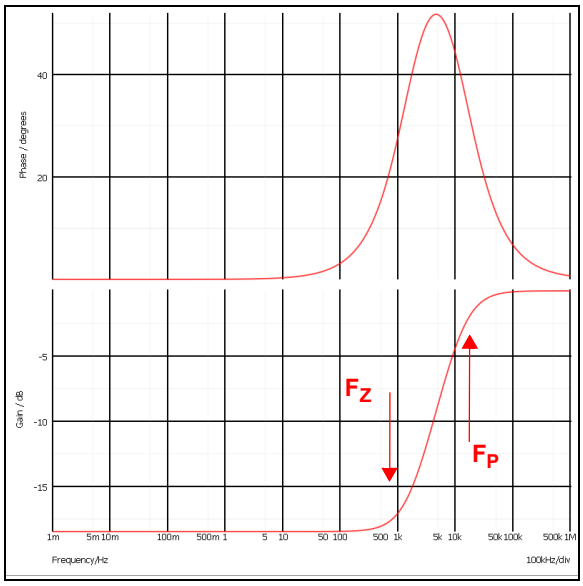


FIGURE 14: *Gain and Phase Boost with CFF.*

CFF introduces a gain boost after its zero frequency (F_Z) and a phase boost is at a maximum between the zero and pole frequencies (F_P). F_P and F_Z can be calculated using Equations 12 and 13. Increasing the value of CFF shifts the zero and pole to lower frequencies, and decreasing the value CFF shifts the zero and pole to higher frequencies. The gain at DC is set by R1 and R2.

EQUATION 12:

$$F_Z = \frac{1}{2\pi \bullet R1 \bullet CFF}$$

EQUATION 13:

$$F_P = \frac{1}{2\pi \bullet CFF}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

A typical choice for CFF is between 1 nF to 100 nF (10 nF is a good starting point), if R1 and R2 are in the kΩ range. The impedance of CFF at the switching frequency should be much lower than R1 and R2, hence the minimum value of CFF can be calculated using Equation 14 (considering the impedance of CFF to be at least an order of magnitude lower than the impedance of R1 in parallel with R2).

EQUATION 14:

$$CFF(min) \geq \left(\frac{10}{2\pi \bullet F_{SW} \bullet \left(\frac{R1 \bullet R2}{R1 + R2}\right)}\right)$$

4.2 Using R-C from SW Node and Feed-Forward Capacitor (Type 3)

In numerous applications, there is a prevalent demand for power supplies to deliver output with exceedingly low ripple. This requirement is important, especially as many modern applications cannot tolerate more than a 1% ripple-to-output voltage ratio, and output voltages may be less than 1V. To achieve such stringent ripple requirements, the widespread adoption of very low ESR capacitors, such as ceramic caps, has become commonplace. These capacitors effectively minimize ripple, ensuring that power supplies meet the stringent performance criteria demanded by modern applications.

In scenarios where the output ripple is less than 20 - 40 mV (or the minimum limit specified in the data sheet) an alternative ripple injection approach should be employed. A simple and proven method involves deriving ripple from the switched node by utilizing an R-C between the switched node and feedback input, alongside a feed-forward capacitor across the top feedback resistor. The configuration of ripple injection components (Ri, CB, and CFF) is illustrated in Figure 15. The current passing through Ri is nearly a square wave with no DC component, as blocked by CB. This current is then integrated across capacitor CFF to generate a triangular waveform. However, caution must be exercised because CFF also directs the entire “out-of-phase” output ripple to the feedback pin. **Therefore, the self-injected “in-phase” ripple must be sufficiently large to overcome the capacitive component of the output ripple.**

In Figure 16, the circuit scenarios are examined individually. Firstly, when the switching node (SW) voltage is present, the circuit can be redrawn with the output connected to ground. The voltage at FB in this situation is noted as VFB1. Secondly, when the switching node voltage is zero, the impact of Ri and CB can be eliminated and consider only CFF, denoting feedback voltage in this situation as VFB2. By applying the superposition theorem, a vector diagram can be drawn, as depicted in Figure 15, with the X-axis representing the inductor current, the positive Y-axis representing the inductor voltage, and the negative Y-axis (90 degrees out of phase with the inductor current) representing the capacitor voltage. VFB1 leads the inductor current, while VFB2 lags it. However, VFB, which is the vector sum of VFB1 and VFB2, is almost in phase with the inductor current in the presented scenario. This alignment is a fundamental and critical attribute of good feedback ripple.

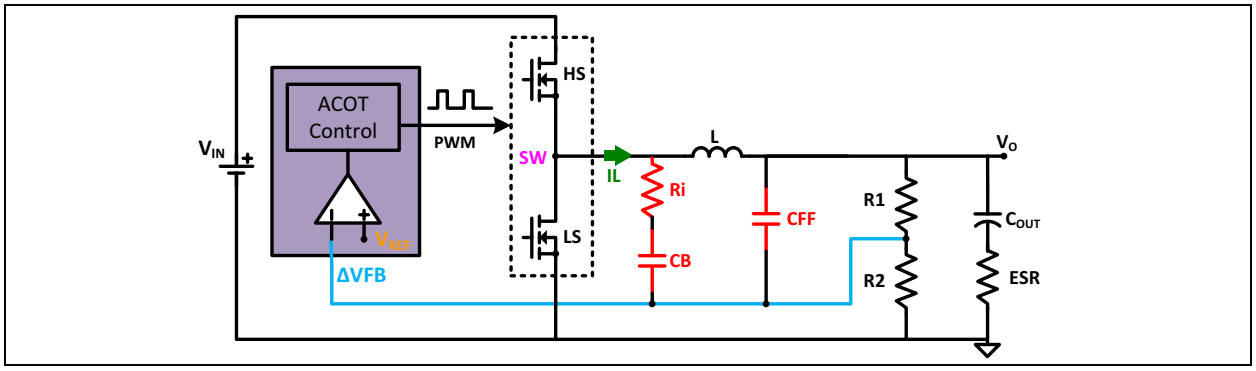


FIGURE 15: *Ripple Injection from Switched Node.*

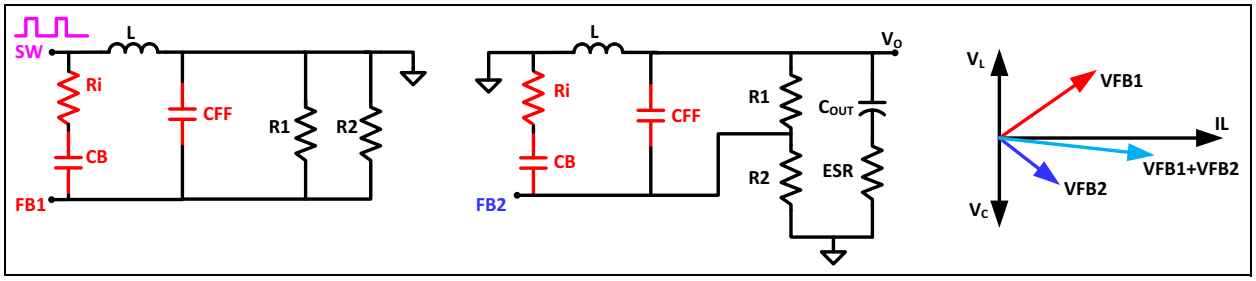


FIGURE 16: *Ripple Injection Equivalent Schematics when SW and Output Voltages are Considered Separately.*

FEEDBACK RIPPLE CALCULATION IN TYPE 3 RIPPLE INJECTION

It is beneficial to derive the formula to calculate the ripple voltage expected at the feedback pin using the type 3 ripple injection circuit. As illustrated in Figure 17, no net DC current can flow through Ri in steady state because CB can be considered as a DC blocking capacitor. Therefore, the DC (average) values at node SW and at **node X** must be equal, and the DC (average) value of node SW is $D \times V_{IN} = V_O$ (assuming a lossless inductor).

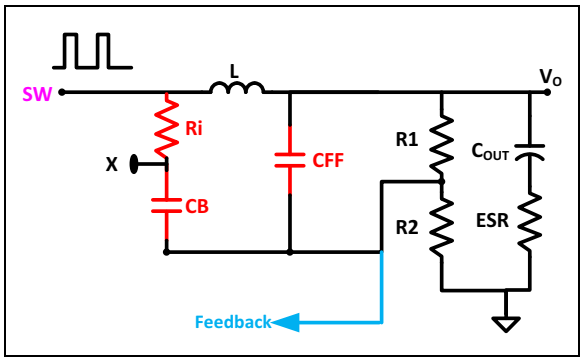


FIGURE 17: *Equivalent Circuit of Ripple Injection from SW.*

When the SW voltage is equal to V_{IN}, the current injected in the feed-forward capacitor (CFF) is calculated by Equation 15 (neglecting the small amount of current flowing through R1 and R2).

EQUATION 15:

$$I_{CFF} = \frac{(V_{IN} - V_O)}{Ri}$$

It is worth noting that the assumptions made here are CB >> CFF (so that CB bypasses all the high frequency AC component) and the impedance of CFF is much less than R1 and R2 (so that we can neglect the current through R1 and R2). These two assumptions are important stability criteria for type 3 ripple injection design.

An equation can be derived for the feedback ripple for the type 3 ripple injection circuit. For a capacitor:

EQUATION 16:

$$\Delta V = \frac{I \bullet \Delta T}{C}$$

Combining Equations 15 and 16, the peak-to-peak ripple injected to the feedback pin across CFF can be calculated using Equation 17.

EQUATION 17:

$$\Delta VFB = \frac{(V_{IN} - V_O) \bullet T_{ON}}{Ri \bullet CFF}$$

This can be rewritten as:

EQUATION 18:

$$\Delta VFB = \frac{V_{IN} \bullet D \bullet (1 - D)}{Ri \bullet CFF \bullet F_{SW}}$$

Sizing the ripple injection components is a crucial step in designing a COT/ACOT control loop. The voltage ripple at the feedback pin due to the ripple injection circuit (Ri, CB, and CFF) can be estimated using Equation 18.

While it may appear to be a straightforward calculation, when reactive components are introduced into the design, certain conditions must be satisfied to ensure proper operation. First, the DC blocking capacitor should have a much higher value than the feed-forward capacitor (Equation 19). Note that an excessively high value of CB can slow down the control loop response, while an excessively low value can cause instability. A good rule of thumb is to set CB to 5-10 times the value of CFF. Second, the impedance of CFF should be significantly lower than that of the feedback resistor dividers, R1 and R2 (Equation 20). Additionally, the time constant of the feedback network should be notably higher than the switching period (Equation 21). Furthermore, the crossover frequency can be estimated using Equation 22, and it needs to be at least 5 times lower than the switching frequency, as depicted in Equation 23. These equations and conditions serve as **stability criteria for the type 3 ripple injection design**.

EQUATION 19:

$$CB \gg CFF$$

EQUATION 20:

$$Impedance\ of\ CFF\ at\ F_{SW} \ll \frac{R1 \bullet R2}{R1 + R2}$$

EQUATION 21:

$$(Ri \,/\!/\, R1 \,/\!/\, R2) \bullet CFF \gg T_{SW}$$

EQUATION 22:

$$Fcrossover(est) = \frac{Ri \bullet CFF}{2\pi \bullet L \bullet Cout}$$

EQUATION 23:

$$Fcrossover(est) < \frac{F_{SW}}{5}$$

4.3 Ripple Injection from Dedicated Pin (Type 4)

The type 3 ripple injection scheme is highly favored for its independence from output ripple, offering greater flexibility in adjusting converter performance compared to the type 1 and type 2 schemes. However, as demonstrated by Equation 18, type 3 ripple injection heavily relies on the input voltage and duty cycle, as the ripple originates from the SW node.

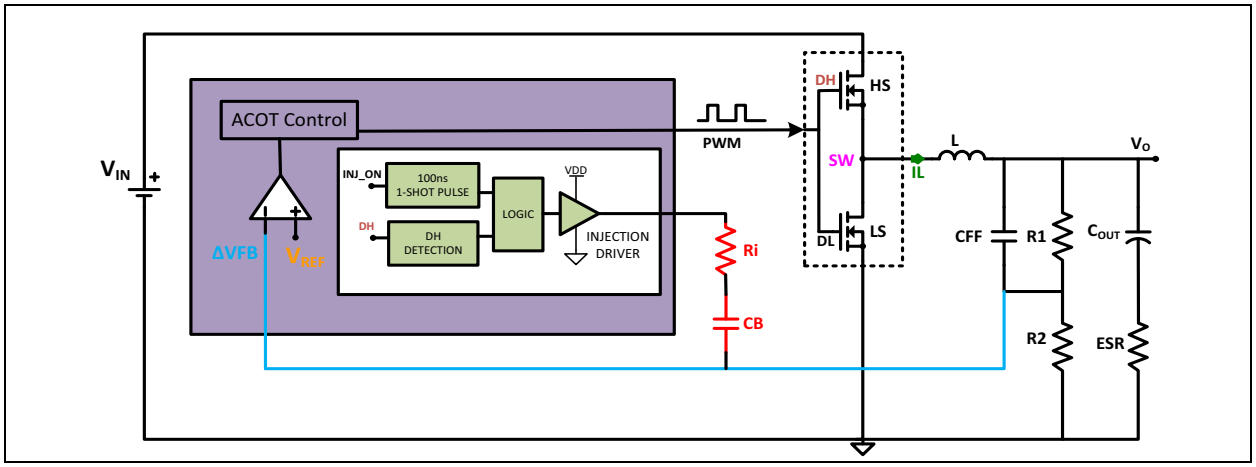


FIGURE 18: *Ripple Injection from the INJ Pin.*

To address this limitation, some devices from Microchip, such as MIC2129, feature a dedicated pin, typically labeled as “INJ”, through which an internally generated pulse is supplied. Connecting an R-C similar to type 3 from “INJ” pin to feedback along with a feed-forward capacitor will provide sufficient ripple to the feedback pin. As shown in Figure , the INJ node of the MIC2129 produces a pulse with 4.5V magnitude,100 ns ON time, at a frequency equal to the switching frequency and in-phase with the SW node as is triggered at DH ON event (high side FET drive output).

Similar to the type 3 scheme, it offers the advantage that the ripple amplitude remains unaffected by input voltage fluctuations, as the ramp is generated internally from a dedicated module which gets a regulated voltage supply. The voltage ripple at the feedback pin due to the ripple injection from INJ pin can be estimated using Equation 24:

EQUATION 24:

$$Ri \bullet CFF = \frac{4.5V \bullet 100\ ns}{\Delta VFB} \bullet \left(1 - \frac{100\ ns}{T_{SW}}\right)$$

The crossover frequency can be estimated using Equation 25:

EQUATION 25:

$$Fcrossover(est) = \frac{Ri \bullet CFF}{2\pi \bullet L \bullet Cout} \bullet \frac{V_O}{4.5V \bullet 100\ ns \bullet F_{SW}}$$

As discussed before, it is crucial to keep the crossover frequency below FSW/5 for stable operation. When employing a type 4 ripple injection scheme, additional device-specific precautions are necessary to ensure smooth operation during start-up and pre-bias. It is important to note that the specific magnitude (4.5V) and ON time (100 ns) mentioned here are device-specific (MIC2129) and may vary from one part to another. Given the device-dependent nature of type 4 ripple injection, this application note will not explore its complexities in details, and it is recommended to follow the guidelines provided in the data sheet for proper implementation.

5.0 STEP-BY-STEP GUIDE FOR RIPPLE INJECTION DESIGN

The primary goal of these design steps is to achieve a satisfactory ripple at the feedback in the control loop. Satisfactory ripple should meet the following criteria:

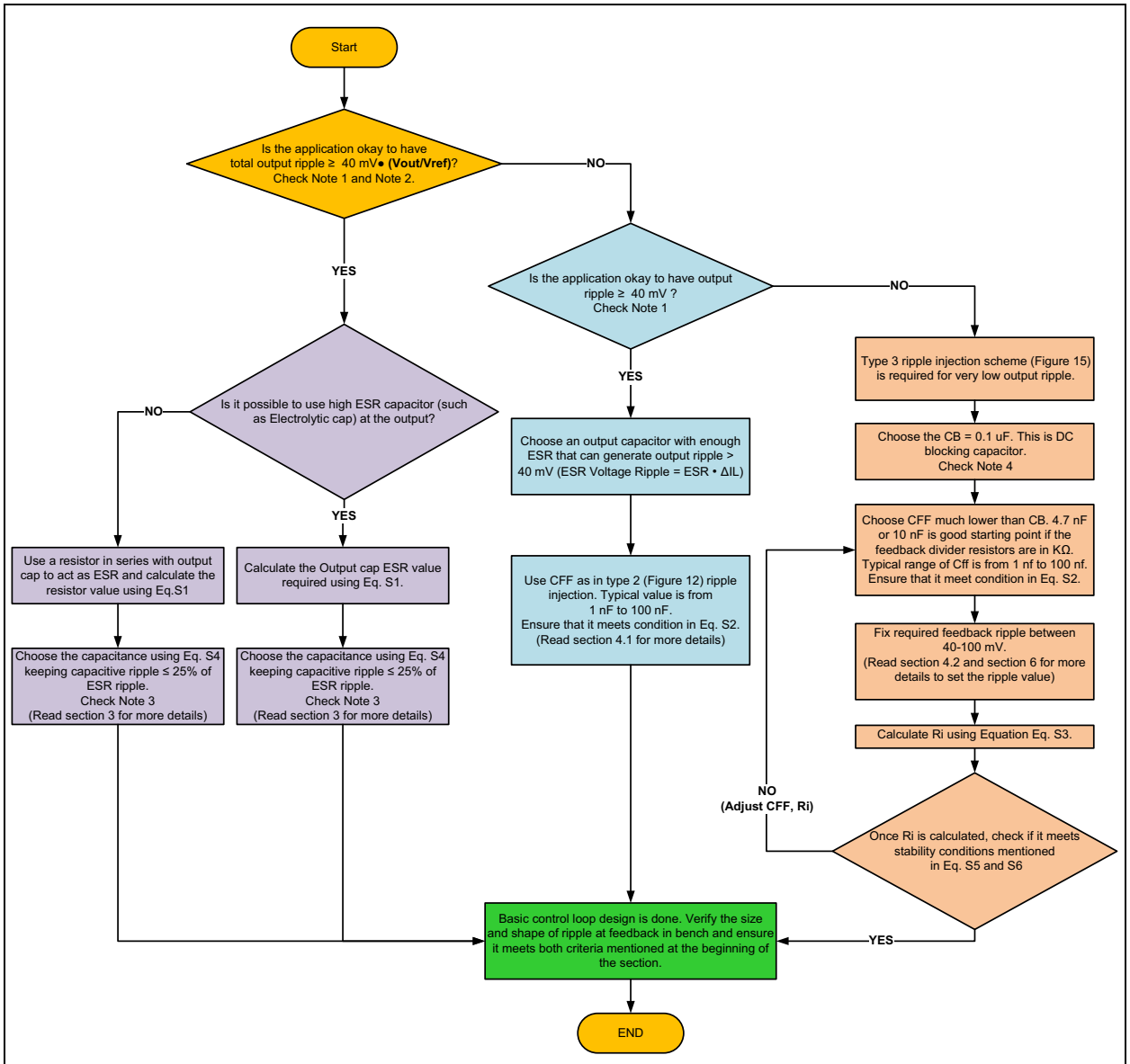
a) **The peak-to-peak ripple amplitude at the feedback pin (ΔVFB) should fall within the range of 20 - 200 mV (or as specified in data sheet).**
1. Why not less than 20 mV: Feedback ripple should be large enough to be sensed by the feedback loop devices internal in the device (typically a transconductance amplifier and error comparator). The lower limit is typically 20 mV, considering the typical noise floor in a buck converter, unless specified otherwise in the device data sheet. Variations in feedback ripple due to input voltage, switching frequency, and duty cycle should be considered during design (refer to Equation 18). Though the theoretical lower limit is 20 mV, a value of 40 mV was chosen to include additional margin for the practical design calculations.
2. Why not more than 200 mV: The maximum feedback ripple voltage is limited by the internal clamps of feedback loop components. If the feedback ripple exceeds a certain value determined by these internal clamps, the output voltage regulation deteriorates because only a fraction of the feedback information is sensed. The higher limit will be specified in the device data sheet.

b) **The ripple waveform should be in phase with the inductor current.**

TABLE 2: RIPPLE INJECTION EQUATIONS

S#	Equation	Equation Number
S1	$ESR = (\Delta VFB/\Delta IL) \bullet (V_O/V_{REF})$	Equation 7
S2	Impedance of CFF at F_{SW} << R1//R2	Equation 20
S3	$Ri = (V_{IN} \bullet D \bullet (1\text{-}D))/(\Delta VFB \bullet CFF \bullet F_{SW})$	Equation 18
S4	$Cout = \Delta IL/(8 \bullet F_{SW} \bullet \Delta Vo\_Cout)$	Equation 6
S5	$(Ri//R1//\ R2) \bullet CFF >> T_{SW}$	Equation 21
S6	$(Ri \bullet CFF)/(2\pi \bullet L \bullet Cout) < F_{SW}/5$	Equations 22, 23

The flowchart depicted in Figure 19 outlines the simplified step-by-step design guide for ripple injection circuit. The flowchart mentions Equations S1 to S6, which can be found in Table 2.



Note 1: 40 mV is considered to provide additional margin to theoretical limit of 20 mV (unless specified otherwise in the data sheet).

2: (V_O/V_{REF}) multiplication factor is to accommodate the attenuation of ripple by feedback resistor dividers.

3: The criteria of 25% is provided to ensure sufficient margin of ESR ripple over capacitive ripple.

4: An excessively high value of CB can slow down the control loop response, while an excessively low value can cause instability. A good rule of thumb is to set CB to 5-10 times the value of CFF. Value of CB can be fine tuned after calculating CFF or during the bench test.

FIGURE 19: *Step-by-Step Guide for Ripple Injection Design.*

6.0 OPTIMIZING RIPPLE INJECTION CIRCUIT DESIGN FOR TRANSIENT RESPONSE

Transient response holds immense significance across various applications, serving as a critical performance aspect in power converter design, by ensuring the converter's ability to swiftly adapt to dynamic load or input voltage changes. It also indicates the stability of the converter by reflecting its capability to maintain consistent performance despite external variations. It shows how fast the converter can settle to a new steady state following a disturbance, such as a load step change or input voltage fluctuation. A power converter with good transient performance can rapidly adjust its output voltage or current to minimize deviations and restore stability within a short time frame. This characteristic is crucial in various applications such as high-power density Point-of-Load (POL) conversion, power supplies for RF loads, telecom POLs, power supplies for FPGAs, processors, memories and various high-end digital systems.

6.1 Transient Response with ACOT Control

One of the biggest advantages of ACOT control is its superior load transient response compared to fixed frequency control (Current mode control or Voltage mode control). The following sections provide a closer look at the step-up and step-down load transient behaviors of each control mode.

Step-up Load Transient

As illustrated in Figure 20, ACOT applies only a minimum OFF time during load step-up transients, ensuring the high side power switch is turned on for a sufficient duration to accommodate the rapid increase in load without compromising stability. This also means ACOT increases the switching frequency during step-up load transients, enabling swift response to sudden load changes and maintaining optimal performance. Importantly, ACOT maintains a consistent pulse width during load transients, ensuring stable regulation without significant output voltage fluctuations. This could be explained by the response delay in ACOT, which is reduced to the minimum OFF time, ensuring rapid and precise adjustments to load variations for enhanced voltage regulation and system stability.

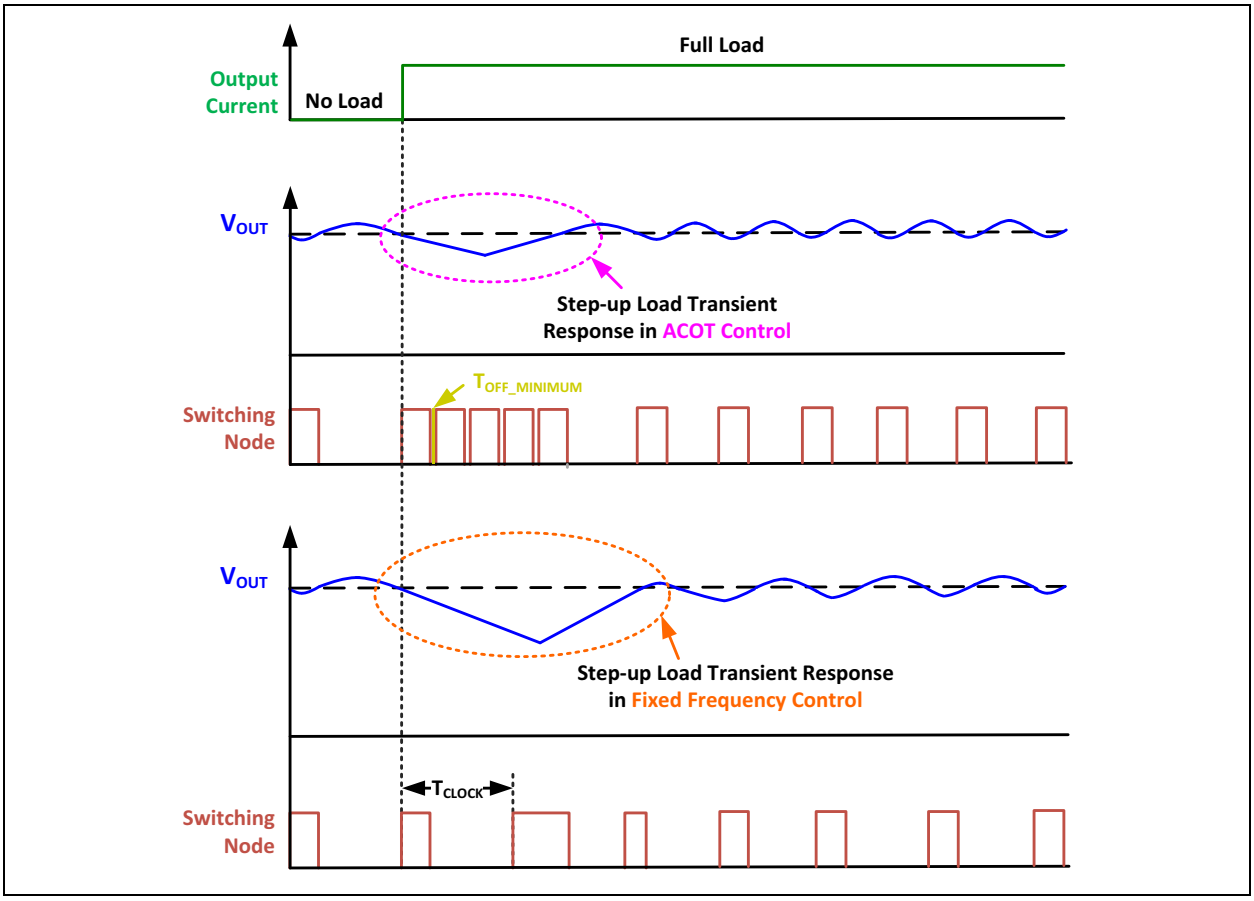


FIGURE 20: *ACOT Control and Fixed Frequency Control during Step-up Load Transient.*

Figure 20 also includes the behavior of fixed frequency control during step-up load transient for comparison. Unlike ACOT, fixed frequency control maintains a constant switching frequency during step-up load transient, which may limit its ability to promptly respond to sudden load variations, affecting transient performance. The delay associated with such control methods can be significant, as severe in the extreme as approaching the clock period (Tclock), compromising response time in dynamic operating conditions.

Step-down Load Transient

ACOT controllers dynamically reduce the switching frequency in response to a step-down load transient, effectively managing the overshoot in output voltage caused by the sudden reduction in load current. This approach leverages ACOT's faster loop response, resulting in minimal delay for output voltage correction. As shown in Figure 21, if the ACOT controller can operate at 0% duty cycle, it may skip switching cycles altogether to prevent excessive voltage overshoot. This capability allows ACOT controllers to react quickly and efficiently to load changes, maintaining output voltage stability.

In contrast, even though fixed-frequency controllers reduce the duty cycle during step-down transient, they still maintain a constant switching frequency which results in a longer correction time compared to ACOT. However, many modern controllers come with 0% duty cycle capability, allowing them to skip cycles during an output voltage overshoot and perform similarly to ACOT controllers during step-down load transients.

Numerous factors influence the transient response in a buck converter, including the design and performance of the control loop, switching frequency, output LC filter design, type of output capacitor, load step size, slew rate, and more. Given the focus on ACOT control, how ripple injection design can influence load transient performance will be examined, while keeping all other factors constant for analysis purposes.

As discussed in **Section 4.0**, there are primarily four types of ripple injection schemes, with RC ripple injection via the SW node (type 3) being a preferred choice among engineers, due to its ability to support the lowest output voltage ripple. Therefore, a deeper analysis of the type 3 ripple injection scheme can be conducted to explore various possibilities for optimizing the transient performance of the converter.

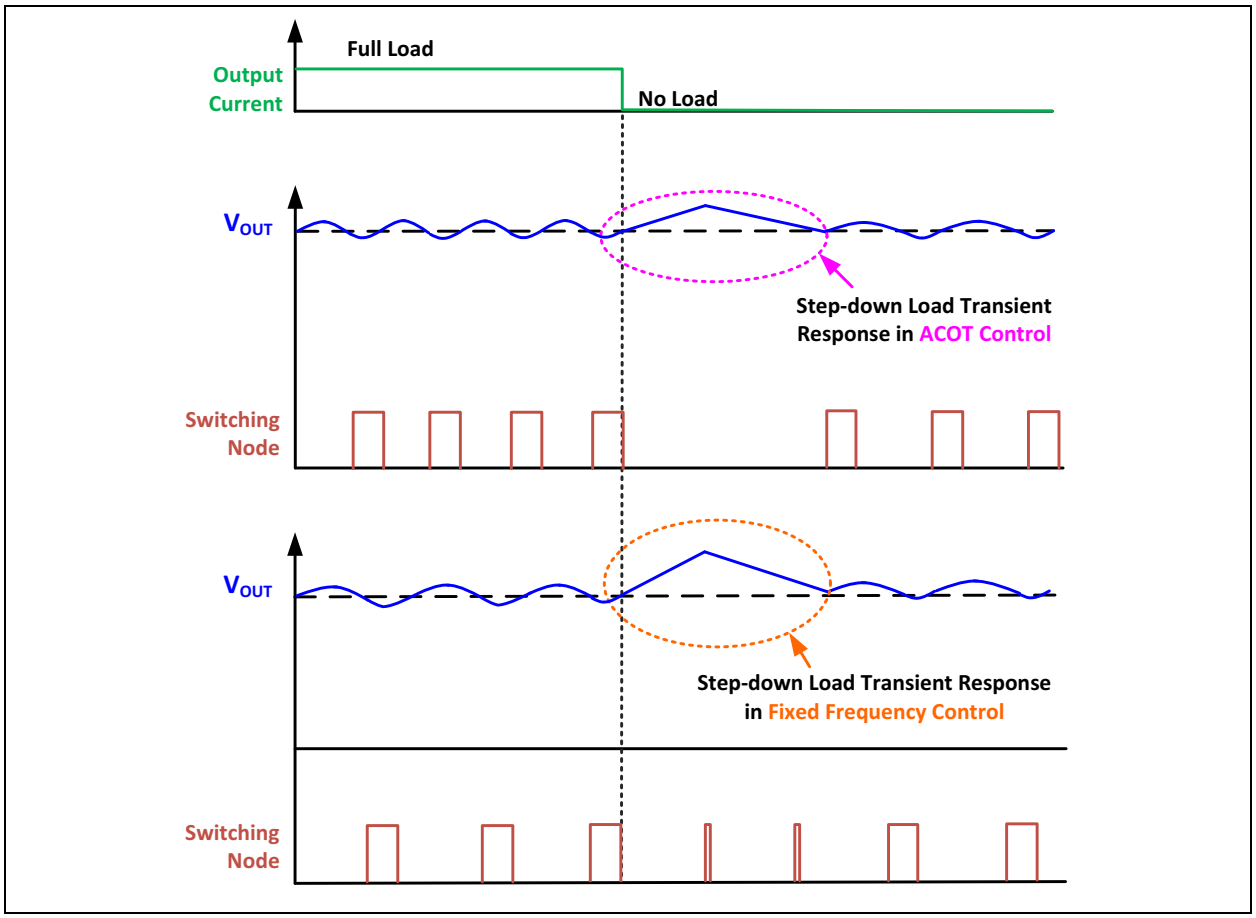
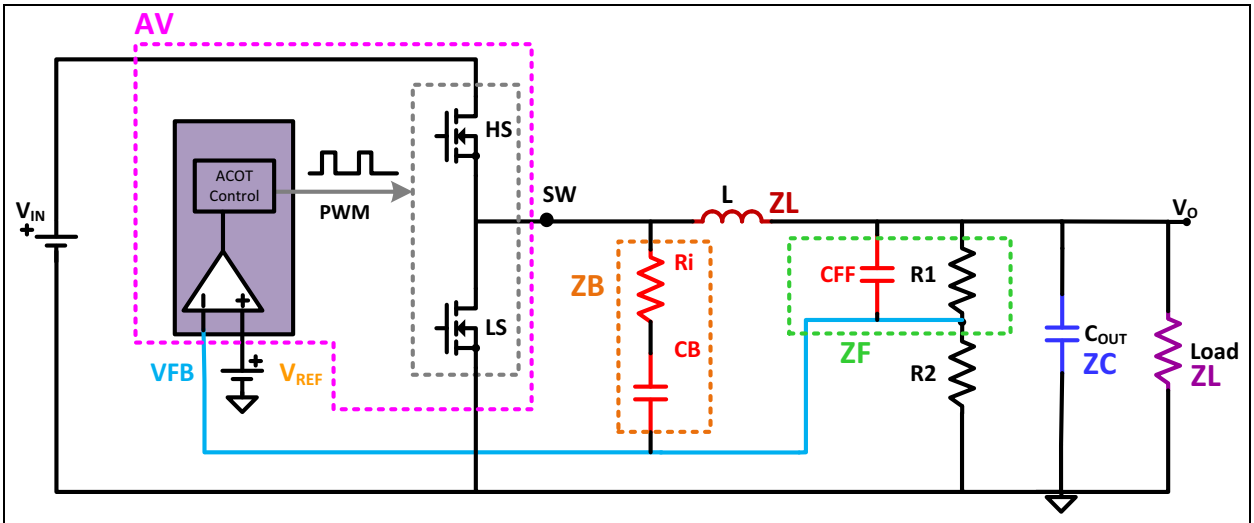


FIGURE 21: *ACOT Control and Fixed Frequency Control during Step-Down Load Transient.*

6.2 Control Loop Gain Analysis

Deeper analysis often requires circuit modeling, allowing us to gain deeper insights. However, conventional modeling methods are typically designed for converters operating at fixed frequencies. This poses a challenge for ripple-based variable frequency converters like COT or ACOT control, which dynamically adjust their frequency in response to load and input voltage variations. However, for analysis purpose, ACOT and ripple injection model can be developed with help of some practical assumptions. Please refer to Figure 22 and the following equations to explore the control loop modeling of ACOT.



ZL = Impedance of inductor

ZB = Impedance of RINJ and CINJ

ZF = Impedance of CFF and R1

ZC = Impedance of Output capacitor

ZLoad = Impedance of load

AV = Combined gain of Modulator and MOSFET power stage

Vsw = Voltage at SW (switching node), Fsw = Switching Frequency

VFB = Voltage at Feedback

Vo = Output voltage

V_{REF} = Reference to the error comparator

FIGURE 22: *Control Loop Modeling of ACOT.*

AV is defined as the combined gain of the modulator gain and MOSFET power stage gain for analysis purposes.

The feedback circuit gain can be expressed as:

EQUATION 26:

$$G_{FB} = -\frac{VFB}{V_O}$$

From Figure 22, the LC filter stage gain can be expressed as:

EQUATION 27:

$$G_{LC} = \frac{V_O}{V_{SW}} = \frac{ZC \,/\!/\, ZLOAD}{ZL + ZC \,/\!/\, ZLOAD}$$

From Equations 26, 27 and Figure 22, the Overall Loop gain (G) can be expressed as:

EQUATION 28:

$$G = G_{FB} \bullet AV \bullet G_{LC}$$

Equation 28 can be rewritten as:

EQUATION 29:

$$G = -\frac{VFB}{V_O} \bullet AV \bullet \frac{ZC \,/\!/\, ZLOAD}{ZL + ZC \,/\!/\, ZLOAD}$$

Next, the aim is to derive an expression for VFB/VO in relation to the impedances of the ripple injection circuit, allowing a correlation can be established between the ripple injection components and loop gain. The detailed mathematical derivation for VFB/Vo is provided in the Appendix. In summary, the Overall Loop gain (G) can be expressed as:

EQUATION 30:

$$G \cong -\frac{ZB}{ZF} \bullet \frac{ZC \,/\!/\, ZLOAD}{ZL \,/\!/\, ZLOAD + ZL}$$

As stated in Figure 22, ZB is the impedance of Ri and CB, which can be expressed as:

EQUATION 31:

$$ZB = Ri + \frac{1}{(2\pi \bullet F_{SW} \bullet CB)}$$

ZF is the impedance of R1 and CFF, which can be expressed as:

EQUATION 32:

$$ZF = \frac{R1}{1 + (2\pi \bullet F_{SW} \bullet R1 \bullet CFF)}$$

From Equation 30, it is evident that the **factor of ZB/ZF,** i.e., the ratio of the impedances of RC ripple injection and feed-forward circuits, plays a crucial role in enhancing the loop gain. From the basics of control theory, it is understood that higher loop gains improve overall regulation (both DC set point accuracy and transient performance).

Returning to the fundamental discussion on ripple injection, Equation 30 underlines the significance of the ZB/ZF ratio and the resulting peak-to-peak ripple amplitude at the feedback pin in defining key parameters, such as loop gain, crossover frequency, and transient response. It is established that maximizing ZB/ZF, indicating the use of the lowest peak-to-peak ripple at feedback, enhances transient response. However, it is essential to acknowledge the trade-off between achieving an acceptable ripple level (sufficiently large compared to noise and switching jitter) and minimizing ripple as much as possible. As a general guideline, maintaining a minimum peak-to-peak ripple amplitude at feedback (ΔVFB) above 20 mV is recommended, considering the typical noise levels in the switching converters and feedback pin sense range. However, it is best to check the minimum or maximum value from the device data sheet.

6.3 Feedback Ripple vs. Transient Response

Now, some design examples can be examined to validate the preceding analyses and explanations. This analysis aims to reveal the transient response performance concerning variations in feedback ripple amplitude (ΔVFB) so that the ripple injection components for the desired transient performance can be optimized.

Figure 23 illustrates the schematic diagram of an MIC28515 buck converter design with **V_{IN} = 48V**, **V_{OUT} = 5V**, **F_{SW} = 266 kHz**. Analysis will be performed with a **load transient from 2.5A to 5A** with a slew rate of 2.5A/3 µs. The details of the evaluation board used for testing can be found in the MIC28515 Evaluation Board User's Guide.

In the reference schematic (Figure 23), the ripple injection components employed are Ri = 16.2k, CB = 0.1 µF, and CFF = 4.7 nF. Utilizing Equation 18, ΔVFB can be calculated. The calculated value is 220 mV, which closely aligns with the test result (slight variations in the duty cycle compensate for losses, leading to slight deviations in the calculated value). Figure 24 depicts the transient response performance associated with the reference schematic (Figure 23), and Figures 25, 26 and 27 show the transient performance across different ΔVFB amplitudes achieved by adjusting the ripple injection components.

Figure 28 shows the abnormal switching when ΔVFB is too low.

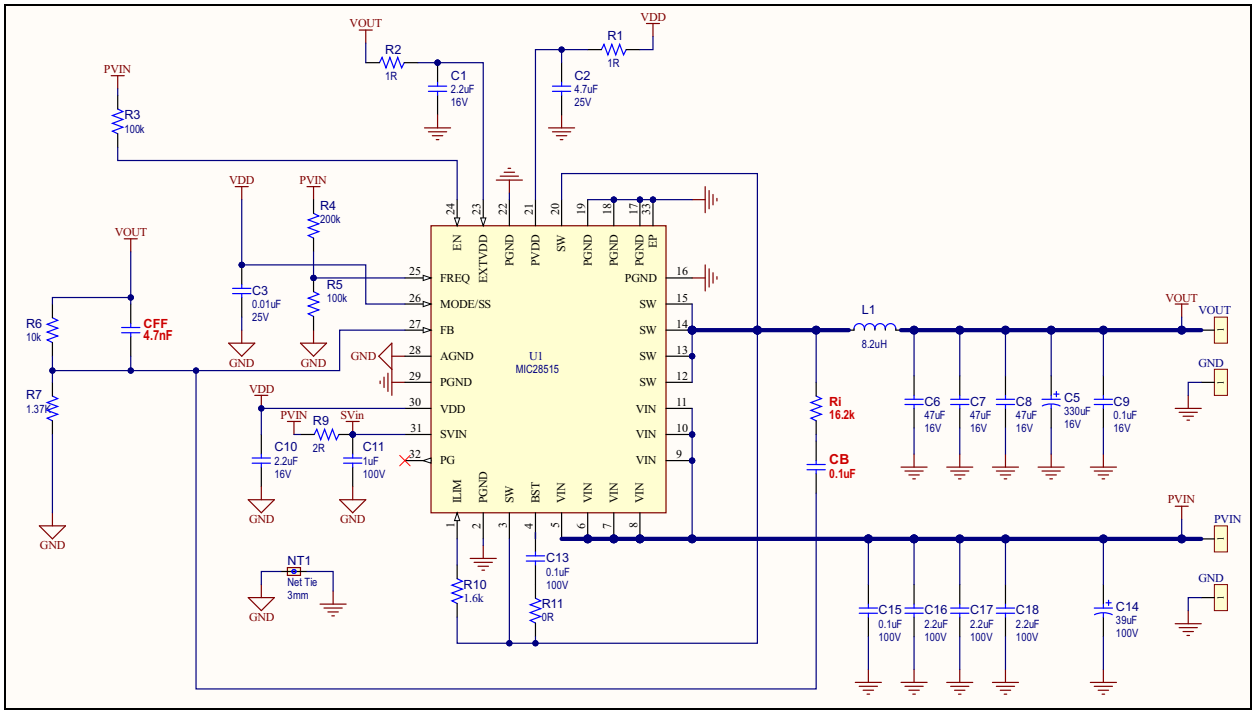


FIGURE 23: *MIC28515 Design Setup for Load Transient Test.*

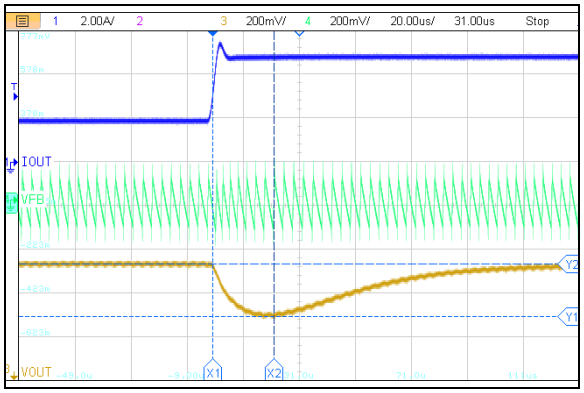


FIGURE 24: *Ri = 16.2k, CFF = 4.7 nF, ΔVFB = 245 mV, Vo Undershoot = 240 mV, Response Time = 70 µs.*

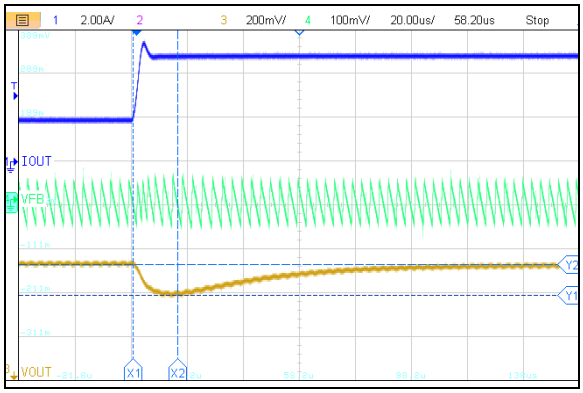


FIGURE 25: ***Ri = 36k****, CFF = 4.7 nF, ΔVFB = 108 mV, Vo Undershoot = 140 mV, Response Time = 40 µs.*

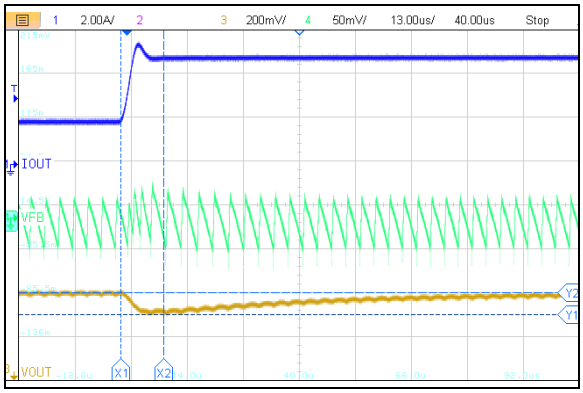


FIGURE 26: ***Ri = 68k****, CFF = 4.7 nF, ΔVFB = 55 mV, Vo Undershoot = 100 mV, Response Time = 25 µs.*

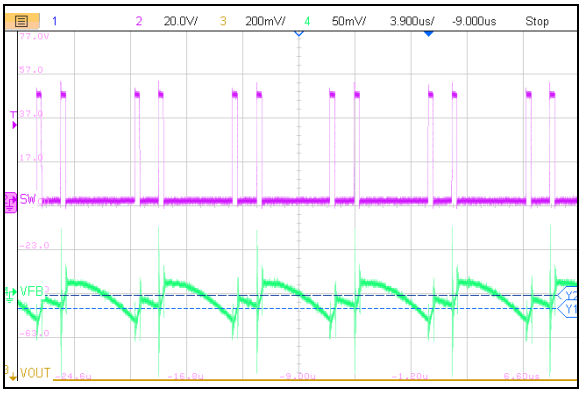


FIGURE 28: *Feedback Ripple vs. Transient Response for Transient Step 2.5 to 5A (Slew Rate = 2.5A/3 µs),* ***RINJ = 82k****,* ***CFF = 10 nF****, ΔVFB = 15 mV, Abnormal Switching and Abnormal Feedback Waveform due to Very Low Ripple at Feedback.*

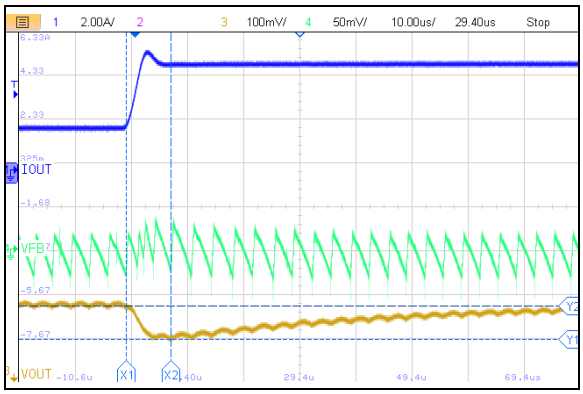


FIGURE 27: ***Ri = 82k****, CFF = 4.7 nF, ΔVFB = 45 mV, Vo Undershoot = 75 mV, Response Time = 20 µs.*

TABLE 3: IMPACT OF RIPPLE INJECTION OPTIMIZATION ON LOAD TRANSIENT PERFORMANCE

Figure	Ripple Injection Components	ZB/ZF Ratio	ΔVFB (mV)	Vo Undershoot (mV)	Response Time (µs)
Figure 24	Ri = 16.2k, CB = 0.1 µF, CFF = 4.7 nF	129	245	240	70
Figure 25	Ri = 36k, CB = 0.1 µF, CFF = 4.7 nF	286	108	140	40
Figure 26	Ri = 68k, CB = 0.1 µF, CFF = 4.7 nF	541	55	100	25
Figure 27	Ri = 82k, CB = 0.1 µF, CFF = 4.7 nF	652	45	75	20

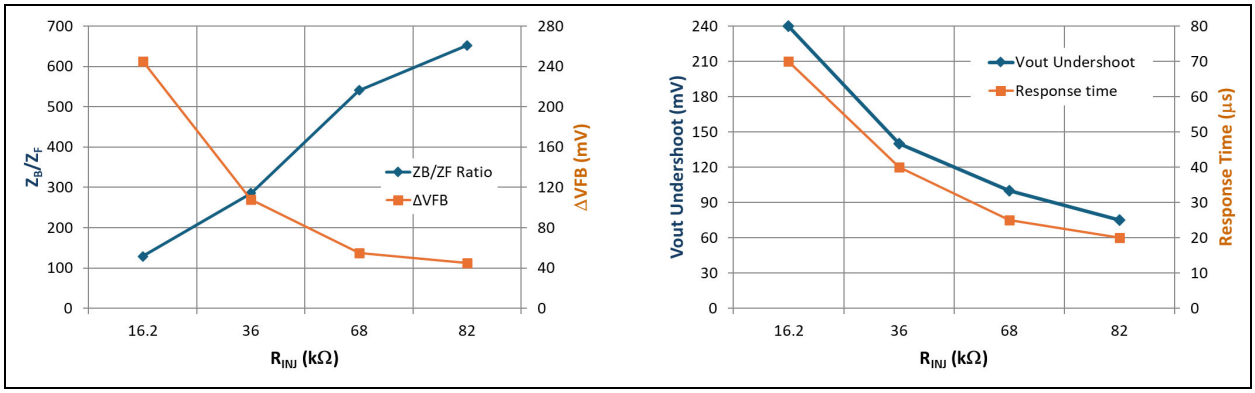


FIGURE 29: *Graphical Representation of Ri vs. ΔVFB and ΔVFB vs. Vout Recovery Time During Transient.*

Table 3 and Figure 29 provide a comprehensive summary of how optimizing ripple injection can significantly impact transient performance in ACOT-based converters. Despite ACOT's advantage in transient response compared to its counterparts, there is always room for further optimization and improvement. As discussed earlier, and derived from Equation 30, the loop gain of ACOT is heavily influenced by the injection RC impedance (ZB) and the impedance of the feed-forward network (ZF). Hence, the ratio of ZB/ZF plays a crucial role in designing the ripple injection circuit that can achieve the best transient response.

Since ACOT Buck converters are nonlinear hysteretic topology converters, evaluating these converters using classical Bode Plot open loop gain-phase measurement may yield inaccurate results and can lead to incorrect conclusions. When checking the stability of ACOT converters, it is recommended to examine load transient response in the time domain rather than loop gain/phase frequency domain measurements.

7.0 DESIGN EXAMPLE: TYPE 3 RIPPLE INJECTION DESIGN

The aim of this section is to explore the practical design steps and provide a real-world design example focusing on ripple injection circuit components. We will specifically focus on Type 3 ripple injection networks, as Types 1 and 2 are less complex and do not require as much mathematical analysis. Additionally, as discussed earlier, Type 3 offers the advantage of promising the least output ripple in the system. With this objective in mind, one of Microchip's well-known buck converters (MIC28515) was selected, to illustrate the design example. The MIC28515 is an integrated FET synchronous buck regulator that features a unique adaptive on-time control architecture, with an input range of 4.5V to 75V and 5A current rating. More details regarding the MIC28515 can be found here: https://www.microchip.com/en-us/product/mic28515.

7.1 Design Overview

The design process for a buck converter typically begins with defining the input and operating specifications before addressing various operating conditions. In this design example, the objective is to convert a 48V input to a 5V output with a capability of handling up to 5A of current. Detailed specifications for this design example are outlined in Table 4.

TABLE 4: MIC28515 DESIGN EXAMPLE SPECIFICATIONS

Parameter	Value
V_{IN}	48V
V_{OUT}	5V
I_{OUT} (max.)	5A
Switching Frequency (F_{SW})	~ 266 kHz
V_{OUT} Ripple	20 mV pk-pk
Mode of Operation	CCM

Following conventional buck converter design steps for the power stage and other configuration settings (extracted from the data sheet), we can design a basic schematic as shown in Figure 30. It is important to note that further optimization of inductor and capacitor values based on application requirements, cost, and size considerations are possible but beyond the scope of this paper. By selecting a higher value of inductance, it ensures that the ripple current remains below 10% of I_{OUT} max. Additionally, by choosing higher output capacitance with low ESR, it ensures that the output voltage ripple remains well within design specifications.

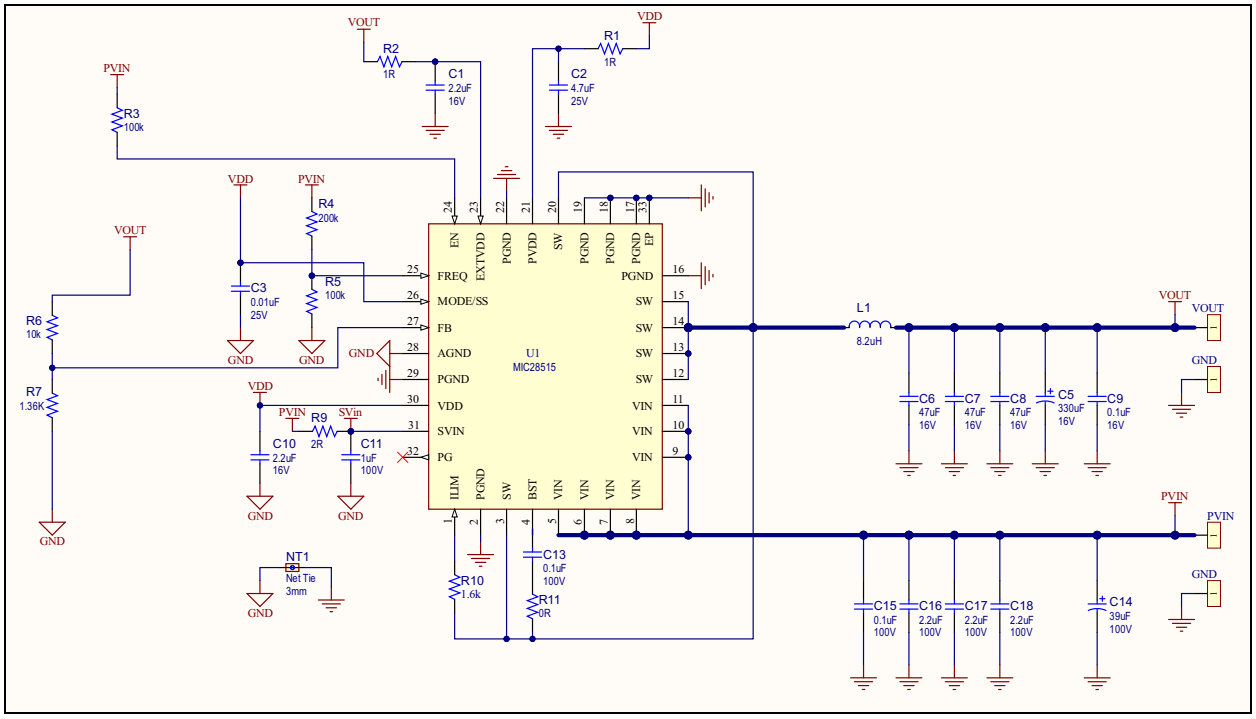


FIGURE 30: *MIC28515 Design Example without Ripple Injection.*

7.2 Ripple Injection Design Steps

Currently, it is evident that there is not much ripple at the output to rely on for feedback ripple, which is a common scenario in many application designs. In this case, it is not possible to rely on type 1 or type 2 ripple injection schemes. Instead, it is required to proceed with the type 3 ripple injection scheme. Figure 31 below illustrates the type 3 scheme.

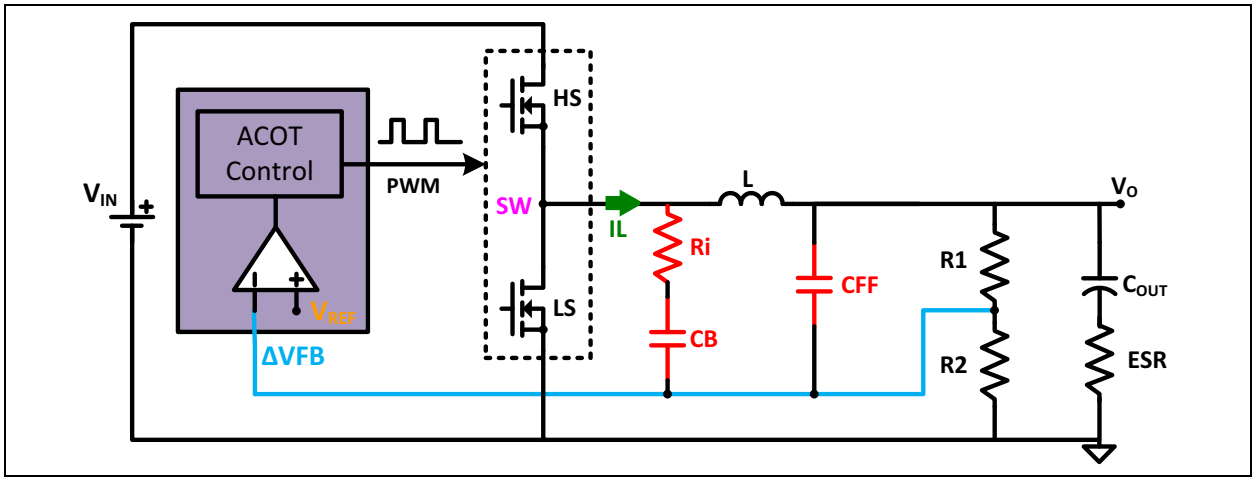


FIGURE 31: *Type 3 Ripple Injection Scheme.*

Setting DC Blocking Capacitor (CB)

The DC blocking capacitor, CB, can be chosen as 100 nF, which is typically considered an AC short for a wide range of frequencies. It is advisable to select a voltage rating for CB higher than the maximum switched node voltage.

Note:	An excessively high value of CB can slow down the control loop response, while an excessively low value can cause instability. A good rule of thumb is to set CB to 5-10 times the value of CFF. Value of CB can be fine tuned after calculating CFF or during the bench test.

Setting Feedback Resistors (R1 and R2)

Typical values for R1 (R6 in the MIC28515 schematic, Figure 30) range from 3 kΩ to 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 (R7 in the MIC28515 schematic) can be calculated using below equation:

EQUATION 33:

$$R2 = \frac{V_{REF} \bullet R1}{V_O - V_{REF}}$$

For the MIC28515, V_{REF} = 0.6V. So, considering R1 = 10k, the result is R2 = 1.36k for V_{OUT} = 5V.

Setting Feed-Forward Capacitor (CFF)

CFF should satisfy three conditions:

1. The impedance of CFF (at the switching frequency) should be much lower than R1//R2.
2. The value of CFF should be much lower than CB.
3. The time constant of the ripple injection network (τ = (R1//R2//Ri) • CFF) should be significantly higher than the total switching period (T_{SW}). Without choosing Ri, it is not possible to calculate the time constant. Therefore, this point will be addressed at a later stage and fine-tune CFF, if necessary.

If the voltage divider resistors, R1 and R2, are in the kΩ range, a CFF of 1 nF to 100 nF can easily meet the large time constant requirements. The first criteria can be verified by using Equation 20 and considering CFF = 10 nF, R1//R2 = 1.2 kΩ, and F_{SW} = 266 kHz.

$$Impedance\ of\ C_{FF} = \frac{1}{2\pi \bullet CFF \bullet F_{SW}} = 0.06\ k\Omega \ll 1.2\ k\Omega$$

The calculations above confirm that choosing 10 nF satisfies the first and second conditions. The third condition will be reassessed once the value of Ri is determined.

Ripple Injection Resistor (Ri)

The peak-to-peak amplitude of the feedback ripple (ΔVFB) must be maintained between the minimum and maximum values specified in the data sheet. For this design example, **the objective is 100 mV ripple at feedback**. A detailed exercise was previously conducted to derive Equation 18, which allows us to calculate Ri for required ΔVFB. Rewriting Equation 18 to calculate Ri:

$$Ri = \frac{V_{IN} \bullet D \bullet (1 - D)}{\Delta FB \bullet CFF \bullet F_{SW}}$$

For this design example, the duty cycle is (D) = 5/48 = 10.4%, ΔVFB = 100 mV, CFF = 10 nF, F_{SW} = 266 kHz, V_{IN} = 48V.

$$Ri = \frac{48 \bullet 0.104 \bullet (1 - 0.104)}{100\ mV \bullet 10\ nF \bullet 266\ kHz} = 16.83\ k\Omega$$

Therefore, the final **ΔVFB estimation will be 105.2 mV,** if the closest standard value as **16k** is chosen.

Time Constant Criteria and Crossover Frequency Verification

As mentioned in Section , Setting Feed-Forward Capacitor (CFF), it is crucial for the ripple injection time constant (τ) to exceed the total switching period significantly to achieve optimal linearity for the injected ripple ramp in the feedback loop.

$$\tau = (R1 \parallel R2 \parallel Ri) \bullet CFF$$

$$= (10\ k\Omega \parallel 1.36\ k\Omega \parallel 16\ k\Omega) \bullet (10\ nF) = 11.1\ \mu s$$

$$T_{SW} = 1/F_{SW} = 3.76\ \mu s$$

So, this design example meets the design criteria of **τ >> T_{SW}**.

To check the crossover frequency criteria:

$$Fcrossover(est) = \frac{Ri \bullet CFF}{2\pi \bullet L \bullet Cout}$$

$$= \frac{16\ k\Omega \bullet 10\ nF}{2\pi \bullet 8.2\ \mu H \bullet 470\ \mu F}$$

$$= 6.61\ kHz \ll F_{SW}$$

Hence, it meets the crossover frequency criteria (Equation 23) because it is much lower than switching frequency.

7.3 Bench Test Results

Now that the ripple injection design is complete, the schematic (Figure 30) can be updated by incorporating the ripple injection network and proceed to bench test. Ri = 16k, CB = 0.1 µF and CFF = 10 nF, were selected, as shown in Figure 32.

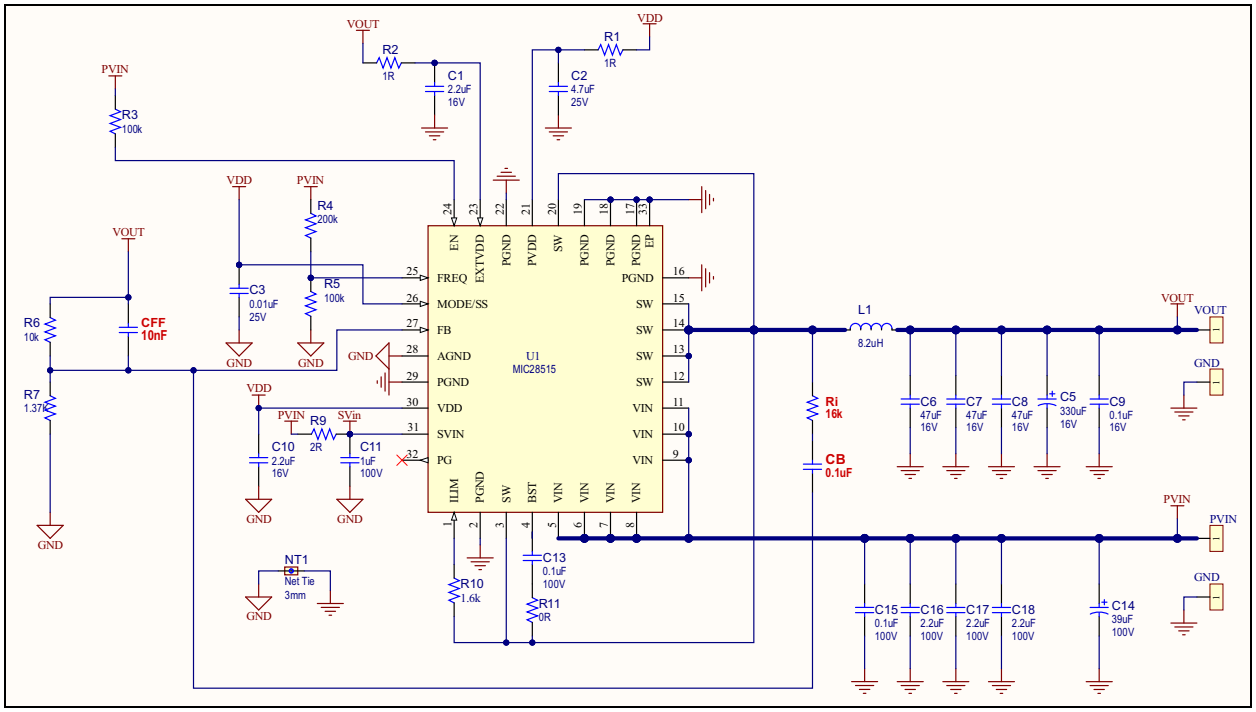


FIGURE 32: *MIC28515 Design Example with Updated Type 3 Ripple Injection Circuit.*

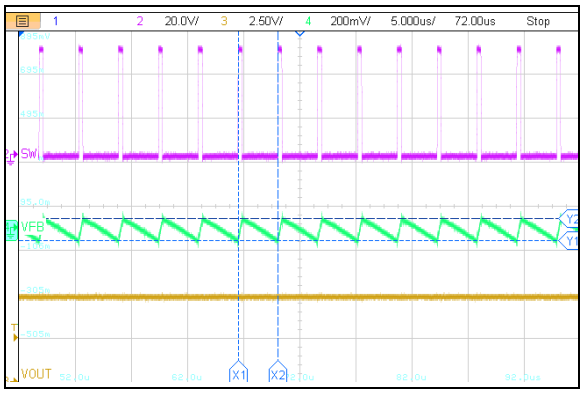


FIGURE 33: *Steady-State Performance. Feedback, Switching Node and V_{OUT} with Time Axis as 5 µs/div; ΔVFB = 100 mV.*

The bench test results (Figure 33) indicate that the feedback ripple has an amplitude of 100 mV, which is in phase with the inductor current, exhibits good linearity, and satisfies all the design requirements. The minor deviation from the calculated value (105 mV) can be attributed to slight variations in the duty cycle and switching frequency during actual operation. If necessary, the ripple injection network and the ΔVFB amplitude can be adjusted to optimize the transient response, following the design iteration steps outlined in Section 6.0, Optimizing Ripple Injection Circuit Design for Transient Response.

8.0 SPEED UP CONTROL LOOP DESIGN WITH MICROCHIP ANALOG DESIGN TOOLS

Design tools and simulation software play a crucial role in modern circuit design, offering engineers invaluable resources for conceptualization, analysis, and validation. These tools provide a virtual environment where engineers can simulate and test various circuit configurations, parameters, and operating conditions before committing to physical prototyping. By utilizing design tools and simulation software, engineers can quickly iterate through design variations, evaluate performance metrics, and identify potential issues or optimizations early in the design process. This not only accelerates the development cycle, but also reduces the cost and risk associated with physical prototyping and testing. Additionally, these tools offer insights into complex circuit behaviors that may not be readily apparent through traditional analysis methods, enabling engineers to design more robust and efficient circuits.

Microchip Technology provides a comprehensive suite of design tools and software solutions to support engineers throughout the entire product development lifecycle. Analog Treelink is a versatile PDF tool that assists engineers in selecting analog components by offering a comprehensive database of Microchip's analog products. MPLAB® Analog Designer, an online tool, assists in the design and simulation of analog circuits, simplifying the component selection and design process for analog applications. This tool

enables quick generation of schematics, performance comparisons among various solutions, and performance optimization. For advanced analysis, Microchip offers the MPLAB Mindi™ Analog Simulator, a powerful platform that allows engineers to simulate analog circuits and analyze their performance virtually.

Additionally, Microchip's Power Check Design Service provides expert guidance and support to ensure that power-related design challenges are addressed effectively. Table 5 provides a quick reference to Microchip's tools and software for designing analog power converters.

TABLE 5: MICROCHIP DESIGN SUITE

Tool/Software	More details at	Remark
Analog Treelink	https://www.microchip.com/treelinktool/	Product selection kiosk
MPLAB® Analog Designer	https://mad.microchip.com/PWR_MGMT	Online automatic design generator and solution recommender
MPLAB® Mindi™ Analog Simulator	https://www.microchip.com/en-us/tools-resources/develop/analog-development-tool-ecosystem/mplab-mindi-analog-simulator	Comprehensive simulation software
Power Check Design Service	https://www.microchip.com/en-us/products/power-management/power-check-design-service	Online design review service

Designing and optimizing control loops and refining ripple injection networks are made considerably easier and faster with the assistance of MPLAB Analog Designer and MPLAB Mindi. MPLAB Mindi integrates SIMPLIS and SIMetrix software platforms, with SIMPLIS being renowned for its effectiveness in modeling switched-mode power converters.

These software tools play a pivotal role in streamlining the design process, making it more intuitive and user-friendly.

APPENDIX

Derivation of Loop Gain Expression

As discussed in Section 4.2, Using R-C from SW Node and Feed-Forward Capacitor (Type 3), there are two components contributing to the overall feedback: VFB1 and VFB2. VFB1 occurs when VSW is high (almost equal to V_{IN}), while VFB2 contributes when VSW is essentially grounded. Hence:

EQUATION 34:

$$VFB = V_{FB1} + V_{FB2}$$

Referring to Figure 22, VFB1 and VFB2 can be expressed as:

EQUATION 35:

$$V_{FB1} = V_{SW} \bullet \frac{R2 \,/\!/\, ZF}{ZB + R2 \,/\!/\, ZF} = V_{SW} \bullet \frac{R2 \bullet ZF}{(ZB + ZF) \bullet R2 + (ZB \bullet ZF)}$$

EQUATION 36:

$$V_{FB2} = V_O \bullet \frac{R2 \,/\!/\, ZB}{ZF + R2 \,/\!/\, ZB} = V_O \bullet \frac{R2 \bullet ZB}{(ZB + ZF) \bullet R2 + (ZB \bullet ZF)}$$

And from Figure 22, VSW can be expressed as:

EQUATION 37:

$$V_{SW} = -AV \bullet VFB$$

Using Equations 35, 36 and 37, VFB can be expressed as:

EQUATION 38:

$$VFB = V_{FB1} + V_{FB2}$$

$$VFB = \left[(-AV \bullet VFB) \bullet \frac{R2 \bullet ZF}{(ZB + ZF) \bullet R2 + (ZB \bullet ZF)}\right] + \left(V_O \bullet \frac{R2 \bullet ZB}{(ZB + ZF) \bullet R2 + (ZB \bullet ZF)}\right)$$

Rearranging Equation 38, VFB/Vo can be obtained as shown below:

EQUATION 39:

$$\frac{VFB}{V_O} = \frac{1}{1 + \frac{ZF}{R2} + (1 + AV) \bullet \frac{ZF}{ZB}}$$

Placing Equation 39 in loop gain expression (Equation 29), the result is:

EQUATION 40:

$$G = \frac{-1}{\left(1 + \frac{ZF}{R2} + \frac{ZF}{ZB}\right) \bullet \frac{1}{AV} + \frac{ZF}{ZB}} \bullet \frac{ZC \,/\!/\, ZLOAD}{ZC \,/\!/\, ZLOAD + ZL}$$

By design and from test results, it is known that AV acts as a high gain amplifier at low frequencies. With this practical assumption (1/AV is almost equal to zero), the expression for Loop gain (G) could be rewritten as:

EQUATION 41:

$$G \cong -\left(\frac{ZB}{ZF} \bullet \frac{ZC \,/\!/\, ZLOAD}{ZC \,/\!/\, ZLOAD + ZL}\right)$$

REFERENCES

1. R. Redl and J. Sun, “Ripple-Based Control of Switching Regulators - An Overview,” IEEE Transactions on Power Electronics, Dec. 2009.
2. J. Sun, “Characterization and Performance Comparison of Ripple-Based Control for Voltage Regulator Modules”, IEEE Transactions on Power Electronics, Mar. 2006.
3. Jinping Wang, Jianping Xu, and Bocheng Bao, “Analysis of Pulse Bursting Phenomenon in Constant-On-Time-Controlled Buck Converter”, IEEE Transactions on Industrial Electronics, Dec. 2011.
4. T. Nabeshima, T. Sato, S. Yoshida, S. Chiba, and K. Onda, “Analysis and Design Consideration of a Buck Converter with a Hysteretic PWM Controller”, IEEE PESC Records, pp.1711-1716, June 2004.
5. Paolo Nora and Surya Talari - “Understanding and Designing a Switching Power Supply with Adaptive COT Architecture” - 20096 PC6 - Microchip Masters Conference 2016. Simplify Your Buck Converter Design with Constant-On-Time Control.
6. MIC28515 Data Sheet, “75V/5A Hyper Speed Control® Synchronous DC/DC Buck Regulator with External Mode Control”, Microchip Technology Inc., 2017, (DS20005762).

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