

Atmel AVR124: AT90PWMs Using the A/D Amplifier



8-bit Atmel Microcontrollers

Application Note

Features

- ADC features on Atmel® AVR® AT90PWM devices:
 - 10-bit ADC amplified conversion with differential inputs
 - Programmable gain
 - Internal voltage reference

1 Introduction

The AT90PWM devices feature a 10-bit successive approximation ADC. The ADC is connected to an analog multiplexer which provides:

- Eight or eleven single-ended inputs which are referenced to 0V (GND)
- One or two amplified ADC channels with differential inputs (AMPx)

Table 1-1 provides ADC configurations versus products:

Table 1-1. ADC features versus AT90PWM devices.

	AT90PWM1	AT90PWM2B	AT90PWM3B	AT90PWM216	AT90PWM316	AT90PWM81/161
A/D single-ended inputs	8	8	11	8	11	8/11
A/D differential channels	1	1	2	1	2	1

The benefits of amplified ADC channels with differential inputs are:

- Adjustable gain: 5x, 10x, 20x, or 40x
- Synchronization with external clock
- Floating inputs not referenced to V_{SS}

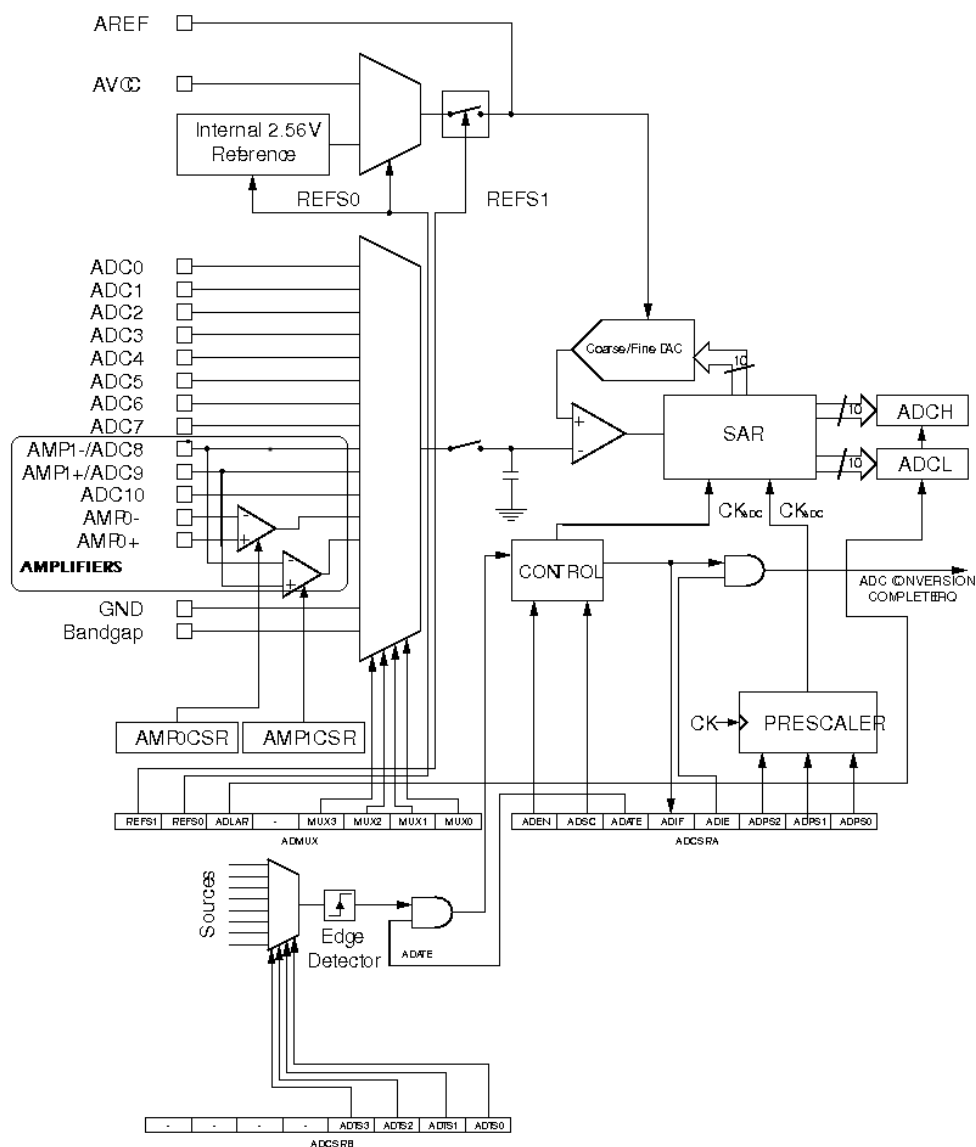
This application note provides the way to configure and use this amplified channel with ADC.



2 Block diagram

The block diagram of the ADC with eight single-ended channels and two fully differential/amplified channels is shown in [Figure 2-1](#).

Figure 2-1. ADC block diagram (Atmel AT90PWM2B/3B datasheet extract).



The A/D amplifier is placed in front of the inputs multiplexer and provides improved performances regarding real time constraints.

3 Theory of operation – The amplifier

3.1 Gain control

The differential input voltage is connected to a programmable gain stage, providing amplification steps of 14dB (5x), 20 dB (10x), 26 dB (20x), or 32dB (40x) before the A/D conversion.

3.2 Clock control

The amplifier is a switched capacitor amplifier and has three phases:

- Sampling
- Amplification
- Hold

In contrary to a purely linear analog amplifier, the output is not constantly proportional to the input, but provides an accurate value of the last sampled input signal. The amplifier needs a clock signal to operate. This clock event is termed as “synchronization clock”.

For every “synchronization clock” event, the input is Sampled/Amplified/Hold at the output of the amplifier. This value is available at the output of the amplifier until the next synchronization clock event.

3.2.1 Sampling

The maximum clock for the amplifier is 250kHz. Amplified conversions can be synchronized to any of the two clock events:

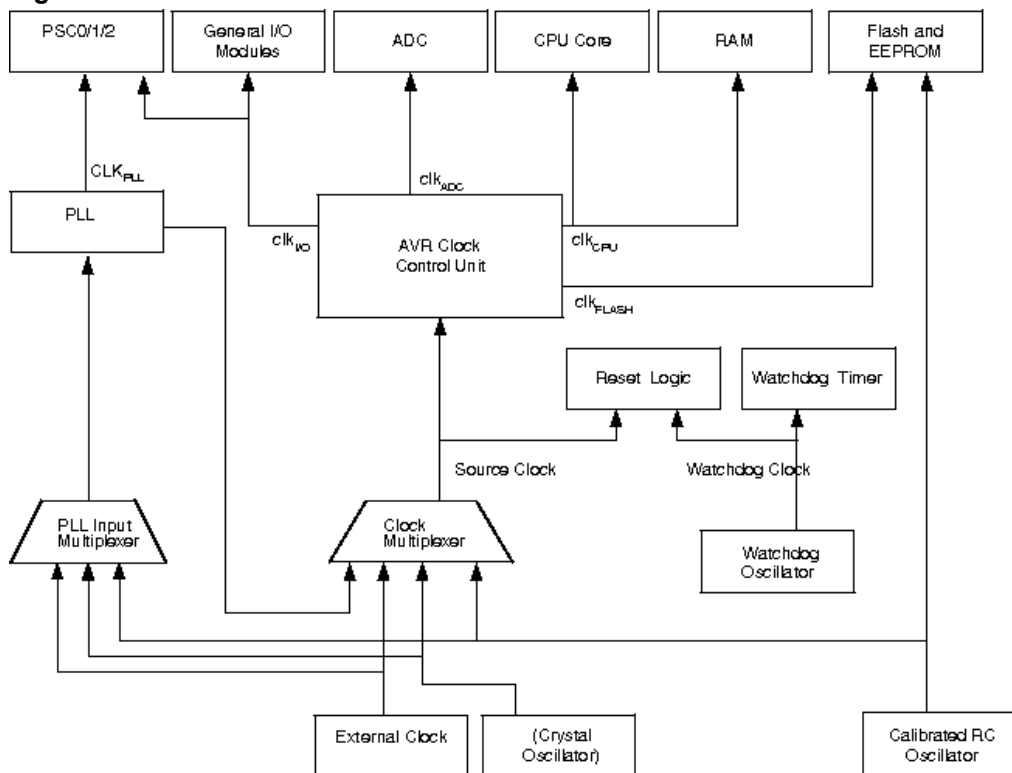
- PSC events. PSC events can be used as synchronization clock for the amplifier. Depending on the mode of operation of the PSC the **PSC n Synchro and Output Configuration** register has to be configured appropriately. More details on PSC can be found from corresponding device datasheet

NOTE

PSC events are related to the clock source for the PSC module; hence if PLL is used to clock PSC then the synchronization clock (PSC Event) has no relation to $clk_{I/O}$ (see [Figure 3-2. A/D timing.](#))

- Internal clock CK_{ADC} equal to eighth the ADC clock frequency. As the ADC maximum frequency is 2MHz, the maximum CK_{ADC} , which can be configured, is also 250kHz (see [Figure 3-1](#))

Figure 3-1. Clock distribution Atmel AT90PWM2B/3B.



3.2.2 Amplification

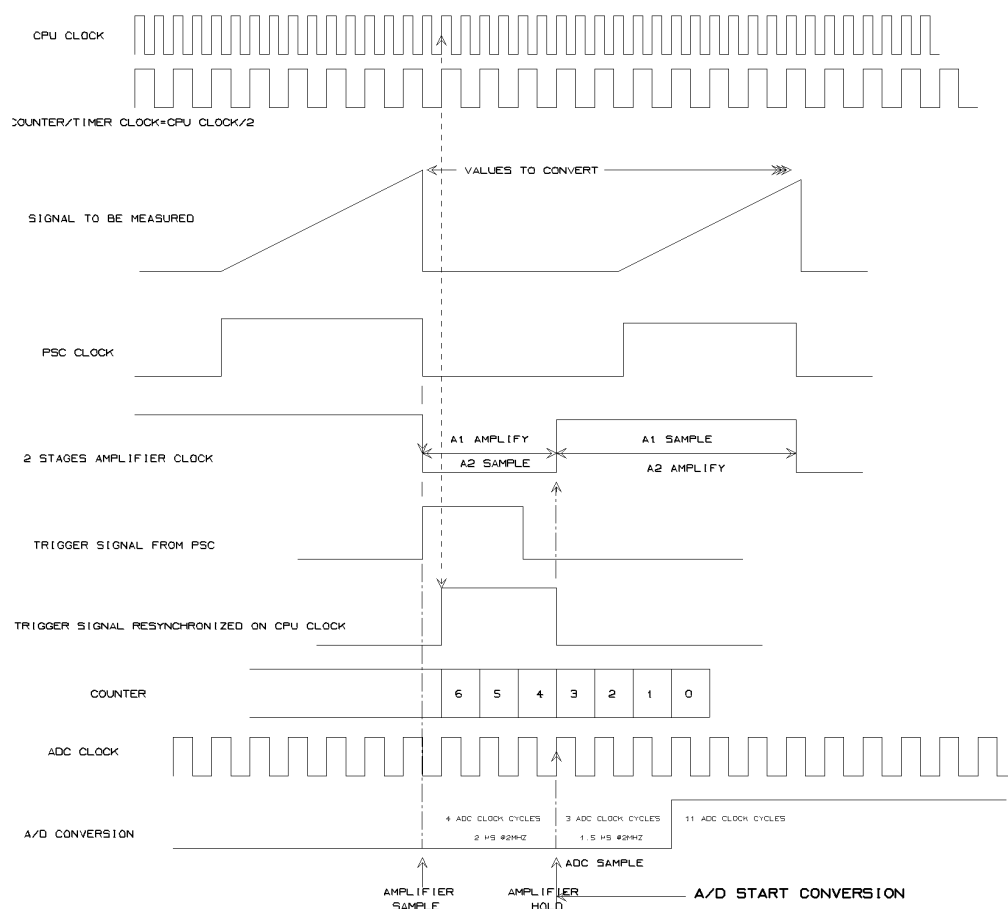
Input signal is amplified versus gain control (5x, 10x, 20x, or 40x).

3.2.3 Hold

The hold of the amplifier output is synchronized with the ADC clock. See [Figure 3-2. A/D timing](#).

This insures the sampling time of the ADC is not violated.

Figure 3-2. A/D timing.



NOTE

A1 and A2 are the two elements of the preamplifier.

Then the result is held at the output of the amplifier, waiting for a new "synchronization" event. During this time the analog to digital conversion can be processed, and the result will correspond to the latest value present at "synchronization" event.

4 Theory of operation – The A/D conversion

A conversion can be started at any moment, and the internal logic inside the microcontroller will guarantee that the result will correspond to the last “synchronization” event.

The amplification takes around 2 μ s. It means that when an analog to digital conversion is requested via the ADSC bit, there are three possibilities:

- The output of the amplifier is stable during all the sample phase of the A/D conversion: the conversion is done as fast as a single ended conversion, and the result corresponds to the conversion of the value at the latest amplifier clock event
- When A/D Conversion is started, the output of the amplifier is not stable. In this case the conversion is not started until the output of the amplifier is stable, and the result corresponds to the conversion of the value at the latest amplifier clock event
- The clock event appears during the sample phase of the AD conversion (it means that conversion has been started and during the sample phase of the conversion the clock event appeared). In this case, even though the sample phase of the ADC is started, as an event clock of the amplifier appears, the sampling of ADC is aborted, and restarted as soon as the output of the amplifier is stable again. Then the ADC result corresponds to the input value there was at the latest amplifier clock event

According to [Figure 3-2. A/D timing.](#), even if the amplification is synchronized with a PSC event, the A/D conversion result could be (and often is) completely asynchronous with this event.

This is the reason why even though it seems not be synchronized on the scope, the synchronization mechanism guarantee internally that the sampled data is the most recent and reliable regarding the application.

5 Using the amplifier

The way to use the amplifier is:

- To select a synchronization clock via the AMPxTS1:0 bits in the AMPxCSR register (example for AMP0 [Table 5-2](#))
- To switch on the amplifier via the bit AMPnEN (example for AMP0 [Table 5-1](#))

Then, the amplification is achieved on each synchronization event. The amplification is done independent of the ADC.

Table 5-1. Amplifier 0 control and status register – AMP0CSR.

Bit	7	6	5	4	3	2	1	0	
	AMP0EN	AMP0IS	AMP0G1	AMP0G0	-	-	AMP0TS1	AMP0TS0	AMP0CSR
Read/Write	R/W	R/W	R/W	R/W	-	-	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – AMP0EN: Amplifier 0 Enable Bit**

Set this bit to enable the amplifier.

Clear this bit to disable the amplifier.

Clearing this bit while a conversion is running will take effect at the end of the conversion.

WARNING

Always clear AMP0TS1:0 when clearing AMP0EN.

- **Bit 1, 0– AMP0TS1, AMP0TS0: Amplifier 0 Trigger Source Selection Bits**

In accordance with the **Error! Reference source not found.**, these two bits select the event which will generate the trigger for the amplifier 0. This trigger source is necessary to start the conversion on the amplified channel.

Table 5-2. XXXXXXXXXXXXXXXXXXXXXXXX.

AMP0TS1	AMP0TS0	Description
0	0	Auto synchronization on ADC clock/8
0	1	Trig on PSC0ASY
1	0	Trig on PSC1ASY
1	1	Trig on PSC2ASY

5.1 Synchronization clock

In case of synchronization with PSC, the amplifier samples/amplifies at the programmed time via synchronization configuration of PSC. The configuration bits are PSYNCn1 and PSYNCn0: see [Table 5-3](#) for PSC0.

Then the result is held at the output of the amplifier, waiting for a new event. During this time the analog to digital conversion can be processed, and the result will correspond to the value at latest synchronization event.

Table 5-3. PSC Synchro and Output Configuration – PSOC0.

Bit	7	6	5	4	3	2	1	0	
	-	-	PSYNC01	PSYNC00	-	POEN0B	-	POEN0A	PSOC0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

• **Bit 5:4 – PSYNCn1:0: Synchronization Out for ADC Selection**

Select the polarity and signal source for generating a signal which will be sent to the ADC for synchronization.

Table 5-4. Synchronization source description on one/two/four ramp modes.

PSYNCn1	PSYNCn0	Description
0	0	Send signal on leading edge of PSCOUTn0 (match with OCRnSA)
0	1	Send signal on trailing edge of PSCOUTn0 (match with OCRnRA or fault/retrigger on part A)
1	0	Send signal on leading edge of PSCOUTn1 (match with OCRnSB)
1	1	Send signal on trailing edge of PSCOUTn1 (match with OCRnRB or fault/retrigger on part B)

Table 5-5. Synchronization source description in centered mode.

PSYNCn1	PSYNCn0	Description
0	0	Send signal on leading edge of PSCOUTn0 (match with OCRnSA)
0	1	Send signal on trailing edge of PSCOUTn0 (match with OCRnRA or fault/retrigger on part A)
1	0	Send signal on leading edge of PSCOUTn1 (match with OCRnSB)
1	1	Send signal on trailing edge of PSCOUTn1 (match with OCRnRB or fault/retrigger on part B)

5.2 Conversions on amplified channel

The following sequence has to be followed to start an A/D conversion on an AMPx channel:

- Configure and enable ADC
- Select the AMP channel in ADMUX
- Start the conversion with ADCSRA |= (1<<ADSC)

Then the internal logic inside the microcontroller will guarantee that the result will correspond to the last event according to PSYNC0x configuration.

When working with the amplifier, the auto-triggering mode of the ADC is not used since the trigger has been configured in AMPxCSR register ([Table 5-1](#)).

So the ADC Auto Trigger Enable bit (ADATE in ADCSRA), ADC Trigger Select bits and ADTS in ADCSRB used for free running mode cannot be used while using amplified A/D conversion.

Auto-triggering (free running mode) is not possible on amplified channel. The only way to achieve repeated conversions on amplifier channel is to write ADSC bit to start conversion via software.

6 Application example

Typical applications of Atmel AT90PWMs products are lighting and motor control. These applications use built in features like timers with PWM functionality and high-speed ADC.

This application note refers to a motor application. One schematics example using an H-bridge is shown in [Table 6-1](#).

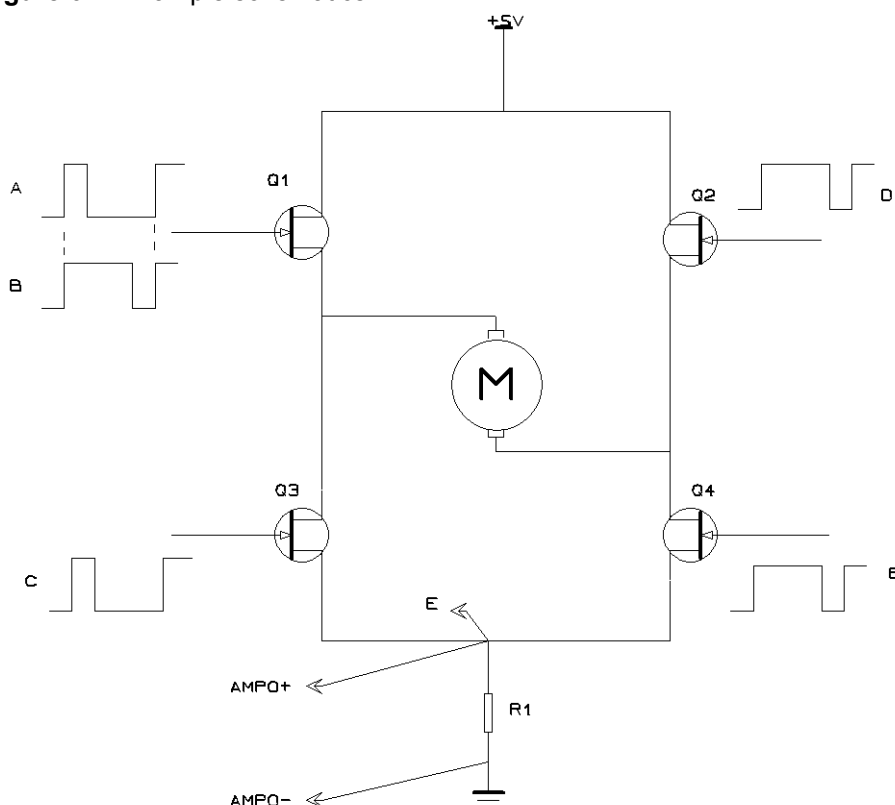
The MOS transistors are driven by the microcontroller according to quadrant switching scheme. The command signals of transistors are controlled with PWM outputs of PSC which is the main feature used to control the motor. Application notes examples for motor control can be downloaded from the Atmel website.

ADC channel can be used to measure motor current and also other parameters such as motor temperature.

This application note provides example of current monitoring.

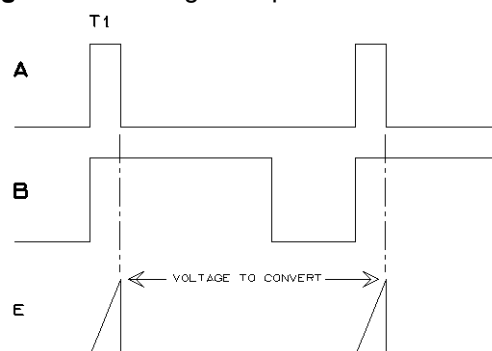
This is achieved with the voltage measurement across R1 (test point is E on schematics in [Table 6-1](#)).

Figure 6-1. Example schematics.



The constraint is to get an exact A/D sample value at the end of T1 (see waveforms in [Table 6-2](#)).

Figure 6-2. Timing example.



6.1 Software implementation

In order to make such a measurement the best solution is to use the amplifier.

It allows decreasing the shunt value and also it provides an accurate sampling of the signal value.

An example program is provided in the software package attached to this application note.

In this example, the following configurations are used:

- AMP0 configuration

To configure with Trig. on PSC0 and enable AMP0 Amplifier, according to [Table 6-1](#), AMP0CSR = 1000 0001 = 0x81.

- PSC0 configuration

To configure the PSC0RA moment to generate PSC0ASY signal:

PSYNC01 = 0 and PSYNC00 = 1 in PSOC0 register.

According to [Table 5-3](#), PSOC0 = 0x25.

- Gain control

A gain five is configured on the AMP0 amplifier as follows:

AMP0G1-0 = 00; ([Table 6-1](#)).

Table 6-1. Amplifier 0 Control and status register – AMP0CSR.

Bit	7	6	5	4	3	2	1	0	
	AMP0EN	AMP0IS	AMP0G1	AMP0G0	-	-	AMP0TS1	AMP0TS0	AMP0SCR
Read/Write	R/W	R/W	R/W	R/W	-	-	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 5, 4– AMP0G1, 0: Amplifier 0 Gain Selection Bits**

These two bits determine the gain of the amplifier 0.

The different settings are shown in [Table 6-2. Amplifier 0 Gain Selection](#).

Table 6-2. Amplifier 0 Gain Selection.

AMP0G1	AMP0G0	Description
0	0	Gain 5
0	1	Gain 10
1	0	Gain 20
1	1	Gain 40

To ensure an accurate result, after the gain value has been changed, the amplifier input needs to have a quite stable input value during at least four amplifier synchronization clock periods.

- A/D Clock

A/D Clock configuration is achieved via ADPS2-0 in ADCSRA register (see [Table 6-3](#)).

The ADC can work at a speed as high as 2MHz. We advise to operate at this frequency.

Table 6-3. ADC Control and Status Register A - ADCSRA.

Bit	7	6	5	4	3	2	1	0	
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 2, 1, 0– ADPS2, ADPS1, ADPS0: ADC Prescaler Selection Bits**

These three bits determine the division factor between the system clock frequency and input clock of the ADC.

The different settings are shown in [Table 6-4. ADC prescaler selector](#).

Table 6-4. ADC prescaler selector.

ADPS2	ADPS1	ADPS0	Division factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

6.2 Hardware configuration

The configurations according to this example are the following:

- Device side:
 - Atmel AT90PWM3B with fuse configuration: F9 / DF / 4E @ 8MHz
 - Using Atmel STK[®] 520 + Atmel STK500
 - or Atmel STK600 + Atmel STK600-RCPWM-19 + Atmel STK600-SOIC

- PC side:

Terminal configuration: 2400 bit/s - 8bits data - 1 stop bit - no parity.

The terminal will display the Hex value of the AMP0 input voltage.

6.3 Conclusion

A/D amplifier provides, in this example, the capability to sample a floating voltage at a specific time, to amplify this signal and finally convert it to digital.

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