MICROCHIP

AN3471

Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Using PD702x1 and PD701x1 ICs

Introduction

This application note provides guidelines for designing a Power over Ethernet (PoE) Powered Device (PD) system for IEEE® 802.3af, IEEE 802.3at, HDBaseT (PoH), and Universal Power Over Ethernet (UPoE) applications by using Microchip's family of PD integrated circuits. The following table summarizes Microchip PD products offerings.

Table 1. Microchip Powered Device Products Offerings

Part	Type	Package	IEEE 802.3af	IEEE 802.3at	HDBaseT (PoH)	UPoE
PD70100	Front end	3 mm × 4 mm 12L DFN	x	—	—	—
PD70101	Front end + PWM	5 mm × 5 mm 32L QFN	x	—	—	—
PD70200	Front end	3 mm × 4 mm 12L DFN	x	x	—	—
PD70201	Front end + PWM	5 mm × 5 mm 32L QFN	x	x	—	—
PD70210	Front end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210A	Front end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210AL	Front end	5 mm × 7 mm 38L QFN	x	x	x	x
PD70211	Front end + PWM	6 mm × 6 mm 36L QFN	x	x	x	x
PD70224	Ideal diode bridge	6 mm × 8 mm 40L QFN	x	x	x	x

Microchip offers PD devices that integrate the front-end PD and the PWM into the product package. Additionally, Microchip offers standalone front-end PD devices that require an external PWM IC to convert the high PoE voltage down to the regulated supply voltage used by the application. The front-end section provides the necessary detection, classification, power-up functions and operating current levels compliant with the listed standards. The PWM section controls the conversion of the PoE high voltage down to regulated supply voltage used by the application. The scope of this application note is to describe the design of a PoE PD front end and integrated PWM section based on Microchip PD701x1/PD702x1 products. This document also includes a description of key features and functions of Microchip's PD products, a brief overview of PoE functionality, standards and key technical considerations for a PoE PD design.

Microchip offers a complementary product for PoE PD applications, the PD70224 Ideal Diode Bridge, which is a low-loss alternative to the dual diode bridges for input polarity protection.

Microchip offers complete reference design packages and Evaluation Boards (EVBs). For access to these design packages, device datasheets, or application notes, consult your local Microchip Client Engagement Manager or visit our website at www.microchip.com/poe.

For technical support, consult your local Embedded Solutions Engineers or go to microchipsupport.force.com/s/.

Microchip PoE PD Controller Key Features

The following are common features of all Microchip PoE PD controllers.

- Provides PD detection signature
- Programmable PD classification signature
- Integrated isolation switch
- 24.9 kΩ detection signature resistor disconnection when power is on, for power saving
- Inrush current limit (soft start)
- Integrated 10.5 V start-up supply output for DC-DC converters
- Overload protection
- Internal discharge circuitry for DC-DC bulk capacitor
- Wide temperature operating range –40 °C to 85 °C
- On-chip thermal protection
- 100 kHz to 500 kHz programmable DC-DC switching frequency
- DC-DC frequency can be synchronized to external clock
- Supports low power mode operation for higher efficiency
- Soft-start circuit to control the output voltage rise time
- Support efficient synchronous rectification or active clamp topologies
- PoE Port Input UVLO with programmable threshold and hysteresis
- Internal differential amplifier simplifying non-isolated step-down converter
- Overload and short circuit protection
- Pulse-by-pulse current limit

The following table summarizes features that vary across PoE PD controllers.

Table 2. Microchip PoE PD Controller Key Features

Part Number	IC Type	Standards	Max Power (W)	Max Current (A)	Max Resistance (Ω)	FLAGS[1]	WA Priority Pin[2]	VAUX
PD70101	Front End + PWM	IEEE 802.3af	15.4	0.45	0.6	PGOOD	No	Yes
PD70201	Front End + PWM	IEEE 802.3af IEEE 802.3at	47	1.123	0.6	AT PGOOD 2-event	No	Yes
PD70211	Front End + PWM	IEEE 802.3af IEEE 802.3at PoH UPoE	95	2.0	0.3	AT 4P_AT HD 4P_HD	Yes	Yes
PD70224	Ideal Diode Bridge	IEEE 802.3af IEEE 802.3at PoH UPoE	95	2	0.76	N/A	N/A	N/A

Note:

1. For detailed descriptions, see section General Operation Theory.
   1.1. AT—AT flag
   1.2. 4P_AT—4-pair AT flag
   1.3. HD—HDBaseT flag
   1.4. 4P_HD—4-pair HDBaseT
   1.5. PGOOD—Power Good flag
2. WA priority pin controls support of wall adapter functionality and enforces auxiliary supply priority to supply power to the load from an external DC source.

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1. PoE Overview

PoE consists of a power source, referred to as Power Source Equipment (PSE), an Ethernet or Network cable (typically contained in an infrastructure) with maximum length of 100 meters, and a Powered Device (PD) that accepts both data and power from the Power Interface (PI) of the Ethernet cable. The PI is typically an eight pin RJ45 type connector. The PSE typically resides in an Ethernet Switch or Midspan. The PD resides in what is sometimes referred to as Data Terminal Equipment (DTE). A diagram of this arrangement is shown in the following figures.

Figure 1-1. Two-Pair Power over Data—Alternative A

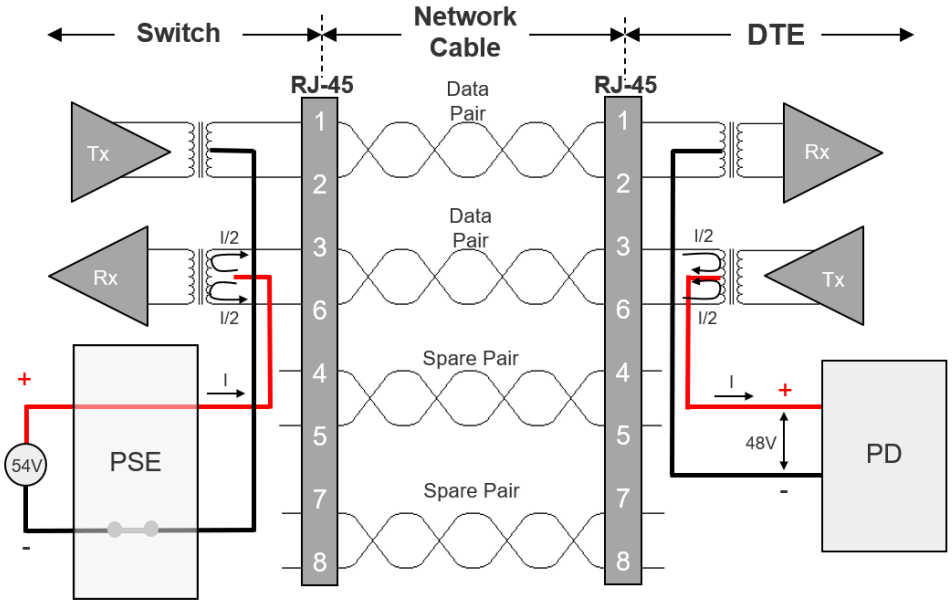


Figure 1-2. Two-Pair Power over Spare—Alternative B

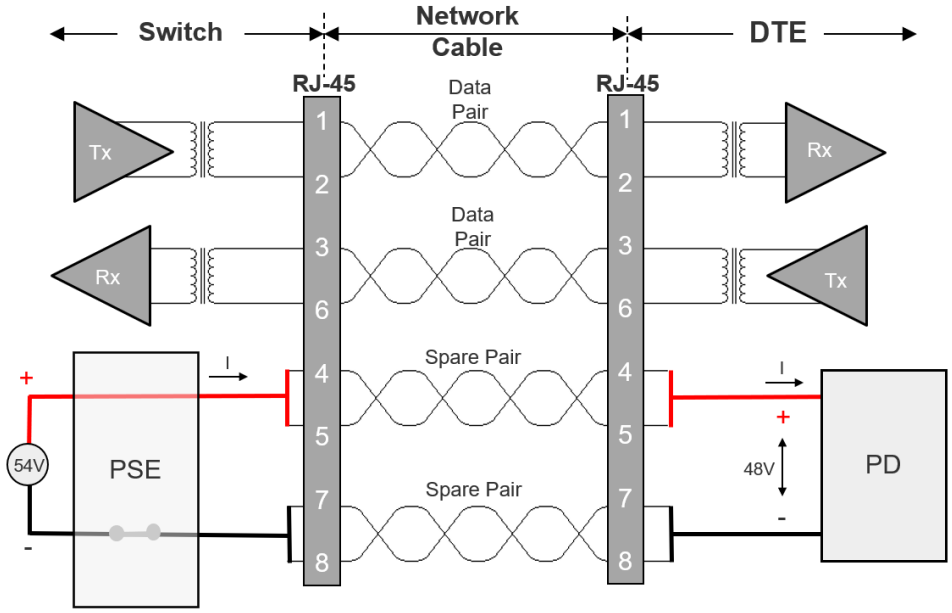
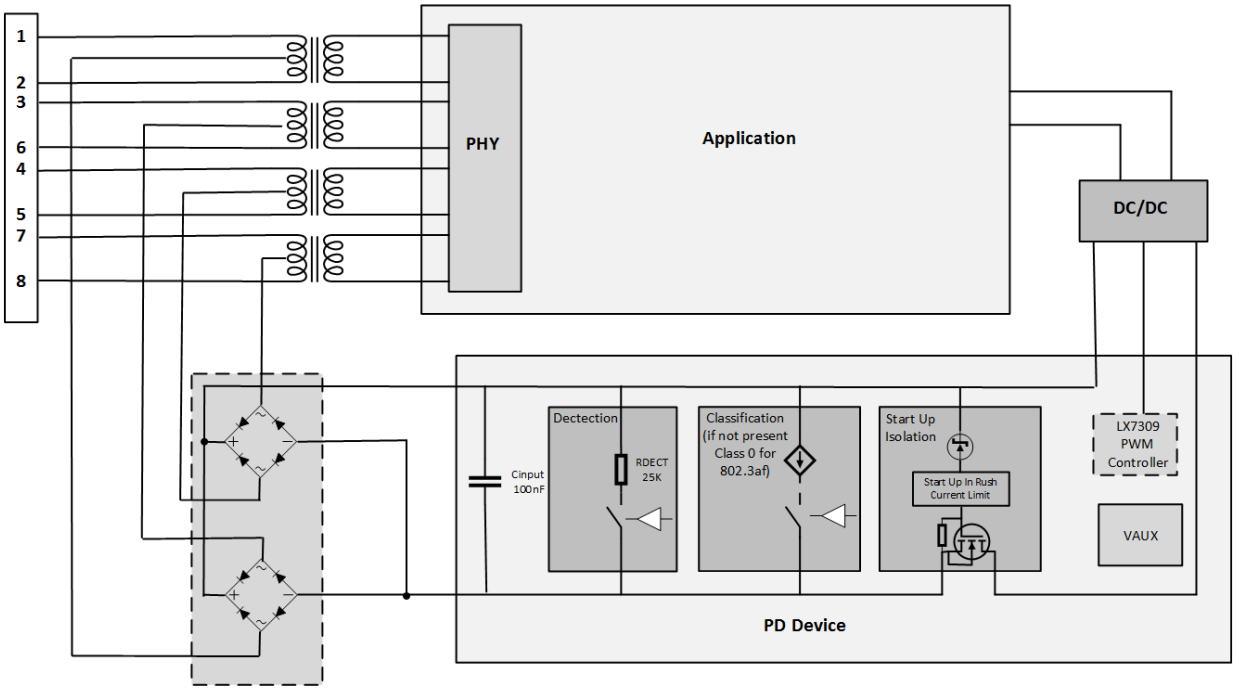


Figure 1-3. Basic PD Block Diagram



The PD provides the following functions.

- Polarity protection—Voltage polarity at the PI is not guaranteed by standards. Therefore, a diode bridge is used to ensure correct polarity at the PD input. For optimized power loss and PCB area, use the Microchip PD70224 Ideal Diode Bridge. Standard diode bridges may also be used.
- Detection—Provides signature for detection.
- Classification—Provides signatures for classification signatures.
- Start-up—After detection and classification, provides a controlled power application.
- Isolation—The PoE domain must have 1500 V_{AC} isolation from earth ground and from user accessible parts. It is recommended to provide this isolation via an isolated DC/DC convertor. With non-isolated designs, the end application would have to provide this isolation. There is a perception that non-isolated design saves cost, but in reality, this is not necessarily true because you still need to provide the controller's bias after initial start-up, which means a custom inductor with auxiliary bootstrap winding.
- VAUX—Bias for DC/DC start-up. All Microchip PoE PD ICs have an available regulated voltage output, VAUX, to be used primarily as a start-up supply for an external DC/DC controller. VAUX is a low current, low duty cycle output, providing current momentarily until an external bootstrap supply can take over.
- PWM Controller and DC/DC—Converts high PoE voltage down to regulated supply voltage used by the application. The PWM may be external Microchip device or integrated into the Microchip PD package.

The following tables compare PoE standards for the PSE and the PD. The HDBaseT (PoH) standard follows IEEE 802.3at type 2 cable types. However, due to its higher supported current, it limits the number of cables in a single cable bundle.

Table 1-1. IEEE 802.3af, 802.3at, and HDBaseT Standards for PSE

PSE Requirements	IEEE 802.3af or IEEE 802.3at Type 1	IEEE 802.3at Type 2	2-Pair HDBaseT Type 3	4-Pair HDBaseT Type 3
Guaranteed power at PSE output	15.4 W	30 W	47.5 W	95 W
PSE output voltage	44 V to 57 V	50 V to 57 V	50 V to 57 V	50 V to 57 V
Guaranteed current at PSE output	350 mA DC with up to 400 mA peaks	600 mA DC with up to 686 mA peaks	950 mA DC with up to 1000 mA peaks	2x 950 mA DC with up to 2000 mA peaks
Maximum cable loop resistance	20 Ω	12.5 Ω	12.5 Ω	12.5Ω
Physical layer classification	Optional	Mandatory	Mandatory	Mandatory
Supported physical layer classification classes	Class 0 to 4	Class 4 mandatory	Class 4 mandatory	Class 4 mandatory
Data link classification	Optional	Optional	Optional	Optional
2-Events classification	Not required	Mandatory	Not required	Not required
3-Events classification	Not required	Not required	Mandatory	Mandatory
4-pair power feeding	Not allowed	Allowed	NA	Allowed
Communication supported	10/100 BaseT (Midspan) 10/100/1000 BaseT (switch)	10/100/1000 BaseT including Midspans (Both type1 and type2)	10/100/1000/ 10000 BaseT	10/100/1000/ 10000 BaseT

Table 1-2. IEEE 802.3af, 802.3at, and HDBaseT Standards for PD

PD Requirements	IEEE 802.3af or IEEE 802.3at Type 1	IEEE 802.3at Type 2	HDBaseT Type 3
Guaranteed power at PD input after 100 m cable	12.95 W	25.50 W	72.40 W
PD input voltage	37 V to 57 V	42.5 V to 57 V	38.125 V to 57 V
Maximum DC current at PD input	350 mA	600 mA	1.7 A
Physical layer classification	Mandatory (No class= Class 0)	Mandatory	Mandatory
Supported physical layer classification classes	Class 0 to 4	Class 4 mandatory	Class 4 mandatory
Data link classification	Optional	Optional	Optional
2-Events classification	Not required	Mandatory	Optional
4-pair power receiving	Allowed	Allowed	Supports
Communication supported	10/100 BaseT (Midspan) 10/100/1000 BaseT (switch)	10/100/1000 BaseT including Midspans (both type 1 and type 2)	10/100/1000/10000 BaseT

DC voltage through wire pairs can be of either polarity. To accommodate all possible combinations of PoE power available at the PI, a use of the PD70224 Ideal Diode Bridge or dual diode bridges on the PD side is required.

In the detection phase, standards define methods of determining whether a cable is connected to a standard compliant PD, that is a device capable of receiving power, connected to a non-power receiving capability device or disconnected.

These standards further define methods of determining power requirements or how much power the connected PoE-compliant PD can receive and methods by which the PD may determine the power level that is supported by the PSE. This is called the classification phase.

A compliant PSE does not apply operating power to the PI until it has successfully detected a PoE compliant PD. During detection phase, a PSE applies a series of low voltage test pulses between 2.80 V and 10.0 V. In response to these pulses a PoE-compliant PD must provide a valid signature, which requires differential resistance between 23.7 kΩ and 26.3 kΩ and input capacitance between 50 nF and 120 nF. To provide a valid detection resistance, all Microchip PoE PD controllers require an external 24.9 kΩ resistor. This resistor is connected between the PD device's VPP and RDET pins. When a Microchip PD controller observes input voltage in the detection range 2.7 V to 10.1 V, it internally connects this resistor to the PI. After detection phase is over, the Microchip controller automatically disconnects the detection resistor to avoid extra power losses. A 100 V ceramic capacitor must be connected between the VPP and VPN in pins of the PD device to provide a valid detection capacitance (recommended values 82 nF to 100 nF).

After a valid signature is detected, the PSE may start the classification phase. Classification is optional for 802.3af and 802.3at type 1 PSEs and PDs; and is mandatory for 802.3at type 2 and PoH. The PSE increases the voltage into a voltage range of 15.5 V to 20.5 V for a specified time duration. This is called a classification finger. If more than one finger is required, the classification fingers are separated by what is referred to as the mark voltage, where the PSE lowers voltage to the range between 6.3 V to 10.1 V, again for a specified time.

While the classification voltage or class finger is applied, the PD then must draw a constant current to signal its class. In Microchip controllers the classification signature is programmed by a resistor RCLS connected between the PD devices RCLS and VPN in pins. When input voltage is in the classification range, the PD draws current programmed by RCLS.

An IEEE 802.3at type 2 compliant PD is required to recognize the 2-event classification and provide to internal circuits the AT flag signal that indicates PD is connected to an AT type 2 compliant PSE.

A PoH type 3 compliant PD is required for recognizing the 3-event classification and provide to internal circuits the HDBaseT flag signal that indicates PD is connected to an HDBaseT type 3 compliant PSE.

Should the port voltage present at the PI drop below 2.8 V, PSE class information resets and the PD must reset the class dependent flag.

Microchip PoE PDs contain an isolating switch that disconnects the return side of the PD from the PI during detection and classification phases, or during power loss and overload. The PD turns the isolating switch on at PI voltage levels 42 V or higher and turn off the isolating switch at PI voltage levels below 30.5 V. They also actively limit the current during start-up to 350 mA or less.

Figures Basic PoE Detection, Classification, and Power-Up Sequences for IEEE 802.3af Standard and Basic PoE Detection, Classification, and Power-Up Sequences for 802.3at Standard show the basic PoE detection, classification, and power-up sequences for type 1 IEEE 802.3af and type 2 IEEE 802.3at, respectively. Class levels, their corresponding currents, and recommended RCLS resistors are listed in table Classification Current Definitions and Required Class Setting Resistors.

Figure 1-4. Basic PoE Detection, Classification, and Power-Up Sequences for IEEE 802.3af Standard

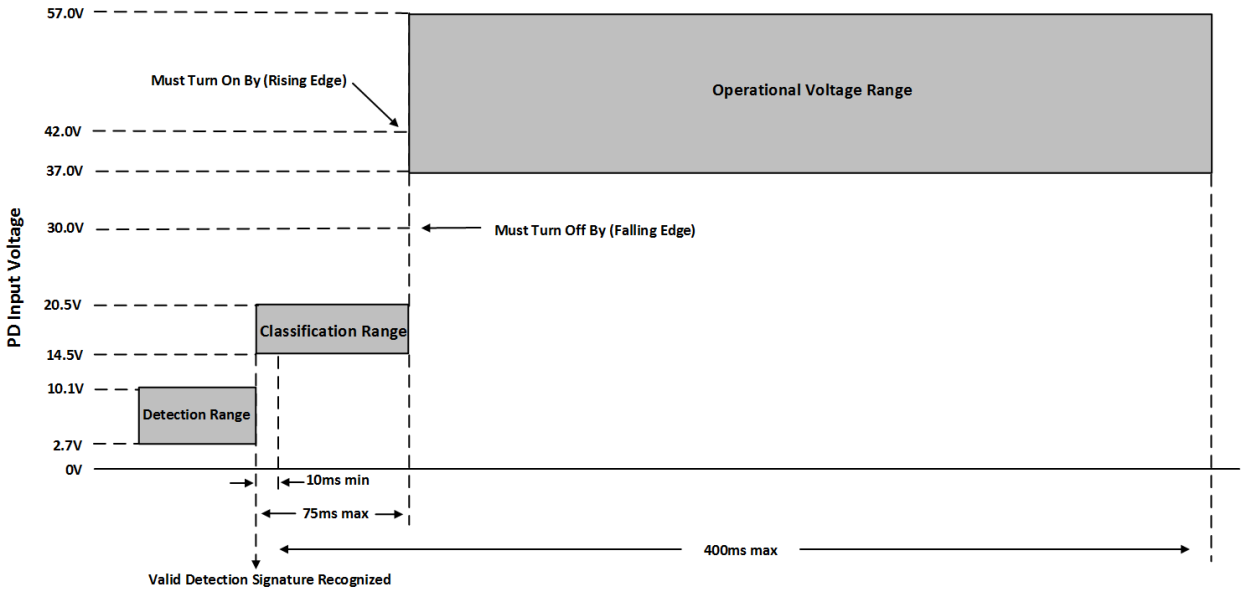


Figure 1-5. Basic PoE Detection, Classification, and Power-Up Sequences for 802.3at Standard

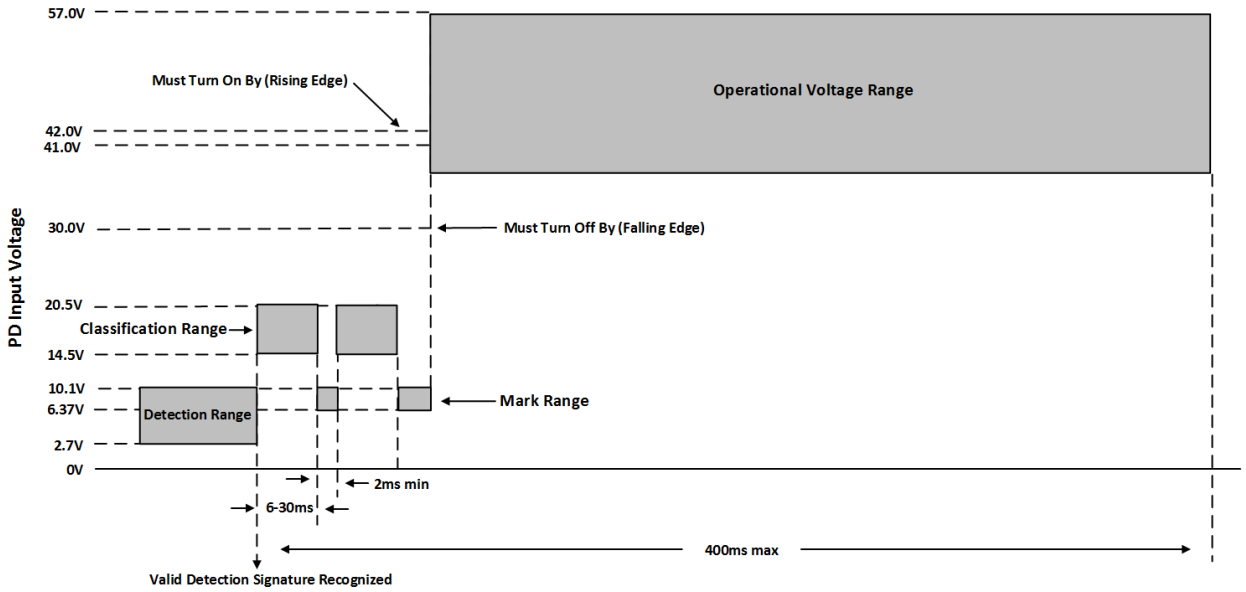


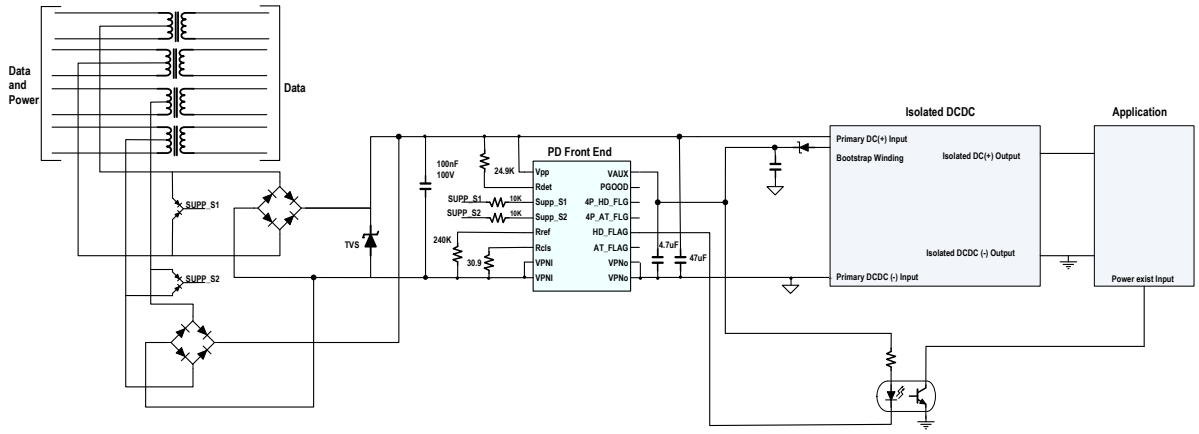
Table 1-3. Classification Current Definitions and Required Class Setting Resistors

Class	PD Current Draw During Classification			RCLASS Resistance Values, Ω
	Min	Nominal	Max	
0	0 mA	NA	4 mA	Not installed
1	9 mA	10.5 mA	12 mA	133
2	17 mA	18.5 mA	20 mA	69.8
3	26 mA	28 mA	30 mA	45.3
4	36 mA	40 mA	44 mA	30.9
Note: PD input voltage during classification phase is 14.5 V to 20.5 V.				

2. Using PD702x1 and PD701x1 ICs

The PD702x1 and PD701x1 ICs may be used for both 2-pair and 4-pair systems, as shown in the following figure. The output from the two diode bridges are connected to V_{PP} (positive bus) and VPN_{IN} (negative bus). Output connections to the DC/DC converter/application are made between V_{PP} and VPN_{OUT}.

Figure 2-1. Typical 2- or 4-Pair Configuration with a Single PD70211



In addition to the basic input/output connections, the following external components are required for a typical application:

- **Detection resistor:** Connect a 24.9 kΩ ±1% resistor between V_{PP} and R_{DET} pin. This resistor is used to provide the detection signature. A low wattage type may be used as there is less than a 7 mW stress on this resistor while detection phase is active, and the resistor is disconnected after power is on.
- **Reference resistor:** A resistor setting bias current for internal circuitry has to be connected between R_{REF} pin and VPN_{IN}. Connect a 60.4 kΩ ±1% resistor for PD70211 IC and 240 kΩ ±1% for PD70101/PD70201. This resistor must be located close to the IC. A low wattage type may be used (power dissipation is less than 1 mW).
- **Classification current resistor:** The value of the resistor connected between R_{CLASS} pin and VPN_{IN} determines the PD current draw during the classification phase. Values corresponding to IEEE compliant classification levels are provided in the previous table.
- **Input capacitor:** IEEE requires a capacitance between 50 nF and 120 nF be present between V_{PP} and VPN_{IN} for a valid detection signature. For best performance and to protect the chip from sharp voltage transients, Microchip recommends using a ceramic capacitor 82 nF to 100 nF per 100 V. It should be located as close as practical to the chip.
- **Input TVS:** If diode bridges are used, for basic protection against basic level voltage transients (<1 kV, both 10x700 µS or 1.2x50 µS, a 58 V TVS (such as SMBJ58A or equivalent) should be connected between V_{PP} pin and VPN_{IN}. If the active bridge PD70224 is used or to meet surge requirements of IEC/EN 61000-4-5 (2014 Ed.3), ITU-T K21, and GR-1089, then refer to Microchip application note AN3410.
- **SUPP_S1 and SUPP_S2 inputs** (PD70211 only): 10 kΩ resistors should be connected in series to each of the input pins SUPP_S1 and SUPP_S2. The signals for these pins come from corresponding pins of the active bridge PD70224, or from an auxiliary rectifier if regular diode bridges are used as shown in the previous figure. These inputs in PD70211 allow setting AT and 4-pair AT flags with some legacy 4-pair midspans that provide only one classification pulse on each pair set. If SUPP_S1 and SUPP_S2 pins left open, the status of the flags in PD70211 are per table Status of PD70211 Flags when SUPP_S1 and SUPP_S2 Pins Not Connected.

Table 2-1. Status of PD70211 Flags when SUPP_S1 and SUPP_S2 Pins Not Connected

Number of Fingers (N-Event Classification)	AT Flag	HDBaseT Flag	4-Pair AT Flag	4-Pair HDBaseT Flag
1	Hi Z	Hi Z	Hi Z	Hi Z
2	0 V	Hi Z	Hi Z	Hi Z
3	0 V	0 V	Hi Z	Hi Z
4	0 V	0 V	0 V	Hi Z
5	0 V	0 V	0 V	Hi Z
6	0 V	0 V	0 V	0 V

- **Power good (PD70201 and PD70101 only):** An open drain power good signal is available at the PGOOD pin. After start-up, a PGOOD flag generates low voltage with respect to VPN_{OUT} to inform the application that the power rails are ready. Pull-up voltage on this pin is limited to V_{PP} voltage for PD70101/PD70201. Power good can also be pulled up by the bootstrap winding output of the DC-DC, in which case it must be isolated via a Schottky diode from V_{AUX} to prevent additional current draw from V_{AUX} during start up.
  If PGOOD is used to start-up an external application, the application must provide 80 ms inrush to operating state delay required by IEEE 802.3.
- **Flags reporting PSE type:** These flags may be sampled by the application to decide upon the maximum power to consume. All these flags are open drain pins. Pull-up voltage on all these pins is limited to 20 V for PD70211, and to V_{PP} voltage for PD70201/PD70101. The flags can be pulled up by the bootstrap winding output of the DC-DC, in which case it must be isolated via a Schottky diode from V_{AUX}. Flags state is set only once at port startup and are asserted with at least 80 ms delay indicating that the application that inrush to operating state delay is over. If SUPP_S1 and SUPP_S2 pins are changing after port turn on, the flags do not change accordingly.
  - **AT_FLAG** (available on PD70211 and PD70201): This flag goes active low when a Type 2 PSE and PD mutually identify each other via classification.
  - **HD_FLAG** (available on PD70211): This flag goes active low when a HDBaseT PSE and PD mutually identify each other via classification.
  - **4P_AT_FLAG** (available on PD70211): This flag goes active low when a 4-pair version of a PSE and PD mutually identify each other via classification.
  - **4P_HD_FLAG** (available on PD70211): This flag goes active low when a 4-pair (Twin) HDBaseT PSE and PD mutually identify each other via classification.
- **V_{AUX} output:** V_{AUX} is a low power regulated output available for use as a start-up supply for an external DC-DC converter controller. After start-up, V_{AUX} must be supported from an auxiliary (bootstrapped) winding of the DC-DC converter. V_{AUX} output requires ceramic capacitor of minimum 4.7 µF to be connected directly between V_{AUX} pin and VPN_{OUT} pin and placed physically close to the device.

3. Using PD70101/PD70201 and PD70211: PWM Controller

The PD70101/PD70201/PD70211 ICs, in addition to providing PD handshake and control functions provide all functions necessary to control both isolated and non-isolated DC-DC topologies, including isolated Flyback and Forward converter topologies, as well as non-isolated Buck and Boost topologies.

The following considerations should be made when using the PD70101/PD70201/PD70211 PWM controller:

- **Frequency setting resistor (R_{FREQ}):** The value of this resistor determines the switching frequency, as well as sets the pin current for both SS and RCLP pins. The value of R_{FREQ} is based on the following equation:
  - Frequency = 1/[(90 pF × R_{FREQ}) + 150 ns], where F is in Hz and R_{FREQ} in Ω
  - Resistor Range = 100 kΩ to 20 kΩ
- **Soft start charge current:** The DC-DC soft start time is determined by the value of the capacitor connected to the SS pin, and the SS pin's charging current. The charging current is calculated:
  - I_{SS_CHG} = 1.2 V/R_{FREQ}
- The time required for soft start to complete is determined by the time required for the SS pin voltage to transition from 0 to 1.1 V (min). This can be calculated with the following equation:
  - T_{SS} = (R_{FREQ} x C_{SS} x 1.1)/1.2
- **Low power mode clamp threshold:** The Low Power Mode Clamp Threshold is set by the resistor connected between RCLP pin (pin 17) and GND. The value is determined by the following equation:
  - V_{CLAMP} = 0.3 x (R_{CLP}/R_{FREQ})

  The clamp voltage determines the threshold below which the DC-DC converter enters low power skip mode (LPM). This threshold is typically set as a percentage of the peak inductor current at maximum output load and minimum input voltage. V_{CLAMP} voltage equates to a percentage of peak current by the following:
  - I_{LPM} = [(0.9 x V_{CLAMP})/1.2] x $I_{PK\ (MAX)}$
  - $I_{PK\ (MAX)}$ = maximum peak inductor current set by the current sense resistor (assumes V_{RCS} = 0.12 V at maximum peak current)

  During start up, it starts with LPM mode until V_{COMP} voltage goes higher than 0.2 V and/or V_{CLAMP} ≤ 1.11 x (V_{COMP}–0.25 V), (V_{COMP} ≥ 0.25 V). Connecting the RCLP pin to ground disables LPM mode during normal operation.
- **VPP UVLO:** The PD70101/PD70201/PD70211 ICs offer a VPP monitoring UVLO function. The UVLO function is dependent on the voltage present at the VINS pin (pin 11), and will switch states based on a 1.2 V threshold. Hysteresis may be programmed in by means of a resistor connected between HYST pin (pin 12) and VINS pin. Components are determined as follows:
  - V_{HYST} = HYST pin output high (5 V typ)
  - V_h = Desired hysteresis
  - V_{RISING} = Upper voltage threshold
  - Set R3 such that (V_{HYST} – 1.2)/R3 ≤ 10 µA
  - R1 = R3 x (V_h/V_{HYST})
  - R2 = 1/[(V_{RISING}/(1.2 x R1)) – (1/R1) – (1/R3)]

  Note: UVLO function set by VINS pin affects only the thresholds of PWM. The UNLO of PD front end is set in the hardware.
- **Complementary gate drivers:** The PD70101/PD70201/PD70211 have two gate drivers that work inversely with a fixed dead time. Primary gate driver (PG) is used to drive the main FET and secondary gate driver (SG) can be used to drive a synchronous FET or an active clamp FET.
- **Differential current sense amplifier (CSP and CSN)** for implementing current mode control and for pulse-by-pulse current limit. Note that the output of the current-sense amplifier is internally amplified by 5 (so a 0.2 V current-sense voltage translates to a 1 V swing at the input of the PWM comparator).
- **Differential-sense voltage amplifier (VSP, VSN)** for implementing feedback in non-isolated applications. The amplifier has gain of 7 and its output (DAO pin) is internally connected to the inverting pin of internal error amplifier, which compares that against a 1.2 V reference.

4. Operation with an External DC Source

PD applications utilizing the PD70211, PD70201, and PD70101 IC provide an external auxiliary power source (DC wall adapter) priority function. In general, there are three methods of providing power with an external source:

- The external source is connected directly to the PD input (V_{PP} to VPN_{IN}). This requires the external source output voltage to be 42 V minimum at no load and more than 36 V at max load. The adapter must be isolated from V_{PP} or VPN_{IN} through an OR-ing diode. This configuration does not provide adapter priority and can be used with PD70211, PD70201, and PD70101.
- The external source is connected directly to PD output (between V_{PP} and VPN_{OUT}). The external source must be isolated from V_{PP} or VPN_{OUT} through an OR-ing diode. For adapter priority, only the PD70211 should be used.
- The external source is connected directly to application's low voltage supply rails (output of DC-DC converter). The external source must be isolated from application power supply's output either through a switched connection, a diode, or a separate regulator that sources current only (does not sink current).

The following figures show examples of PD70211 configured with an external wall adapter. For more details and recommended values of voltage dividers, see AN3472: Implementing Auxiliary Power in PoE.

Figure 4-1. Auxiliary Power Connected to PD70211 Input

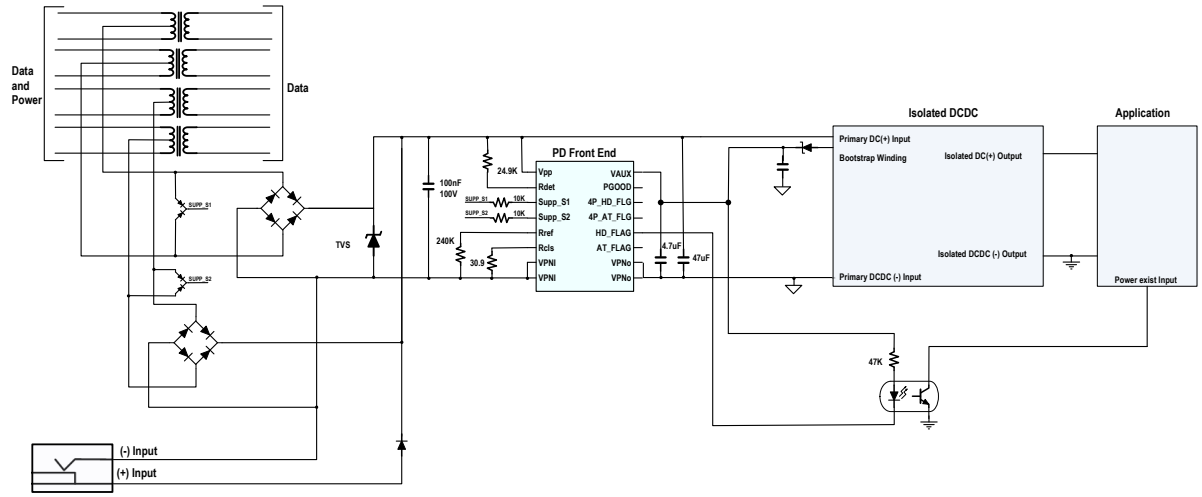


Figure 4-2. Auxiliary Power Connected to PD70211 Output

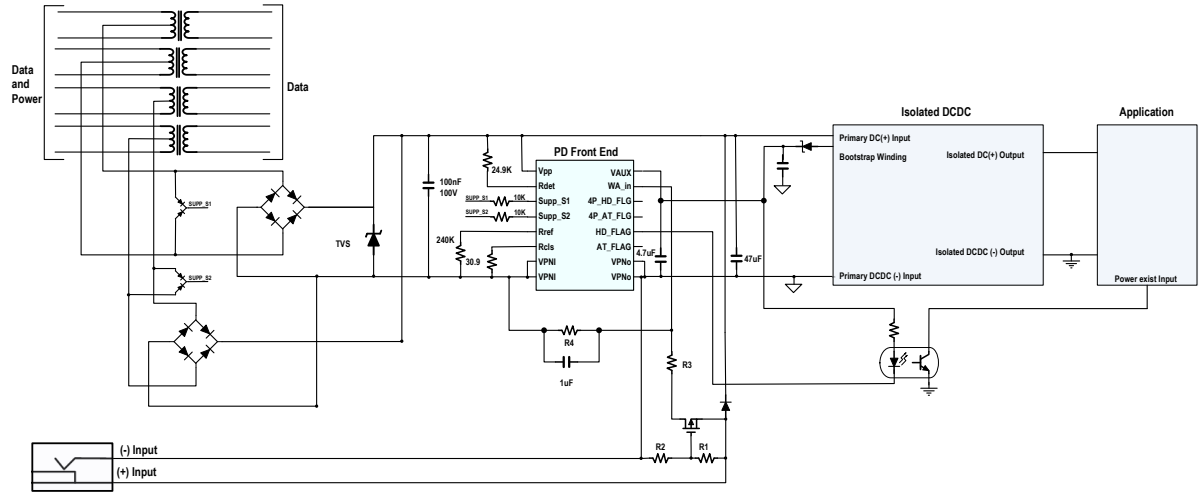
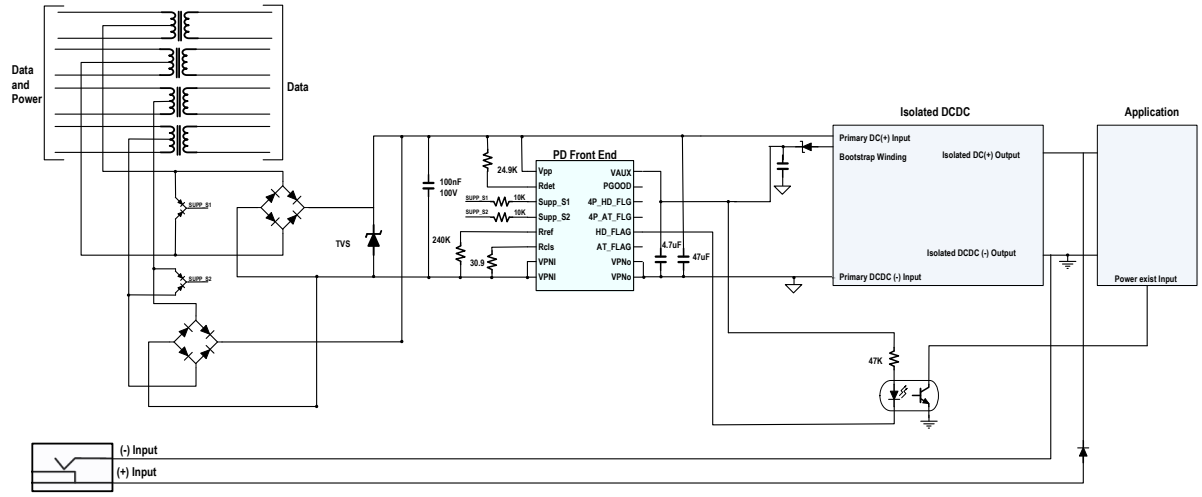


Figure 4-3. Auxiliary Power Connected to Application Supply



5. General Operation Theory

5.1 Event Thresholds

PD ICs switch between different states depending on the voltage between V_{PP} and VPN_{IN} pins.

- **V_{PP}–VPN_{IN}= 1.3 V to 10.1 V (rising voltage):** Detection resistor R_{DET} is connected between V_{PP} and VPN_{IN}.
- **V_{PP}–VPN_{IN}= 10.1 V to 12.8 V (rising voltage):** Detection resistor R_{DET} is disconnected from VPN_{IN}.
- **V_{PP}–VPN_{IN}= 11.4 V to 13.7 V (rising voltage):** Classification current source is connected between V_{PP} and VPN_{IN}. This threshold establishes the programmed current draw set by R_{CLASS}. Current magnitude sets class level per IEEE 802.3at and HDBaseT standards. This function is optional for IEEE 802.3af compliant PDs and mandatory for IEEE 802.3at and HDBaseT compliant PDs. Classification current source remains connected during V_{PP} rising voltage up to 20.9 V.
- **V_{PP}–VPN_{IN}= 20.9 V to 23.9 V (rising voltage):** Classification current source is disconnected. There is some hysteresis between enable and disable thresholds of classification current source.
- **V_{PP}–VPN_{IN}= 4.9 V to 10.1 V (falling voltage):** This is the mark voltage range. IC will recognize V_{PP}–VPN_{IN} voltage falling from classification current source connect threshold to mark threshold as one event of the 2 events classification signature. The number of class to mark level events will cause IC to set the relevant flags to their active low state.
- **V_{PP}–VPN_{IN}= 36 V to 42 V (rising voltage):** Isolation switch is switched from Off state to Inrush Current Limit (Soft Start) mode. In this mode, the isolation switch limits the DC current to 240 mA (typical). The current limit circuitry during soft start mode monitors the voltage difference across the isolation switch (VPN_{OUT}–VPN_{IN}) and maintains inrush current. During inrush current limit internal MOSFET operates in linear mode.

  When VPN_{OUT}–VPN_{IN} drops to 0.7 V or below, isolation switch inrush current limit is disabled, V_{AUX} is enabled, the isolation switch is fully turned on with 2.2 A (max) over current protection and relevant flags are asserted after tFLAG delay, which is minimum 80 ms.
- **V_{PP}–VPN_{IN}= 30.5 V to 34.5 V (falling voltage):** Isolation switch is turned off, establishing high impedance between VPN_{IN} and VPN_{OUT}. Bulk capacitor discharge function is enabled and stays enabled if difference between voltages V_{PP} and VPN_{OUT} remains between 30 V and 7 V. If auxiliary power source is used, its voltage either must be above 34.5 V, or an isolation diode must be added between VPN_{OUT} and the return of auxiliary power source to prevent discharge current flow.
- **V_{PP}–VPN_{IN}= 2.8 V to 4.85 V (falling voltage):** Detection resistor R_{DET} is reconnected at this threshold. R_{DET} is disconnected when V_{PP}–VPN_{IN} voltage drops below 1.1 V.

5.2 Inrush Current Limit

Inrush current limit is necessary for limiting the current during initial charge-up of bulk capacitors upon system start-up and is required by PoE standards. Large inrush currents can create large voltage sags at PI, which in turn can cause system functions tied to event thresholds (such as AT_FLAG) to reset to their initial states. Soft Start current limit will significantly reduce voltage sag upon start-up.

Start-up into a fully discharged bulk capacitor will result in large power dissipation in the isolation switch for a time dependent on the size of the bulk capacitance. Maximum initial voltage drop across isolation switch can be about 42 V. Maximum power dissipated by the isolation switch will decrease as the bulk capacitor charges, eventually decreasing to a normal operating power dissipation when the switch is fully on. The time required to switch from Soft Start mode to normal operation mode can be calculated using the following formula:

$T = ((\Delta V – 0.7) \times C) / I$

Where:

I= IC’s current during soft start (typically 240 mA)

C= Total input bulk capacitance

ΔV= Initial VPN_{OUT}–VPN_{IN} voltage at the beginning of soft start ($\Delta V_{MAX} = V_{PP}$)

Maximum value of bulk capacitor is 240 uF.

5.3 Bulk Capacitor Discharge

PD70211, PD70201, and PD70101 ICs provide discharge of the application bulk capacitor when V_{PP}–VPN_{IN} falling voltage drops below the isolation switch turn-off. This feature ensures that the application bulk capacitance does not discharge through the detection resistor, which can cause detection signature to fail and prevent PSE from starting the PD. While enabled, discharge function provides a minimum controlled discharge current of 22.8 mA, which flows through V_{PP} pin, internally through isolation MOSFET's body diode, and out through VPN_{OUT} pin. Discharge circuitry monitors voltage difference between V_{PP}–VPN_{OUT}, and remains active while difference voltage is 7 V ≤ (V_{PP}–VPN_{OUT}) ≤ 30 V. Use the following equation to calculate maximum time to discharge:

$$T = ((\Delta V - 7V) \times C) / 0.0228$$

Where:

C= Total input bulk capacitance

ΔV= Initial V_{PP}–VPN_{OUT} voltage at isolation switch turn-off

Example: For an initial capacitor voltage of 32 V, it takes 240 ms for a 220 µF capacitor to discharge to a 7 V level.

The discharge operation has a timer and it is active for at least 430 ms.

5.3.1 Auxiliary Voltage—V_{AUX}

All Microchip PD ICs have an available regulated voltage output, V_{AUX}, to be used primarily as a start-up supply for an external DC/DC controller. V_{AUX} is a low current, low duty cycle output, providing current momentarily until an external bootstrap supply can take over. For stable operation connect 4.7 uF or greater capacitor between V_{AUX} and power ground pins.

V_{AUX} output is regulated at nominal 10.5 V and supplies a peak current of 10 mA for 10 ms (5 ms for PD70201/PD70101). Continuous current is 4 mA for PD7021x and 2 mA for PD7020x/PD7010x. Typically, V_{AUX} output is connected to a bootstrapped supply of higher voltage (such as a rectified auxiliary output from an isolated DC/DC converter transformer). V_{AUX} output does not sink current. Once bootstrapped voltage exceeds V_{AUX} output voltage level, V_{AUX} output will no longer provide current and will be transparent to the operation of the DC-DC converter. It is recommended to design the rectified bootstrapped output under all operating conditions for a minimum output voltage of 12.5 V.

During Soft Start mode or when isolation switch turned-off, V_{AUX} output is disabled by falling V_{PP}.

5.3.2 PGOOD Output

PD70201 and PD70101 ICs provide an open drain output indicating power good status. This output asserts active low when the voltage between V_{PP} and VPN_{OUT} reaches approximately 40 V. Upon assertion, PGOOD output switches to ground with a current sink capability of 5 mA. When V_{PP}–VPN_{IN} voltage falls below the isolation switch turn-off threshold, PGOOD output sets back to high impedance state.

This output may be used to detect when PI voltage is in operating range.

PD70211 do not contain PGOOD output. If such functionality is required, V_{AUX} output can be used as an option. If you tie V_{AUX} to the gate of an external small signal N-channel FET, and its source to VPN_{OUT}, the drain of this FET can be used as PGOOD replacement.

6. WA_EN Input (PD70211 Only)

This input pin is used for external power input connection between V_{PP} and VPN_{OUT}.

See figure Auxiliary Power Connected to PD70211 Output.

A resistor divider R1 and R2 is connected between V_{PP} and VPN_{OUT}. These resistors set the P-channel FET turn-on threshold.

A 100 V low signal P-ch FET gate and source should be connected to R1.

The P-ch drain is connected to WA_EN input through R3 resistor. R4 resistor is connected between WA_EN and VPN_{IN}.

R3 and R4 set the level in which a valid WA input is detected.

WA_EN input requires a standard logic level.

When WA_EN input is high, the PD70211 isolation switch is turned off and all the flags are asserted—changed to low level.

The resistor selection guide is specified in application note AN3472: Auxiliary Power for PDs.

6.1 SUPP_S1 and SUPP_S2 Inputs (PD70211 Only)

SUPP_S1 and SUPP_S2 inputs enable the PD to recognize the source of the power whether it is data, spare pairs, or both. Each of these inputs requires a common cathode dual diode to be connected to the relevant pair, if the PD device samples a high level of 35 V and above in this input it counts this pair as an active pair.

These inputs are used when working with special PSE which having detection and classification on two pair only but having the power in all 4 pairs.

SUPP_S1 and SUPP_S2 inputs should have 10 kΩ resistor connected in serial to each of them.

When these functions are not used, the SUPP_S1 and SUPP_S2 pins can be disconnected from external circuits and connected to VPN_{IN} input or left floating.

6.2 PSE Type Flag Outputs

The PD702x1 and PD701x1 ICs provide an open drain outputs indicating the PSE type by its detected Classification pattern. The output is in a high impedance state until the isolation switch moves from Soft Start Current Limit mode to normal operation mode.

It will then be asserted low, depending on the classification pattern that was recognized. Upon assertion, flags output switches to ground with a current sink capability of 5 mA. Flags output signals switch back to high impedance state when V_{PP}–VPN_{IN} voltage falls below isolation switch turn-off threshold.

The flags enable the PD designer to work with the flag that is relevant to the application. For each power that is detected, all the lower power flags are also asserted (IE AT_FLAG is asserted AT level and for all power levels above AT).

The available power level is listed in table Available PD Power Level and Flag Indication. As specified in the table, the PD counts the classification fingers event and by its count recognize the PSE type.

SUPP_S1 and SUPP_S2 enable the PD to recognize a special AT level PSE which having the classification on two pair only but having the power in all 4 pairs. Therefore, if two fingers are recognized, then the PD device samples SUPP_S1 and SUPP_S2 inputs and if both are high, then the power is supplied to the 4 pairs and 4P_AT flag is asserted.

Table 6-1. Available PD Power Level and Flag Indication

Number of Class Fingers	SUPP_S1	SUPP_S2	PGOOD_ FLAG	AT_ FLAG	HD_ FLAG	4P_AT_ FLAG	4P_HD_ FLAG	Available Power Level
1	X	X	0 V	Hi Z	Hi Z	Hi Z	Hi Z	802.3 AF level/ 802.3 AT Type 1 level
2	H	L	0 V	0 V	Hi Z	Hi Z	Hi Z	802.3 AT Type 2 level
2	L	H	0 V	0 V	Hi Z	Hi Z	Hi Z	802.3 AT Type 2 level
2	H	H	0 V	0 V	Hi Z	0 V	Hi Z	Dual 802.3 AT Type 2 level
3	L	H	0 V	0 V	0 V	Hi Z	Hi Z	HDBaseT Type 3 level
3	H	L	0 V	0 V	0 V	Hi Z	Hi Z	HDBaseT Type 3 level
3	H	H	0 V	0 V	0 V	0 V	Hi Z	HDBaseT Type 3 level
4	X	X	0 V	0 V	0 V	0 V	Hi Z	Dual 802.3 AT Type 2 level
5	X	X	RESERVED FOR FUTURE					NA
6	X	X	0 V	0 V	0 V	0 V	0 V	Twin HDBaseT Type 3 level

7. Thermal Protection

The PD702x1 and PD701x1 ICs provide thermal protection. Integrated thermal sensors monitor the internal temperatures of the isolation switch and classification current source. If the over-temperature threshold of either sensor is exceeded, that sensor's respective circuit will disable.

To ensure trouble free operation, it is important to make sure PD IC's exposed pad is mounted to a copper area on the PCB that provides an adequate heat sink.

8. PCB Layout Guidelines

IEEE 802.3at and HDBaseT standards specify certain isolation requirements which must be met by all PoE equipment. Isolation is specified at 1500 V_{RMS} minimum between incoming data and power lines, and any signal, power, or chassis connection that can come into contact by the end user outside the application. On a typical FR4 PCB, this requirement is generally satisfied by creating an isolation barrier of a minimum 0.080 inch (2 mm) between adjacent traces requiring 1500 V_{RMS} isolation.

Give the PCB design special attention to provide adequate heat sinking of the exposed pad (VPN_{OUT}). All Microchip PD IC packages utilize the exposed pad to provide thermal cooling of the package, and as such requires PCB design to include sufficient copper area attached to the exposed pad. For multilayer boards, conductive vias to an adjacent plane layer may be used. Keep in mind that exposed pad is electrically connected to VPN_{IN} and must be electrically isolated from VPN_{OUT}.

When using vias to provide thermal conductivity between a plane layer and exposed pad, barrels should be 12 mils in diameter and (where possible) placed in a grid pattern. Barrel holes should be plugged or tented for proper solder paste release. When tented holes are used, solder mask inclusion area should be 4 mils (0.1 mm) larger than via barrel.

For single or dual layer boards, use large copper fills in direct contact with the exposed pad. Copper thickness of 2 oz will improve thermal performance. If using copper traces of less than 2 oz, it is recommended to increase overall trace thickness by adding excess solder to trace areas where appropriate.

PCB design should provide wide, heavy copper traces for high current power lines. A 4-pair, extended-power PD can have maximum trace currents of 2 A for the V_{PP} and VPN terminals. Traces carrying current for V_{PP}, VPN_{IN}, and VPN_{OUT} should be sized to provide the lowest temperature rise practical at the maximum current. For example, a minimum of 15 mils wide 2 oz copper will accommodate up to 1.6 A current with a maximum 10 °C temperature rise. If using copper traces of less than 2 oz, increase the minimum width to accommodate maximum current with lowest temperature rise.

PoE signals contain voltages up to 57 V_{DC}. Component working voltage must be considered, and components sized accordingly. Surface mount resistors are a good example: 0402 and 0603 resistors have typical maximum working voltage specifications of 50 V, whereas 0805 resistors are typically specified at 150 V.

When used with the PD702x1 and PD701x1 ICs, the detection resistor R_{DET} is only connected at PoE voltages up to 12.8 V, and is disconnected otherwise, so it may be a low voltage type (0402 or 0603).

For details on PCB layout, see AN222 PD70210(A), PD70211 System Layout Guidelines and AN208 PD70101A/ PD70201 PD device Layout Guidelines.

9. Design Example

This section describes a design example for a 47 W DC-DC flyback converter using the PD70201 IC. A schematic and parts list of the 47 W example can be found in figure PD70201 Design Example (12 V, 47 W).

9.1 Design Requirements

Vmin := 32	Minimum Input Voltage
Vmax := 57	Maximum Input Voltage
Vout := 12	Output Voltage
Pout := 48	Maximum Output Power
Eff := .90	Estimated Efficiency
Fsw := 200k	Switching Frequency
Vaux := 12	Auxillary Output Voltage
Tamb := 70	Ambient Operating Temperature

Flyback operation in DCM is best for output power less than 20 W. Therefore, the design will be a CCM design.

9.2 Estimated Secondary Diode Drop

Synchronous rectification is used in place of a blocking diode; choose FDMS86322 N-FET.

Sync Transistor: FDMS86322; RDSon = 0.008 at 25°C

$$Iout := \frac{Pout}{Vout} \qquad Iout = 4$$

Kt := 1.58 Multiplier for 100°C

rdson := 0.008·Kt

ddrop := Iout·rdson ddrop = 0.051

9.3 Transformer Turns Ratio

Transformer turns ratio is driven by V_{MIN}, V_{OUT}, the secondary diode drop, and the controller's maximum duty cycle. Per the datasheet, maximum duty cycle for the PD70201= 46%.

Dmax := 0.46

$$Tratio := \frac{Vout + ddrop}{Dmax \cdot Vmin} - \frac{Vout + ddrop}{Vmin}$$

Tratio = 0.442 Secondary to Primary (Ns/Np) Turns Ratio

For this design, we will increase the turns ratio to 0.444. 0.444 gives a Np/Ns turns ratio of 2.25:1, a more practical value.

9.4 Required Primary Inductance

Minimum required primary inductance is based on the desired ripple factor (Krf), which is defined as the percentage of peak-to-peak inductor ripple current versus inductor average current. This number sets the point in which the primary inductance changes from CCM to DCM operation. A good rule of thumb is to set this number between 0.5 to 1.4. For this design, we will set it to 0.7.

$Krf := 0.7$ Krf is the ratio of inductor ripple to inductor average current

$$Lpri := \frac{Eff \cdot Vmin^2 \cdot \left(\frac{Vout + ddrop}{Tratio}\right)^2}{Krf \cdot Fsw \cdot Pout \cdot \left[Vmin + \left(\frac{Vout + ddrop}{Tratio}\right)\right] \cdot \left[\left(\frac{Vout + ddrop}{Tratio}\right) + Eff \cdot Vmin\right]}$$

$Lpri = 3.054 \times 10^{-5}$

Nominal Primary Inductance (allows for +/- 15%):

$Lnom := Lpri \cdot 1.15$ $\quad Lnom = 3.512 \times 10^{-5}$

9.5 Transformer Primary/Secondary Currents

Average Input Current:

$$Iinavg := \frac{Pout}{Eff \cdot Vmin} \qquad Iinavg = 1.667$$

Average Primary Current:

$$Ipriavg := \frac{Iinavg}{Dmax} \qquad Ipriavg = 3.623$$

Primary Ripple:

$$Ipriripple := Ipriavg \, Krf \qquad Ipriripple = 2.536$$

Peak Primary Current:

$$Ipripk := \frac{Ipriripple}{2} + Ipriavg \qquad Ipripk = 4.891$$

Primary Circuit RMS Current:

$$Iprirms := \sqrt{Dmax \cdot \left[Ipripk^2 - (Ipripk \cdot Ipriripple) + \frac{Ipriripple^2}{3}\right]}$$

$Iprirms = 2.507$

Secondary Circuit RMS Current:

$$Isecpk := \frac{Ipripk}{Tratio} \qquad Isecpk = 11.016$$

$$Isecrms := \sqrt{(1 - Dmax) \cdot \left[Isecpk^2 - \left(Isecpk \cdot \frac{Ipriripple}{Tratio}\right) + \frac{Ipriripple^2}{Tratio^2 \cdot 3}\right]}$$

$Isecrms = 6.118$

9.6 Transformer Specifications

Based on the calculations above, the following can be given to a transformer manufacturer for transformer fabrication.

Primary Voltage Range:

$\underline{Vmin} = 32$

$\underline{Vmax} = 57$

Secondary Voltage & Power:

$\underline{Vout} = 12$ $\underline{Pout} = 48$

Auxilliary Voltage & Power:

$\underline{Vaux} = 12$ Paux = 1.2

$\underline{Fsw} = 2 \times 10^{5}$ Switching Frequency

$$\underline{Dmin} := \frac{\underline{Vout} + \underline{ddrop}}{\underline{Vout} + \underline{ddrop} + \underline{Tratio} \cdot \underline{Vmax}} \qquad \underline{Dmin} = 0.323$$

Maximum Primary Operating Volt-Seconds:

$$\underline{Vsecmax} := \frac{\underline{Dmin} \cdot \underline{Vmax}}{\underline{Fsw}} \qquad \underline{Vsecmax} = 9.193 \times 10^{-5}$$

Open Circuit Primary Inductance (+/- 15%):

$\underline{Lnom} = 3.512 \times 10^{-5}$

Turns Ratio:

$$\underline{Naux} := \frac{\underline{Vaux}}{\underline{Vout}}$$ Turns Ratio Calculation for Aux Winding

Nsec/Npri: $\underline{Tratio} = 0.444$ Npri/Nsec: $\frac{1}{\underline{Tratio}} = 2.252$

Naux/Nsec: $\underline{Naux} = 1$

Winding Currents:

$\underline{Iprirms} = 2.507$ $\underline{Ipriavg} = 3.623$

$\underline{Ipripk} = 4.891$ $\underline{Isecrms} = 6.118$

9.7 Primary Clamp Equations

The maximum transformer primary voltage seen across the V_{DS} of the primary transistor during the off period will be greater than the maximum input voltage by a factor of the secondary voltage reflected by the transformer's turns ratio *plus* the voltage generated by the leakage inductance of the primary. Because of this, a suitable clamp is required to insure the primary voltage does not exceed the transistor's maximum V_{DS}. There are many types of clamps available to the designer; each has its merits and drawbacks. For this design, the more common RCD clamp will be used. An example of an RCD clamp is outlined in figure PD70201 Design Example (12 V, 47 W).

The first step is to select a maximum V_{DS} transistor rating. The reflected voltage is found:

Reflected Mosfet Drain Voltage:

$$Vd := \left(\frac{Vout + ddrop}{Tratio}\right) + Vmax \qquad Vd = 84.141$$

Vd= Reflected voltage across transistor

Based on the above equation, the transistor selection will need to have a V_{DS} rating considerably larger than 85 V. 100 V does not leave margin for voltage overshoot, and would require significant power loss to achieve, so a 150 V transistor will be used.

Next, the maximum clamp voltage and a clamping coefficient is calculated using the chosen V_{DS} rating derated by 15%. The clamping coefficient is simply the following ratio.

Clamp Voltage Limit (with BVdss derated):

$$Vclamp := BVdss \cdot 0.85 - Vd \qquad Vclamp = 43.359$$

Clamp Coeffient based on selected Turns Ratio:

$$Kccalc := \frac{Tratio \cdot Vclamp}{(Vout + ddrop)} \qquad Kccalc = 1.598$$

Maximum Transistor Stress Voltage:

$$Vstress := Vd + Vclamp \qquad Vstress = 127.5$$

$$BVdss \cdot 0.85 = 127.5$$

Using leakage inductance estimated at 1% of the primary inductance, and the values calculated above, the final RC values are calculated as follows.

Estimated Leakage Inductance:

$Lleak := Lnom \cdot 0.01$ Leakage is set at 1% of total primary inductance

Clamp Voltage Limit:

$Vclamp = 43.359$

Desired Clamp Capacitor Ripple Voltage:

$$Vcripple := Vclamp \cdot 0.1$$

Clamp Coefficient:

$$Kccalc = 1.598$$

Resistor Calculation:

$$Rclmp := \frac{(Kccalc - 1)\cdot\left[2\cdot Kccalc\cdot(Vout + ddrop)^2\right]}{Tratio^2\cdot Fsw\cdot Lleak\cdot Ipripk^2}$$

$$Rclmp = 837.011$$

Resistor Power Dissipation:

$$Prclmp := 0.5\cdot Fsw\cdot Lleak\cdot Ipripk^2\cdot\frac{Kccalc}{Kccalc - 1}$$

$$Prclmp = 2.246$$

Capacitor Calculation:

$$Cclmp := \frac{Kccalc\cdot(Vout + ddrop)}{Tratio\cdot Rclmp\cdot Fsw\cdot Vcripple}$$

$$Cclmp = 5.974\times 10^{-8}$$

Clamp Current Calculation:

$$Trst := \frac{Tratio\cdot Lleak\cdot Ipripk}{Tratio\cdot Vclamp - (Vout + ddrop)}$$

Leak L Reset Time: $Trst = 1.059\times 10^{-7}$

$$Iclmprms := Ipripk\cdot\sqrt{\frac{Trst\cdot Fsw}{3}}$$

$$Iclmprms = 0.411$$

Based on the above equations, the clamp resistor will need to be 3 × 2.7K Ω, 1 W 5% resistors in parallel. The capacitor will need to be a .068 µF, 100 V capacitor.

Using the clamp current and maximum stress voltage, the diode is selected. A fast diode is desired.

$$Vstress = 127.5$$

$$Iclmprms = 0.411$$

A 200 V, 1 A ES1D diode is selected.

Note: The above component selections will require final tweaking at the prototype stage.

9.8 Primary FET Requirements

The primary FET is chosen based on maximum primary RMS current, and maximum V_{DS} stress.
Note: The maximum stress has already been accounted for. We chose a 150 V FET based on the primary RMS current and RDSon.

Iprirms = 2.507

A FDMS86200 FET by Fairchild has a V_{DS} rating of 150 V, maximum continuous I_{DS} rating of 9.6 A, and a specified RDSon of 18 mΩ at 25 °C.

9.9 Primary FET Power Dissipation

Selected Transistor: FDMS86200

Chosen RDSon (at 100°C): RDSon := .03

Chosen θja: θja := 50

Chosen Ambient T: Tamb = 70

Chosen Max. Junction T: Tj := 100

Transistor BVdss: BVdss = 150

Transistor Power Limit:

$$Plimit := \frac{Tj - Tamb}{\theta ja} \qquad Plimit = 0.6$$

Transistor Qgs2: Qgs := 2.9n

Transistor Qgd: Qgd := 7.7n

Transistor gate resistance: Rg := 1.2

Transistor gate voltage at start of miller effect: Vgsmiller := 3.9

Transistor gate threshold voltage: Vth := 2.5

Transistor gate drive max voltage: Vcc := 12

Gate drive on resistance: Rhi := 10

Gate drive off resistance: Rlo := 5

Rising Gate Current and Turn-on Time:

$$Ig1 := \frac{Vcc - [0.5 \cdot (Vgsmiller + Vth)]}{Rhi + Rg} \qquad Ig1 = 0.78571$$

$$Ig2 := \frac{Vcc - Vgsmiller}{Rhi + Rg} \qquad Ig2 = 0.72321$$

$$\Delta ton := \frac{Qgs}{Ig1} + \frac{Qgd}{Ig2} \qquad \Delta ton = 1.43378 \times 10^{-8}$$

Falling Gate Current and Turn-off Time:

$$Igf1 := \frac{Vcc - [0.5\cdot(Vgsmiller + Vth)]}{Rlo + Rg} \qquad Igf1 = 1.41935$$

$$Igf2 := \frac{Vcc - Vgsmiller}{Rlo + Rg} \qquad Igf2 = 1.30645$$

$$\Delta toff := \frac{Qgs}{Igf1} + \frac{Qgd}{Igf2} \qquad \Delta toff = 7.93701\times 10^{-9}$$

Valley Current:

$$Ivalley := Ipriavg - \frac{Ipriripple}{2} \qquad Ivalley = 2.30496$$

Operational Primary RMS Current:

$$Iprirms = 2.48022$$

Conduction Loss:

$$Pcond := Iprirms^2\cdot RDSon \qquad Pcond = 0.18454$$

Turn On Switch Loss:

$$Pswon := \frac{Ivalley\cdot\left(Vmin + \frac{Vout + ddrop}{Tratio}\right)\Delta ton}{6}\cdot Fsw$$

$$Pswon = 0.06515$$

Turn Off Switch Loss: $\qquad Vclamp = 43.3591$

$$Pswoff := \frac{Ipripk\cdot(Vmin + Vclamp)\cdot\Delta toff}{2}\cdot Fsw \qquad Pswoff = 0.28634$$

Total Power Loss:

$$Plosstot := Pcond + Pswon + Pswoff \qquad Plosstot = 0.53603$$

In the preceding calculations, RDSon is derated at 100 °C. Values for Vth, Qgd, and Rg are available in most MOSFET datasheets. Qgs2 is the switching gate charge; if not specified, it may be estimated using the Vgs vs Gate charge graph (found in all MOSFET datasheets) by determining the equivalent charge between Vth and Vgsmiller.

9.10 Synchronous FET Requirements

The output synchronous FET is chosen by calculating the maximum DS voltage created during the primary on time (sync FET is off), and the maximum secondary RMS current. To derate the FET, DS voltage is increased by 30% and DS current is increased by 50% for proper FET selection.

Maximum Primary Reflected Voltage across FET:

$$Vsecref := Vmax\cdot Tratio + Vout \qquad Vsecref = 37.308$$

$$Vsecref\cdot 1.3 = 48.5$$

Maximum FET Current (de-rated):

$$Irect := Isecrms\cdot 1.5 \qquad Irect = 9.177$$

A FET is chosen with a V_{DS} of 60 V or higher, and a current capability of 9 A or greater. Chosen is the FDMS86322. This FET has an RDSon (25 °C) of 0.007 at 13 A, and a maximum V_{DS} of 80 V.

9.11 Synchronous FET Power Dissipation

ddropcalc := Isecrms·rdson

ddropcalc = 0.077 Voltage drop across the transistor

rdson = 0.013 Rdson at 100°C

Rectifier Power Loss:

Prect := Isecrms·ddropcalc Prect = 0.473

Rectifier Junction Temp:

Tamb = 70

Thetajarect := 50 Package theta ja

Jtrect := Thetajarect·Prect + Tamb Jtrect = 93.654

9.12 Sense Resistor Calculation

The sense resistor is chosen based on the maximum peak current expected, and the voltage threshold where the controller starts to limit current. For the PD70201, the current limit threshold voltage is 1.2 V with a gain of 5 current sense amplifier, so the resistor is sized such that the operating peak primary current develops at approximately 90% of this value. 1.1 V is approximately 90% of 1.2 V.

Vthreshold := 1.1

Sense Resistor Value (accounts for X5 gain):

$$Rsns := \frac{Vthreshold}{Ipripk \cdot 5} \qquad Rsns = 0.04596$$

$$Prsns := Iprirms^2 \cdot Rsns \qquad Prsns = 0.2827$$

The above takes into account Av = 5 for the current sense amplifier.

A 47 mΩ, ½ W resistor will meet the requirement.

9.13 Output Capacitor Calculation

The output filter capacitor is chosen based on the desired output voltage ripple, output voltage undershoot (droop) during load step, and the RMS ripple current the capacitor must endure.

Desired Output Ripple: $Vripple := 0.1$

Desired Closed-Loop Bandwidth: $Fc := 4k$

Desired Output Droop Load Step: $Vdroop := 0.6$

Load Step: $Istep := Iout \cdot 0.9$

$Isecpk = 11.016$

$Ioutavg := \frac{Iinavg}{Tratio}$ $Ioutavg = 3.754$

$Isecrms = 6.118$

$Icoutrms := \sqrt{Isecrms^2 - Ioutavg^2}$ $Icoutrms = 4.831$

$Cesr := \frac{Vripple}{Isecpk}$ $Cesr = 9.077 \times 10^{-3}$

$Cout := \frac{Istep}{2 \cdot \pi \cdot Vdroop \cdot Fc}$ $Cout = 2.387 \times 10^{-4}$

Chosen Output Capacitor:

$Coutact := 360u$

$Cesract := 0.008$

For the output capacitor, we will choose 2x Sanyo OSCON 25SVPF180M capacitors in parallel. These are 180 µF, 25 V capacitors with an ESR of 16 mΩ and a maximum ripple capability of 4.65 A_{RMS}.

9.14 Input Filter Calculation

The input filter is used to reduce the voltage fluctuations seen at the DC-DC converter input due to the large peak currents involved. There are several approaches to providing an input filter; the input filter can consist of a simple input capacitor (usually several capacitors in parallel due to the large ripple currents), or can be a more complex LC filter. For this design, we will choose an LC filter as our input filter. The input to the LC filter will be a common aluminum electrolytic; the output of the LC filter will consist of smaller ceramic capacitors to absorb the ripple current.

Our design requires the ripple voltage on V_{PP} to be 50 mV or less. We will first choose a suitable ripple voltage at the primary, and then size the input capacitor to achieve that ripple voltage. The input capacitor will need to absorb most of the primary ripple current, so its ripple handling capability is critical. Ceramic capacitors have very good ripple current capability and are a good choice for the input capacitor for this design.

First, we determine the maximum ripple current seen by the capacitor, and use this current to select a suitable input capacitor based on our selected primary ripple of 320 mV:

$Vinripple := 0.32$

$Cinputrms := \sqrt{Iprirms^2 - Iinhigh^2}$

$Cinputrms = 1.873$

$Cmin := \frac{Cinputrms \cdot Dmax}{Fsw \cdot Vinripple}$ $Cmin = 1.34888 \times 10^{-5}$

For this design, we choose 4x 4.7 µF, 100 V ceramic capacitors in parallel. 4 capacitors are chosen to account for capacitor tolerance variation. The ceramic capacitors chosen (1812 case size) have a ripple capability at 100 kHz of greater than 2 A for a 20 °C case temperature rise.

The capacitors chosen will meet more than this requirement.

Next, we determine the voltage developed across our chosen input

$Cminact := 15u$ Actual capacitance - 20% tolerance

$Cinesr := 1.2m$

$$deltavin := \frac{Cinputrms \cdot Dmax}{Fsw \cdot Cminact} + Ipriavg \cdot Cinesr$$

capacitors: $deltavin = 0.29202$

Next, we chose an inductor based on the desired attenuation. For this design, we will attenuate the input current by 40 dB:

Filter Attenuation Desired:

$A := 0.01$

Filter Cutoff Frequency for Required Attenuation:

$Fo := \sqrt{A} \cdot Fsw$ $Fo = 2 \times 10^{4}$

Required Lin vs Cin:

$$Lin1 := \frac{1}{4\pi^{2} \cdot Fo^{2} \cdot Cminact}$$ $Lin1 = 4.22172 \times 10^{-6}$

$InputfilterIrms := A \cdot Cinputrms$ $InputfilterIrms = 0.01837$

For this design we use a 4.7 µH inductor. This inductor must handle the maximum Primary RMS current at low line, and should be sized with a minimum DCR to increase efficiency.

Finally, we must check our filter for stability. For the filter to be stable, the filter output impedance must be less than the input impedance of the DC-DC converter. The input impedance is calculated at DC for a first order check. The filter output impedance is compared at two frequency points: DC (which is simply the DCR of the inductor), and at the resonant point where peaking occurs due to the filter Q:

$$Zinsmpsdc := \frac{Vmin^{2} \cdot Eff}{Pout}$$

$Zinsmpsdc = 19.2$ Converter Input Impedance at DC

$Zoutfilterdc := DCR$ Filter Output Impedance at DC

$Zoutfilterdc = 0.045$

Filter Output Impedance at resonant point:

$$Zoutfiltermax := \sqrt{\frac{(Cinact \cdot ESR^{2} + Linact) \cdot (Cinact \cdot DCR^{2} + Linact)}{Cinact^{2} \cdot (ESR + DCR)^{2}}}$$

$Zoutfiltermax = 6.804$

The calculated output impedance of our filter at DC is 45 mΩ; at the resonant point it is 6.8 Ω. Both these values are less than the Converter DC input impedance of 19.2 Ω; our filter values will not cause stability issues.

9.15 Control Loop Calculations

Control loop calculations are made by determining the modulator and filter gain and phase at the desired crossover frequency, and then selecting feedback components to increase (or decrease) the gain for unity gain at the crossover point. First, the modulator and filter must be evaluated to determine the frequency location of the Right Hand Plane Zero (inherent in CCM flyback designs), and assure that the chosen crossover frequency is less than 20% of that frequency:

Calculation of Right Hand Plane Zero:

$$Rload := \frac{Vout}{Iout}$$

$$Fzrhp := \frac{(1 - Dmax)^2 \cdot Rload}{2\pi \, Dmax \cdot Lnom \cdot Tratio^2} \qquad Fzrhp = 4.372 \times 10^4$$

$Fzrhp \cdot 0.2 = 8.744 \times 10^3$ This number must be greater than the proposed crossover frequency.

Our proposed crossover frequency is 4 kHz; we have plenty of margin.

The modulator and filter gain-phase of our regulator utilizes the following transfer function:

$$Kcc := \frac{Ipripk}{1.2}$$ Current Control Factor

$$\omega z1 := \frac{1}{Cesract \cdot Coutact}$$ Capacitor ESR zero

$$\omega z2 := \frac{(1 - Dmax)^2 \cdot Rload}{Dmax \cdot Lnom \cdot Tratio^2}$$ RHP zero

$$\omega p := \frac{(1 + Dmax)}{Rload \cdot Coutact}$$ Load pole

$$Vro := \frac{Dmax}{1 - Dmax} \cdot Vmin$$ Reflected output voltage

$$H(s) := \frac{Kcc \cdot Rload \cdot Vmin \cdot Tratio^{-1}}{2 \cdot Vro + Vmin} \cdot \frac{\left(1 + \frac{s}{\omega z1}\right) \cdot \left(1 - \frac{s}{\omega z2}\right)}{1 + \frac{s}{\omega p}}$$

Solving for H at the crossover frequency:

$$Gxo := 20 \cdot \log\left(\left|H(2 \cdot \pi \cdot i \cdot Fc)\right|\right)$$

$Gxo = -5.179$ Gain at crossover point (dB)

$$Pxo := \arg(H(2 \cdot \pi \cdot i \cdot Fc)) \cdot \frac{180}{\pi}$$

$Pxo = -88.008$ Phase shift at crossover point (Degrees)

Once the gain and phase are known, the loop must be closed such that the gain at the crossover frequency is equal to 1 (0 dB), and the phase margin is greater than 45°.

In most isolated designs, the feedback loop is closed by means of an optocoupler that bridges the primary/secondary isolation barrier. The optocoupler is chosen to account for the isolation requirements and the input/output current gain (noted as a percentage, “CTR”, which translates to the percentage of input LED current transferred to the output). For our design, the optocoupler will drive the PD70201’s COMP pin directly. The optocoupler components are selected as follows:

Optocoupler Calculations:

$Vf := 1$ Optocoupler: NEC PS2711-1-M-A

$Vdd := 5.0$ Vdd = PD70201's VL typical output voltage

$Rpullup := 1k$ Rpullup added to increase Optocoupler pole frequency

$Vcesat := 0.3$

$Tf := 5u$ These values are fall time test conditions found in the datasheet; used for estimating the pole capacitance; Tf = fall time, Rl = test load.

$Rl := 100$

$CTRmax := 2.00$

$CTRmin := 1.00$

$$Ioptomin := \frac{Vdd - 1.2}{Rpullup} \qquad Ioptomin = 3.8 \times 10^{-3}$$

$$Ioptomax := \left(\frac{Vdd - Vcesat}{Rpullup}\right) + 500u \qquad Ioptomax = 5.2 \times 10^{-3}$$

Ioptomin assumes 1.2 max regulation input for PD70201; Ioptomax adds maximum Error Amp Comp pin current capability.

Optoisolator Characteristic Pole Capacitor:

$$Cpole := \frac{Tf}{2.2 \cdot Rl} \qquad Cpole = 2.273 \times 10^{-8}$$

$$\omega popto := \frac{1}{Rpullup \cdot Cpole} \qquad fpopto := \frac{\omega popto}{2 \cdot \pi} = 7.003 \times 10^{3}$$

$$Iledmin := \frac{Ioptomin}{CTRmax} \qquad Iledmin = 1.9 \times 10^{-3}$$

On the secondary side, the optocoupler must be driven with an error amplifier that regulates the output voltage. Most designs utilize a common TL431 shunt regulator, due to its ability to regulate without requiring additional input power for operation. The compensation components, as well as the DC setting resistors will be placed around the TL431.

First, the DC setting resistors are calculated:

TL431 Calculations:

Reference Resistors:

$Vref := 2.5$

$Iref := 4u$

$Iresistordivider := 1m$

$Rlowercalc := \frac{Vref}{Iresistordivider}$ $Rlowercalc = 2.5 \times 10^{3}$

$Rlower := 2.49k$ Actual resistor used

$Ruppercalc := \frac{(Vout - Vref)}{Iresistordivider + Iref}$ $Ruppercalc = 9.462 \times 10^{3}$

$Rupper := 9.53k$ Actual resistor used

$Voutcalc := \left(\frac{Vref}{Rlower} + Iref\right) \cdot Rupper + Vref$ $Voutcalc = 12.106$

Next, the compensation components are selected:

431 Compensation (Type Two):

$Gxo = -5.179$ Modulator and Filter gain at Fc (dB)

$$Gc := 10^{\left(\frac{Gxo}{20}\right)}$$

$Gc = 0.551$ Modulator and Filter gain at FC (mag)

$G431 := \frac{1}{Gc} = 1.815$ Required feedback gain

$fz431 := 54$ Compensation Zero; set to 1/4 Load Pole

$fp431 := 14k$ Compensation Pole; set to 1/4 ESR zero

$Ibias := 2m$ 431 bias for regulation

$CTRtyp := 1.5$ Optoisolator CTR typical

$$Rledcalc := \frac{CTRtyp \cdot Rpullup}{G431}$$

$Rledcalc = 826.267$ LED Resistor

$$Czcalc := \frac{1}{2 \cdot \pi \cdot Rupper \cdot fz431}$$

$Czcalc = 3.093 \times 10^{-7}$ Calculated Zero Capacitor

$$Cpcalc := \frac{1}{2 \cdot \pi \cdot Rpullup \cdot fp431}$$

$Cpcalc = 1.137 \times 10^{-8}$ Calculated Pole Capacitor

$Cpole = 2.273 \times 10^{-8}$ Optoisolator Pole Capacitor

Actual Compensation Values Used:

$Rled := 825$

$Cz := 330n$ If Cpole less than 5x Cpcalc, use Cpole in the Transfer Function

$Cp := 22.7n$

Finally, the chosen values are used in the TL431/optocoupler Transfer Function:

TL431/Optoisolator Transfer Function:

$$G(s) := -\left(\frac{s \cdot Rupper \cdot Cz + 1}{s \cdot Rupper \cdot Cz}\right) \cdot \left(\frac{1}{1 + s \cdot Rpullup \cdot Cp}\right) \cdot \frac{Rpullup}{Rled} \cdot CTRtyp$$

Bias Resistor:

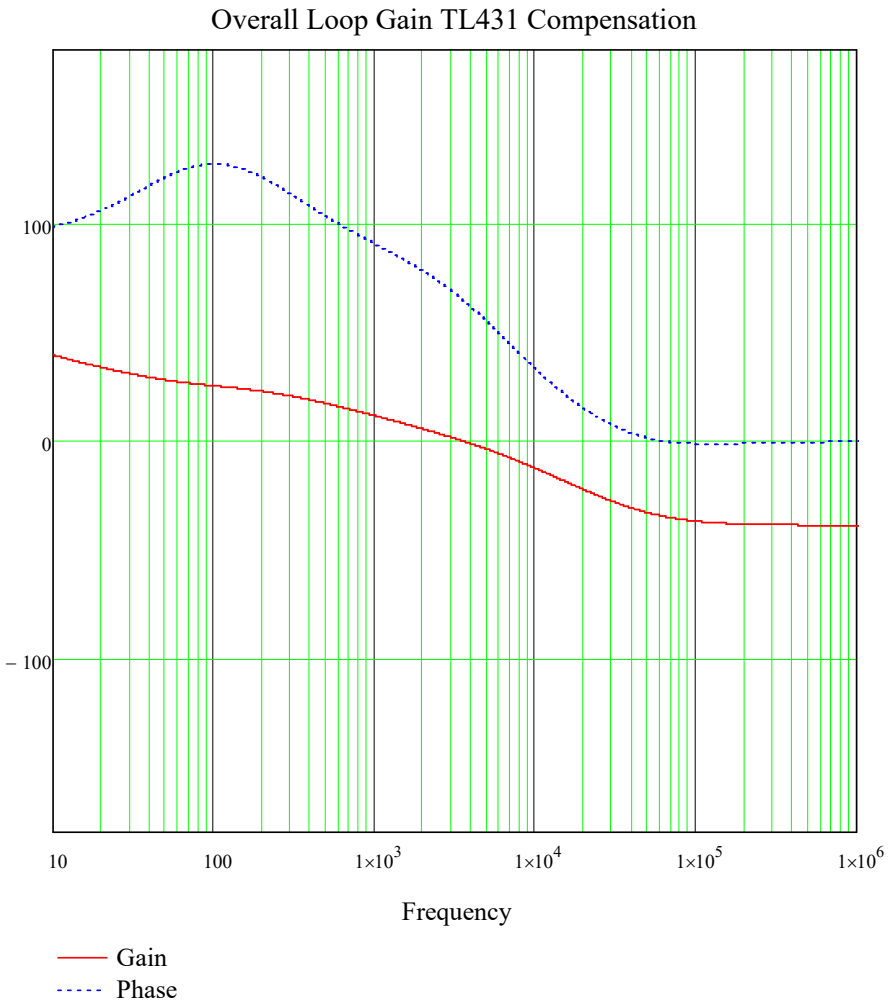
$$Rbias := \frac{Rled \cdot lledmin + Vf}{Ibias}$$

$Rbias = 1.284 \times 10^{3}$

The two functions are multiplied together to achieve the overall loop gain:

$$Gtot431(s) := H(s) \cdot G(s)$$

Figure 9-1. Loop Bode Plot



9.16 Synchronous Gate Drive

The PD70101/PD70201 IC provides a dedicated output driver for a Synchronous FET. This output is available on the SG pin (pin 25) To adhere to the isolation requirements, the SG output is transformer coupled to the Synchronous FET. A coupling capacitor is required in series with the primary to reset the magnetizing inductance. The transformer will saturate without it. The LC tank circuit formed by the coupling capacitor and the transformer magnetizing inductance can generate oscillations during sudden changes in duty cycle. A damping resistor in series with the coupling capacitor should be used to damp oscillations. On the secondary side, a DC restoration and fast gate turn-off circuits are provided to keep the gate drive voltage constant over varying duty cycle, and to insure fast transistor turn off.

As shown in figure PD70201 Design Example (12 V, 47 W), DC restoration is provided via Capacitor C20 and Diode D7. The fast turn-off circuit consists of R14, Q3, and D6. Resistor R19 limits the synchronous MOSFET's turn-on rate of rise, and is optional (can be used to limit EMI).

When selecting the components for the synchronous FET gate drive, first the transformer should be selected based on the maximum volt-microseconds of the SG pin drive output.

Maximum volt-microseconds is calculated:

$VCCmax := 15$

$Dmin = 0.323$ Duty Cycle at High Line

$$Vgdusecmax := \frac{(1 - Dmin)\cdot VCCmax}{Fsw} \qquad Vgdusecmax = 5.081\times 10^{-5}$$

Because of the capacitor in series with the primary, the drive voltage is bipolar. The calculated maximum volt-microsecond value may be divided by 2 for transformer selection due to the bipolar drive.

The magnetizing inductance will affect the transient response of the isolated drive signal. Generally, a lower inductance will produce a faster response time. Our selected transformer has a magnetizing inductance of 296 µH.

Once the transformer is selected, the two coupling capacitor values are calculated. The coupling capacitor values will determine the amount of ripple voltage seen at the gate of the synchronous FET; total gate ripple will be the sum of the individual capacitor ripple voltages.

To size the coupling capacitors, first determine the maximum ripple we will allow each capacitor to contribute to the overall gate ripple voltage. (~1% of the maximum gate drive voltage is chosen for our design). Next, factor in the values for synchronous FET gate charge, and the current flowing in the pull down resistor, R14:

$Qg := 31n$	FDMS86322 Gate Charge
$Vdrv := 12$	Nominal Gate Drive Voltage
$\Delta Vc1 := 0.1$	Desired Ripple Across Primary Cap
$\Delta Vc2 := 0.1$	Desired Ripple Across Secondary Cap
$Rgs := 1k$	Gate Resistor
$D := 0.95$	Off Time Duty Cycle (increased to account for transients)
$Lm := 296u$	Magnetizing Inductance
$Fsw = 2\times 10^{5}$	Switching Frequency

$$Cc2 := \frac{Qg}{\Delta Vc2} + \frac{(Vdrv - 0.7)\cdot D}{\Delta Vc2\cdot Rgs\cdot Fsw}$$

$Cc2 = 8.467\times 10^{-7}$ Secondary Side Capacitor

Our design will use a 1 µF capacitor on the secondary side. On the primary side:

$$Cc1 := \frac{Qg}{\Delta Vc1} + \frac{(Vdrv - 0.7)\cdot D}{\Delta Vc1\cdot Rgs\cdot Fsw} + \frac{Vdrv\cdot\left(D^2 - D^3\right)}{\Delta Vc1\cdot 4\cdot Lm\cdot Fsw^2}$$

$Cc1 = 9.611\times 10^{-7}$ Primary Side Capacitor

We will use a 1 µF capacitor on the primary side.

Once the primary side capacitor is determined, the series damping resistor is found:

$Cc1act := 1.0u$ Primary Side Capacitor

$$\sqrt{\frac{Lm}{Cc1act}} \cdot 2 = 34.409$$

A total series resistance of 34 Ω is required. This resistance includes the PD70201's drive resistance of 10 Ω, meaning an additional resistance of 24 Ω must be added. Resistor power is calculated assuming the transformer magnetizing current is dominant:

$$drcurrentpk := \frac{Vdrv}{Lm} \cdot \left[\frac{(1 - Dmin)}{Fsw}\right] \qquad drcurrentpk = 0.137$$

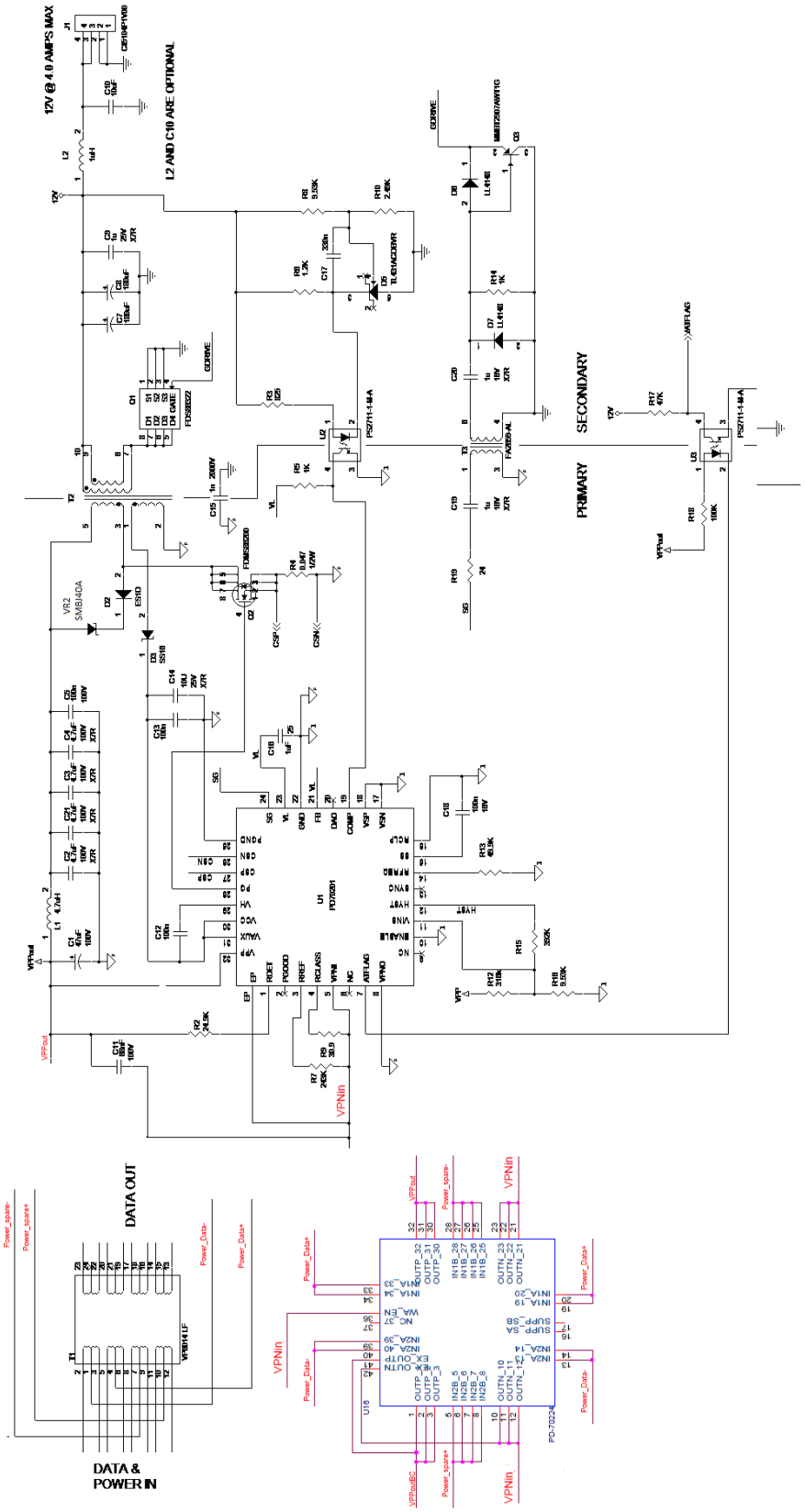
$$drcurrentrms := drcurrentpk\sqrt{\frac{(1 - Dmin)}{3}} \qquad drcurrentrms = 0.065$$

$$drvpwr := drcurrentrms^2 \cdot 24$$

$drvpwr = 0.102$ Calculated Resistor Power

Our chosen resistor is 24 Ω, 1 W. This is a standard value.

Figure 9-2. PD70201 Design Example (12 V, 47 W)



10. Design Tool

Microchip offers an online analog design tool: MPLAB Analog Design (MAD) for the PoE PD DC-DC converter. The tool allows you to browse existing evaluation boards or to generate a custom design based on your requirements. The design can then be exported into MPLAB® Mindi™ schematic for simulation. The MAD tool can be accessed at the Microchip website.

11. Reference Documents

All Microchip documentation is available online at www.microchip.com/poe.

- IEEE 802.3at-2015 standard, Section 33 (DTE Power via MDI)
- HDBaseT Specification
- PD70210/PD70210A/PD70210AL Datasheet
- PD70211 Datasheet
- PD70100/PD70200 Datasheet
- PD70101/PD70201 Datasheet
- PD70224 Datasheet
- AN3410 Design for PD System Surge Immunity PD701xx_PD702xx
- AN3472 Implementing Auxiliary Power in PoE
- AN3471 Designing a Type 1/2 802.3 or HDBaseT Type 3 PD Front End Using PD702x1 and PD701x1 ICs
- AN222 PD70210(A), PD70211 System Layout Guidelines
- AN208 PD70101A/ PD70201 PD device Layout Guidelines
- MPLAB Analog Design tool (MAD) at http://www.microchip.com/mad-poe.

12. Revision History

Revision	Date	Description
B	6/2021	The following is the summary of changes: • Updated Table 1 in the Introduction section. • Added the 10. Design Tool section. • Updated the 11. Reference Documents section. • Updated the 9.16 Synchronous Gate Drive section.
A	06/2020	This is the initial issue of this document. Designing a Type1/2 802.3 or HDBaseT Type 3 Powered Device Front End Using PD702x0 and PD701x0 ICs was previously described in the following document: • AN194: Designing a Type-1/2/3 IEEE 802.3at/af and POH Powered Device Using PD70101/PD70201/PD70211 PD Front-End With Integrated PWM Controller ICs

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