Silicon Errata and Data Sheet Clarifications

AVR64DB28/32/48/64

www.microchip.com Product Pages: AVR64DB28, AVR64DB32, AVR64DB48, AVR64DB64

The AVR64DB28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002300), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR64DB28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002300) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A0	Rev. B1
Device	Increased Current Consumption May Occur When VDD Drops	X	-
	Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X
CLKCTRL	The PLL Will Not Run when Using XOSCHF with an External Crystal	X	-
DAC	DAC Output Buffer Lifetime Drift	X	-
NVMCTRL	Flash Multi-Page Erase Can Erase Write Protected Section	X	X
	NVM_EEPROM_ERASE Command does Not Respect Write Protect	X	X
SPI	Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices	X	-
TCA	Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	-
TCB	CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	-
	TCB4 Waveform Output Alternative 1 Non-Functional	X	X
TCD	Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	-
	CMPAEN Controls All WOx for Alternative Pin Functions	X	-
	Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X
TWI	Flush Non-Functional	X	X
USART	Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	-
	Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X	X

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Increased Current Consumption May Occur When V_{DD} Drops

The device may experience increased current consumption of approximately 1.5 mA if V_{DD} drops below 2.1V and is held in the range of 1.9-2.1V. This will only occur if V_{DD} is originally at a higher level and then drops down to the mentioned voltage range.

Work Around

Ensure V_{DD} is always kept above 2.1V by setting the BOR trigger level to 2.2V to keep the device from executing if V_{DD} drops towards the affected voltage range. If operation in voltage range 1.9-2.1V is required, make sure V_{DD} does not rise above 2.1V and then drops down again. Note that the voltage levels given are not absolute values but typical values.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.2.2 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

2.3 CLKCTRL - Clock Controller

2.3.1 The PLL Will Not Run when Using XOSCHF with an External Crystal

When the PLL is configured to run from an external source (SOURCE in CLKCTRL.PLLCTRLA is '1'), the PLL will only run if XOSCHF is configured to use an external clock (SELHF in CLKCTRL.XOSCHFCTRLA is '1'). It will not work with an external crystal.

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.4 DAC - Digital-to-Analog Converter

2.4.1 DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over the device's lifetime if powered with the DAC output buffer disabled.

Work Around

Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is '1') continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

2.5.2 NVM_EEPROM_ERASE Command does Not Respect Write Protect

The NVM_EEPROM_ERASE command does not respect the EEPROM Write Protected (EEWP) bit in the Control B (NVMCTRL.CTRLB) register. Content will be erased even though it should not.

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

2.6 SPI - Serial Peripheral Interface

2.6.1 Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices

Alternative 2 Pin Position is non-functional for the SPI1 instance (SPI1 in PORTMUX.SPIROUTEA is 0x2) with 48-pin devices.

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.7 TCA - 16-Bit Timer/Counter Type A

2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.8 TCB - 16-Bit Timer/Counter Type B

2.8.1 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.8.2 TCB4 Waveform Output Alternative 1 Non-Functional

It is impossible to select TCB4 Waveform Output (WO) alternative 1 (TCB4 in PORTMUX.TCBROUTEA is '0x1') even if pin PC6 exists.

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

2.9 TCD - 12-Bit Timer/Counter Type D

2.9.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A0	Rev. B1

X	-

2.9.2 CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around

None.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.9.3 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

2.10 TWI - Two-Wire Interface

2.10.1 Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in the Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around

Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. An ordinary operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

2.11 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.11.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	-

2.11.2 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A0	Rev. B1
X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002300).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	12/2024	• Document: – General editorial updates – Back Matter and PDF front cover updates • Added Erratum for silicon Rev. A0 and Rev. B1: – TCB: TCB4 Waveform Output Alternative 1 Non-Functional • Updated Erratum for silicon Rev. B1: – USART: Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Removed Data Sheet Clarifications: – Device: • *Features* • *FUSE - Configuration and User Fuses - SYSCFG0* – AC: *Analog Comparator Interrupt Control* – DAC: *DAC Output* – SPI: • *SPI - Serial Peripheral Interface: Operation - Client Mode* • *SPI - Serial Peripheral Interface: Operation - Client Mode - Buffer Mode* – Electrical Characteristics: • *I/O Pin Characteristics* • *Memory Programming Specifications* • SPI
C	04/2024	• General editorial updates • Added Silicon Revision: B1 • Added Errata: – Device: Write Operation Lost if Consecutive Writes to Specific Address Spaces – NVMCTRL: NVM_EEPROM_ERASE Command does Not Respect Write Protect – SPI: Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices – TCD: Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used – TWI: Flush Non-Functional – USART: Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Added Data Sheet Clarifications: – SPI: *SPI - Serial Peripheral Interface* – SPI: *SPI - Serial Peripheral Interface* – Electrical Characteristics: *I/O Pin Characteristics* – Electrical Characteristics: *SPI*

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Doc. Rev.	Date	Comments
B	03/2022	• Document: General editorial updates. • Added errata: – DAC: DAC Output Buffer Lifetime Drift – NVMCTRL: Flash Multi-Page Erase Can Erase Write Protected Section – TCD: Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used – TWI: Flush Non-Functional • Added data sheet clarifications: – Device: *Features* – Device: *FUSE - Configuration and User Fuses - SYSCFG0* – AC: *Analog Comparator Interrupt Control* – DAC: *DAC Output* – Electrical Characteristics: *Memory Programming Specifications*
A	02/2021	Initial document release

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