AVR® EA

Product Brief

Introduction

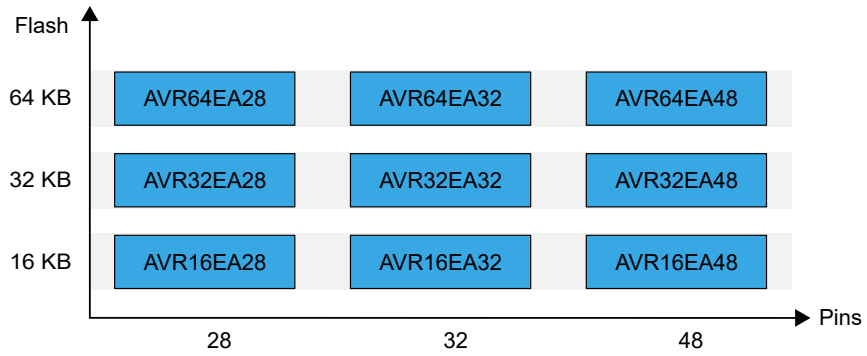
The AVR® EA Family of microcontrollers uses the AVR® CPU with hardware multiplier running at clock speeds up to 20 MHz, with up to 64 KB of Flash, up to 6 KB of SRAM, and 512 bytes of EEPROM in 28-, 32- or 48-pin packages. The AVR® EA Family uses the latest technology from Microchip with a flexible and low-power architecture, including an Event System, accurate analog subsystems, and advanced digital peripherals.

Family Overview

The figure below shows the AVR® EA Family of devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

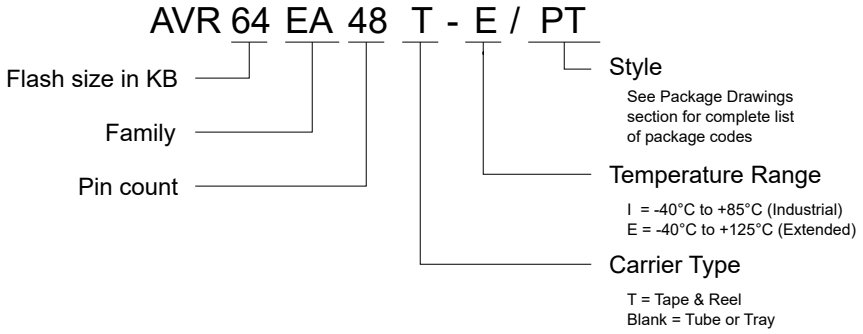
Figure 1. AVR® EA Family Overview



Devices with different Flash memory sizes typically also have different SRAM sizes.

A device name in the AVR® EA Family decodes as follows:

Figure 2. AVR® EA Family Device Designation



Memory Overview

Table 1. Memory Overview

Devices	AVR16EA28 AVR16EA32 AVR16EA48	AVR32EA28 AVR32EA32 AVR32EA48	AVR64EA28 AVR64EA32 AVR64EA48
Flash memory (Read-while-write section)	16 KB (12 KB)	32 KB (28 KB)	64 KB (56 KB)
SRAM	2 KB	4 KB	6 KB
EEPROM	512B	512B	512B
User row	64B	64B	64B

Peripheral Overview

Table 2. Peripheral Overview

Feature	AVR16EA28 AVR32EA28 AVR64EA28	AVR16EA32 AVR32EA32 AVR64EA32	AVR16EA48 AVR32EA48 AVR64EA48
Pins	**28**	**32**	**48**
Max. frequency (MHz)	20	20	20
16-bit Timer/Counter type A (TCA)	2	2	2
16-bit Timer/Counter type B (TCB)	4	4	4
Real-Time Counter (RTC)	1	1	1
USART/SPI host	3	3	3
SPI host/client	1	1	1
TWI/I^2C	1(1)	1(1)	1(1)
12-bit differential ADC (channels)	1 (24)	1 (28)	1 (32)
10-bit DAC	1	1	1
Analog Comparator (AC)	2	2	2
Configurable Custom Logic Look-up Table (CCL LUT)	4	4	4
Watchdog Timer	1	1	1
Event System channels	6	6	6
General Purpose I/O pins (input/output(2))	24/23	28/27	42/41
PORT	PA[7:0] PC[3:0] PD[7:0] PF[7,6,1,0]	PA[7:0] PC[3:0] PD[7:0] PF[7:0]	PA[7:0] PB[5:0] PC[7:0] PD[7:0] PE[3:0] PF[7:0]
External interrupts	24	28	42
CRCSCAN	1	1	1

.....continued			
Feature	**AVR16EA28 AVR32EA28 AVR64EA28**	**AVR16EA32 AVR32EA32 AVR64EA32**	**AVR16EA48 AVR32EA48 AVR64EA48**
Pins	**28**	**32**	**48**
Unified Program and Debug Interface (UPDI)	1	1	1

Notes:

1. The TWI/I^2C can operate simultaneously as a host and client on different pins.
2. PF6/$\overline{\text{RESET}}$ pin is input only.

Features

- AVR® CPU
  - Running at up to 20 MHz
  - Single-cycle I/O register access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
  - Supply voltage range: 1.8-5.5V
- Memories
  - 16/32/64 KB In-system-programmable Flash memory with a true read-while-write operation
  - 2/4/6 KB SRAM
  - 512B EEPROM
  - 64B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash: 10,000 cycles
    - EEPROM: 100,000 cycles
  - Data retention: 40 Years at 55°C
- System
  - Power-on Reset (POR) circuit
  - Brown-out Detector (BOD) with user-programmable levels
  - Voltage Level Monitor (VLM) with interrupt at a programmable level above the BOD level
  - Clock Failure Detection (CFD)
  - Clock options:
    - High-precision internal oscillator with selectable frequency up to 20 MHz (OSCHF)
      - Auto-tuning for improved internal oscillator accuracy
    - Internal ultra-low power 32.768 kHz oscillator (OSC32K)
    - External 32.768 kHz crystal oscillator (XOSC32K)
    - External clock input
    - External high-frequency crystal oscillator with clock failure detection (XOSCHF)
  - Single pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes
    - Idle with all peripherals running for immediate wake-up
    - Standby with a configurable operation of selected peripherals
    - Power-Down with full data retention
- Peripherals
  - Two 16-bit Timer/Counters type A (TCA) with three compare channels for PWM and waveform generation
  - Four 16-bit Timer/Counters type B (TCB) with input capture for capture and signal measurements
  - One 16-bit Real-Time Counter (RTC) that can run from an external crystal or internal oscillator
  - Three USARTs with fractional baud rate generator, auto-baud, and start-of-frame detection
  - One host/client Serial Peripheral Interface (SPI)
  - One Two-Wire Interface (TWI) with dual address match
    - Independent host and client operation (Dual mode)
    - Phillips I^2C compatible
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz)
  - Event System for CPU-independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with up to four programmable Look-up Tables (LUTs)
  - One 12-bit, 300 ksps, differential Analog-to-Digital Converter (ADC)

  - One 10-bit Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (ACs) with window compare functions
  - Multiple voltage references (VREF)
    - 1.024V
    - 2.048V
    - 2.500V
    - 4.096V
    - VREFA
    - V_{DD}
  - Automated Cyclic Redundancy Check (CRC) Flash program memory scan
  - Watchdog Timer (WDT) with Window mode and separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - Up to 42/41 programmable I/O pins
  - 28-pin SPDIP, SSOP and VQFN 4x4
  - 32-pin VQFN 5x5 and TQFP 7x7
  - 48-pin VQFN 6x6 and TQFP 7x7
- Temperature Ranges
  - Industrial: -40°C to 85°C ambient
  - Extended: -40°C to 125°C ambient

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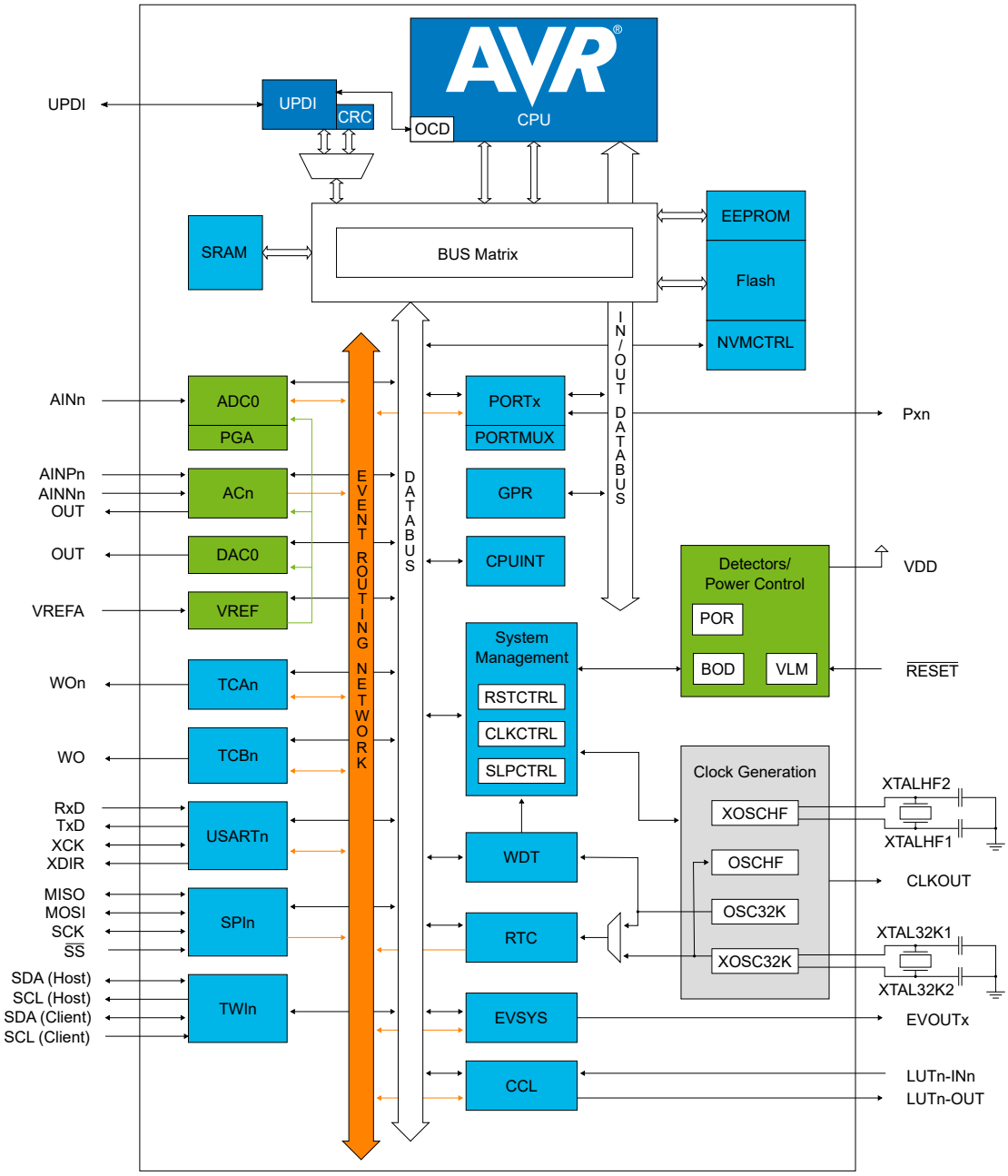
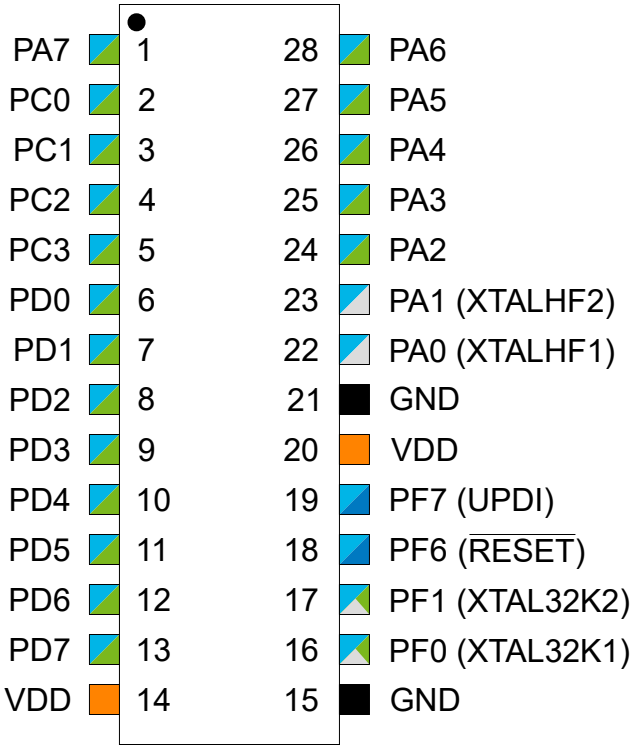
1. Block Diagram



2. Pinout

2.1 28-pin SPDIP and SSOP



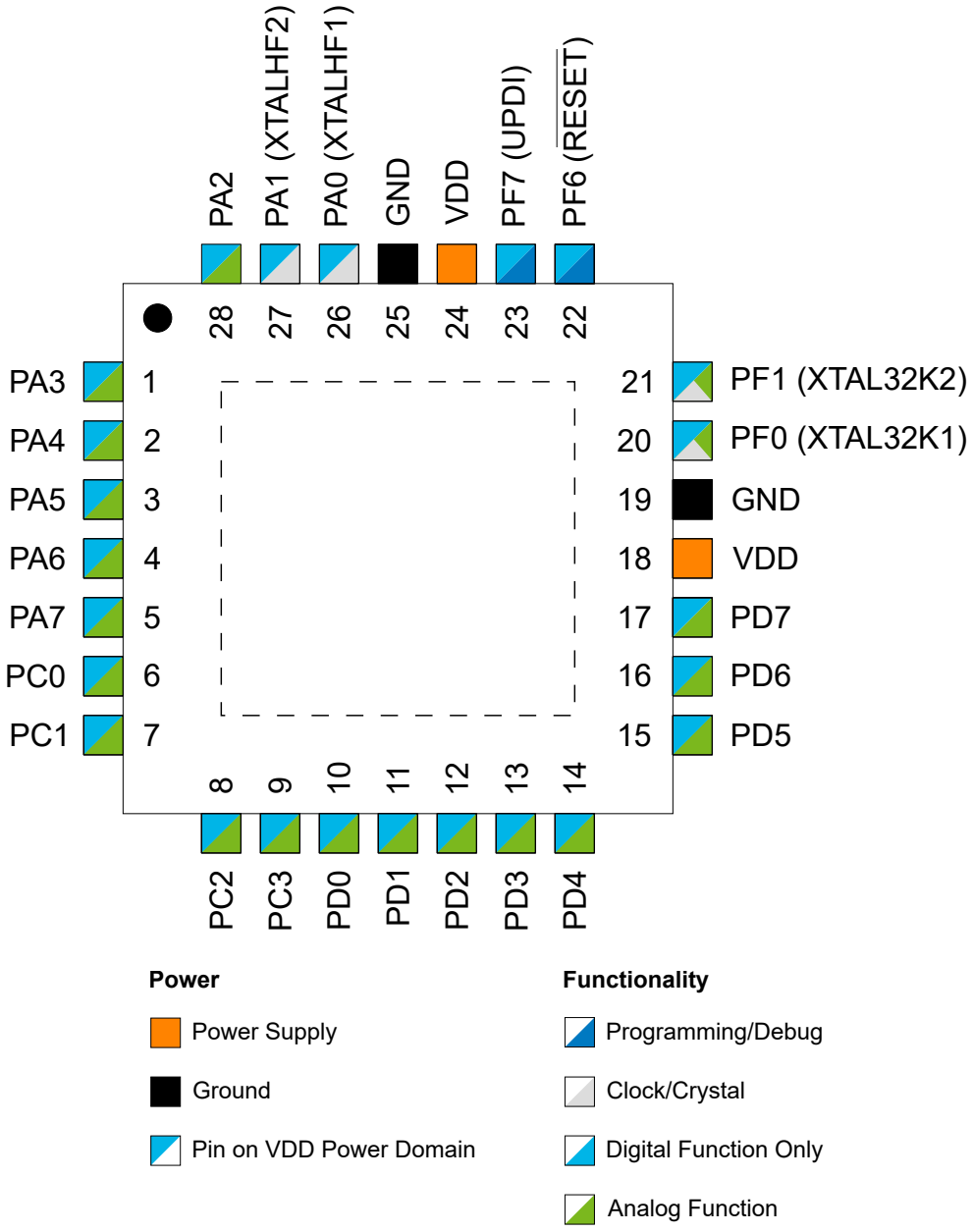
Power

- Power Supply
- Ground
- Pin on VDD Power Domain

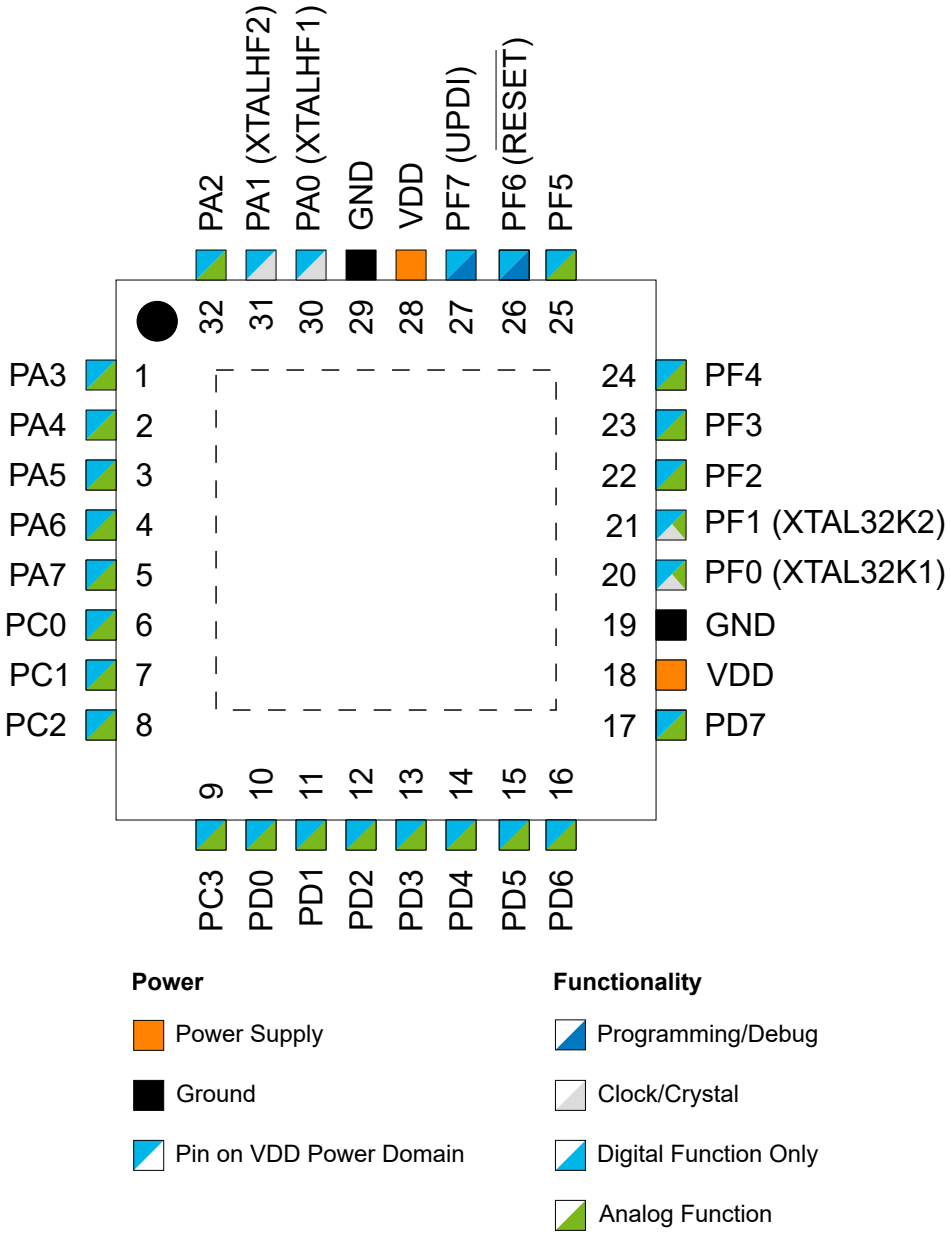
Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

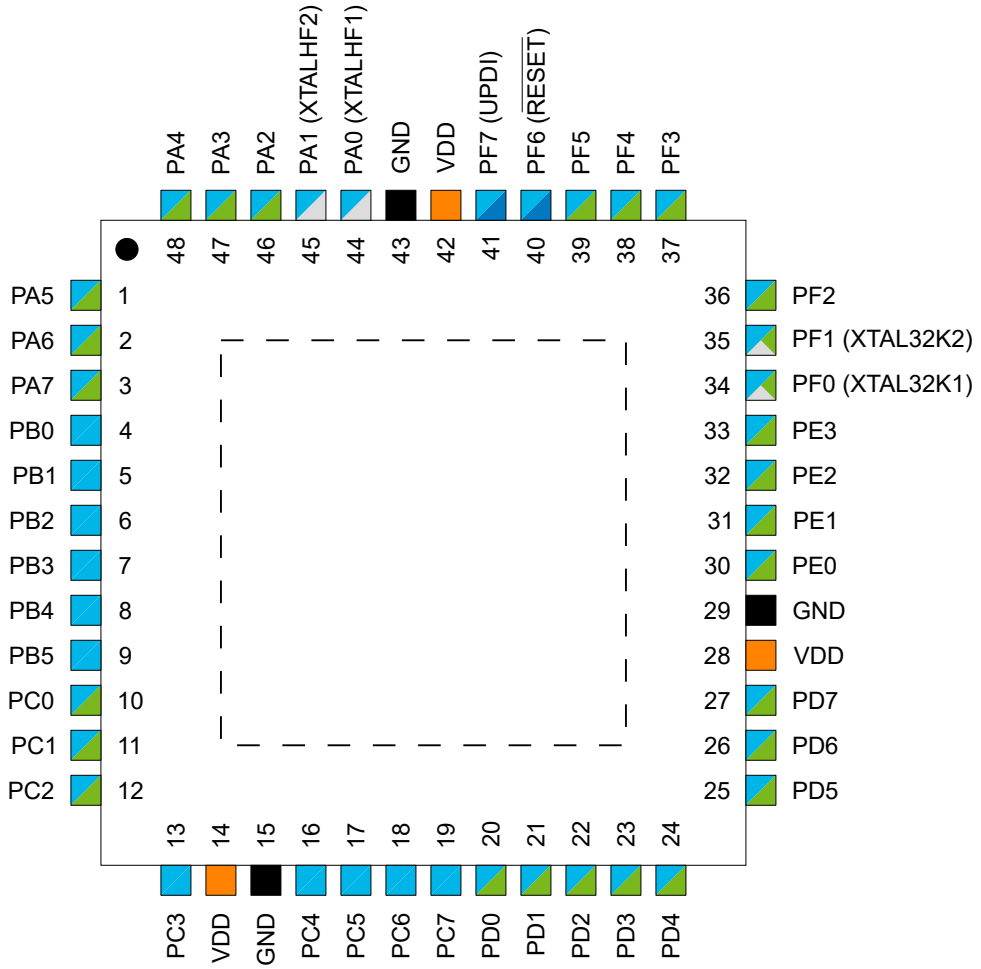
2.2 28-pin VQFN



2.3 32-pin VQFN and TQFP



2.4 48-pin VQFN and TQFP



3. I/O Multiplexing and Considerations

3.1 I/O Multiplexing

Table 3-1. PORT Function Multiplexing

VQFN/TQFP 48-pin	VQFN/TQFP 32-pin	SPDIP/SSOP 28-pin	VQFN 28-pin	Pin name(1)	Special	ADC0	ACn	DAC0	USARTn	SPI0	TWI0(3)	TCAn	TCBn	CCL	EVSYS
44	30	22	26	PA0	XTALHF1 EXTCLK				0, TxD	0, MOSI(2)	0, SDA(HC)(2)	0, WO0		LUT0, IN0	
45	31	23	27	PA1	XTALHF2				0, RxD	0, MISO(2)	0, SCL(HC)(2)	0, WO1		LUT0, IN1	
46	32	24	28	PA2		AIN22			0, XCK 0, TxD(2)		0, SDA(HC)	0, WO2	0, WO	LUT0, IN2	EVOUTA
47	1	25	1	PA3		AIN23			0, XDIR 0, RxD(2)		0, SCL(HC)	0, WO3	1, WO	LUT0, OUT	
48	2	26	2	PA4		AIN24			0, TxD(2)	0, MOSI		0, WO4 1, WO0(2)			
1	3	27	3	PA5		AIN25			0, RxD(2)	0, MISO		0, WO5 1, WO1(2)			
2	4	28	4	PA6		AIN26			0, XCK(2)	0, SCK		1, WO2(2)		LUT0, OUT(2)	
3	5	1	5	PA7	CLKOUT	AIN27	0, OUT 1, OUT		0, XDIR(2)	0, $\overline{SS}$					EVOUTA(2)
4				PB0								0, WO0(2) 1, WO0			
5				PB1								0, WO1(2) 1, WO1			
6				PB2								0, WO2(2) 1, WO2			EVOUTB
7				PB3								0, WO3(2) 1, WO3			
8				PB4								0, WO4(2) 1, WO4	2, WO(2)		
9				PB5								0, WO5(2) 1, WO5	3, WO		
10	6	2	6	PC0		AIN28			1, TxD	0, SCK(2) 0, MOSI(2)		0, WO0(2)	2, WO	LUT1, IN0	
11	7	3	7	PC1		AIN29			1, RxD 0, TxD(2)	0,$\overline{SS}$(2) 0, MISO(2) 0, MOSI(2)		0, WO1(2)	3, WO(2)	LUT1, IN1	
12	8	4	8	PC2		AIN30	0, AINN3 1, AINN3		1, XCK 0, RxD(2)	0, SCK(2) 0, MISO(2)	0, SDA(C) 0, SDA(HC)(2)	0, WO2(2)		LUT1, IN2	EVOUTC
13	9	5	9	PC3		AIN31	0, AINP4 1, AINP4		1, XDIR 0,XCK(2)	0, $\overline{SS}$(2) 0, SCK(2)	0, SCL(C) 0, SCL(HC)(2)	0, WO3(2)		LUT1, OUT	
14				VDD											
15				GND											
16				PC4					1, TxD(2)			0, WO4(2) 1, WO0(2)			
17				PC5					1, RxD(2)			0, WO5(2) 1, WO1(2)			
18				PC6			0, OUT(2) 1, OUT(2)		1, XCK(2)		0, SDA(C)(2)	1, WO2(2)		LUT1, OUT(2)	
19				PC7					1, XDIR(2)		0, SCL(C)(2)				EVOUTC(2)
20	10	6	10	PD0		AIN0	0, AINN1 1, AINN1					0, WO0(2)		LUT2, IN0	
21	11	7	11	PD1		AIN1						0, WO1(2)		LUT2, IN1	

.....continued

VQFN/TQFP 48-pin	VQFN/TQFP 32-pin	SPDIP/SSOP 28-pin	VQFN 28-pin	Pin name(1)	Special	ADC0	ACn	DAC0	USARTn	SPI0	TWI0(3)	TCAn	TCBn	CCL	EVSYS
22	12	8	12	PD2		AIN2	0, AINP0 1, AINP0					0, WO2(2)		LUT2, IN2	EVOUTD
23	13	9	13	PD3		AIN3	0, AINN0 1, AINP1					0, WO3(2)		LUT2, OUT	
24	14	10	14	PD4		AIN4	1, AINP2		0, TxD(2)	0, MOSI(2)		0, WO4(2) 1, WO0(2)			
25	15	11	15	PD5		AIN5	1, AINN0		0, RxD(2)	0, MISO(2)		0, WO5(2) 1, WO1(2)			
26	16	12	16	PD6		AIN6	0, AINP3 1, AINP3	OUT	0, XCK(2) 1, TxD(2)	0, SCK(2)		1, WO2(2)		LUT2, OUT(2)	
27	17	13	17	PD7	VREFA	AIN7	0, AINN2 1, AINN2		0, XDIR(2) 1, RxD(2)	0, $\overline{SS}$(2)					EVOUTD(2)
28	18	14	18	VDD											
29	19	15	19	GND											
30				PE0		AIN8	0, AINP1			0, MOSI(2)		0, WO0(2)			
31				PE1		AIN9				0, MISO(2)		0, WO1(2)			
32				PE2		AIN10	0, AINP2			0, SCK(2)		0, WO2(2)			EVOUTE
33				PE3		AIN11				0, $\overline{SS}$(2)		0, WO3(2)			
34	20	16	20	PF0	XTAL32K1	AIN16			2, TxD			0, WO0(2)		LUT3, IN0	
35	21	17	21	PF1	XTAL32K2	AIN17			2, RxD			0, WO1(2)		LUT3, IN1	
36	22			PF2		AIN18			2, XCK			0, WO2(2)		LUT3, IN2	EVOUTF
37	23			PF3		AIN19			2, XDIR			0, WO3(2)		LUT3, OUT	
38	24			PF4		AIN20			2, TxD(2)			0, WO4(2)	0, WO(2)		
39	25			PF5		AIN21			2, RxD(2)			0, WO5(2)	1, WO(2)		
40	26	18	22	PF6	$\overline{RESET}$/HV										
41	27	19	23	PF7	UPDI					0, $\overline{SS}$(2)					EVOUTF(2)
42	28	20	24	VDD											
43	29	21	25	GND											

Notes:

1. Pin names are of P*xn* type, with *x* being the PORT instance (A, B, C, ...) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event inputs.
2. Alternative pin positions.
3. TWI pins are marked *HC* if they can be used as TWI Host or Client pins and *C* if they only can be used as TWI Client pins.

4. Product Brief Revision History

Note: The product brief revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Rev. B - 08/2022

Section	Changes
Document	Changes to reflect the latest data sheet updates
Family Overview	8 kB flash variants removed from the document: • Family Overview figure • Memory Overview table • Peripheral Overview table • *Features* section

4.2 Rev. A - 09/2020

Section	Changes
Document	Initial release

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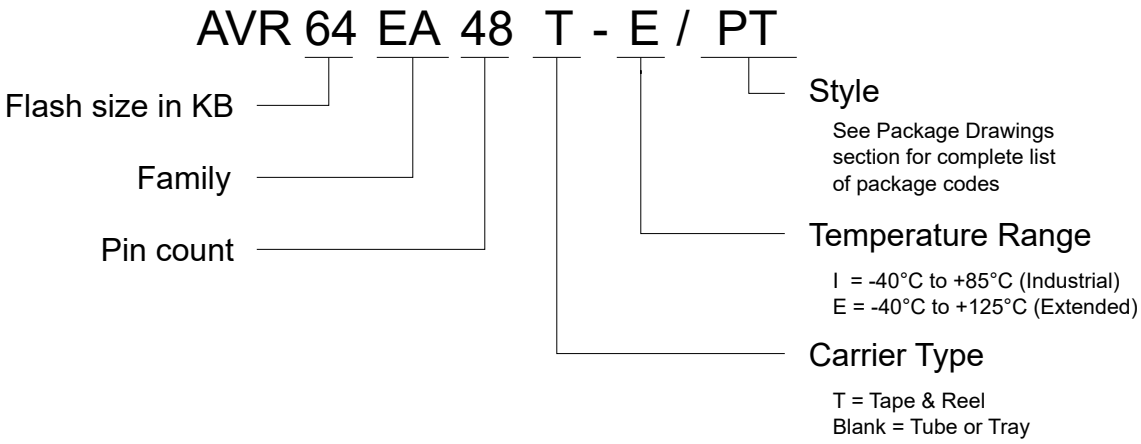

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