ATSENSE-301 Interfacing Guidelines

APPLICATION NOTE

Introduction

This Application Note provides hardware considerations and design guidelines for the hardware interface to the ATSENSE-301 Analog Front End (AFE) for metrology applications. It provides details about recommended ADC input circuitry.

ATSENSE can be used with standard Atmel® | SMART microcontrollers, such as SAM4S, for non-metering applications.

Reference Documents

Type	Title	Atmel Lit. No.
Datasheet	(ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) Multi-Channel Sigma-Delta Analog Front End	11219
Application Note	EMAFE Control on SAM4CM Series	44039

Table of Contents

1. Power Supply Filtering & Decoupling

The Power Supply interface circuits are important for minimizing the impact of electrical noise on the ATSENSE performance. The ATSENSE has an internal LDO for powering its analog circuits, including VREF. The LDO has a typical power supply rejection ratio (PSRR) of 40 dB. For most cases, this alleviates the need for a series element as part of the filtering for VDDIN. For cases where additional filtering is desirable, a series choke in the VDDIN path is a cost-effective approach.

2. Analog Inputs

2.1 ADC Inputs Characteristics

The ATSENSE utilizes Sigma-Delta ADCs with the following design constraints:

1. The sampling frequency is nominally 1.024 MHz.
2. The maximum DC source impedance is 3 kΩ.
3. The signal band is DC to 1386Hz (21st harmonic of the fundamental, i.e., 21 * 60Hz+10%).

An anti-aliasing filter is required for band-limiting the input signals. Typically, a single-pole RC filter is sufficient for metrology applications. Setting the cutoff frequency at a nominal 16 kHz provides a good tradeoff between filter simplicity and performance. Note that at 16 kHz, the in-band attenuation is less than 0.1dB at 1386Hz. The phase impact is also minimal.

2.2 Analog Current Inputs for Current Transformer (CT) Connections

The circuit below is an excerpt from the SAM4CMx-DB User's Guide. D505 and D506 are protection diodes. X505 and X506 are ferrite bead inductors. C513 and C514 are high frequency shunt capacitors. These devices provide protection for EMC fast transient bursts. The diodes also clamp the voltage to keep the ATSENSE ADC inputs below the absolute maximum ratings, without affecting normal (in-range) signals.

In the circuit below, R513 and R514 provide the burden resistance for the CT. The CT design and burden resistance are closely linked; the burden resistor values shown below are representative only.

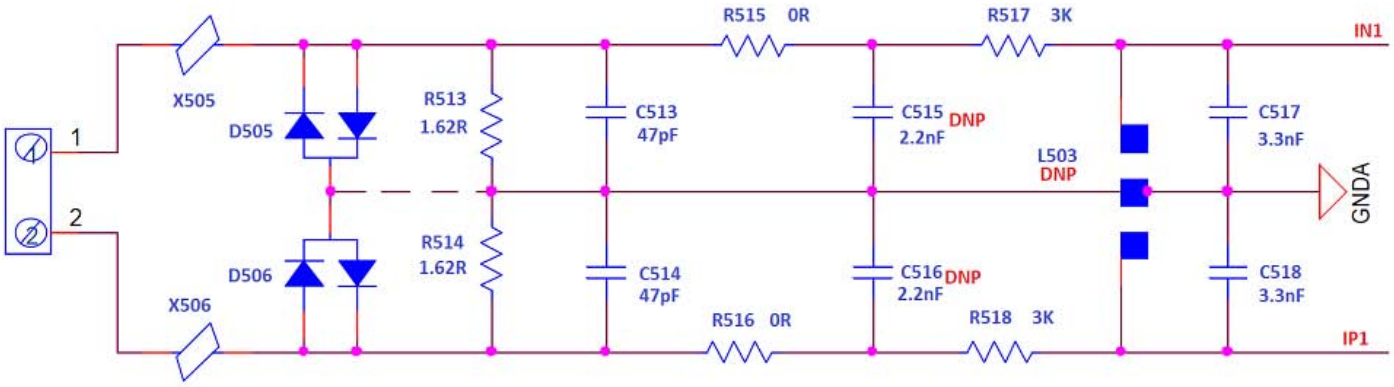
Note that the circuit shows a two pole anti-aliasing filter topology, where R517+C517 & R518+C518 form the first pole, and where R515+C515 & R516+C516 form the second pole. (In the case of CT or shunt resistor sensors, the second pole is not used; R515 and R516 are 0Ω resistors, while C515 and C516 are left out.) Typically, a single-pole filter is sufficient. For the figure, the effective filter is the RC combination of the 3 kΩ resistor and the 3.3nF capacitor. The cut-off frequency is defined by the equation below:

$$f_c = \frac{1}{2\pi RC}$$

With R = 3 kΩ and C = 3.3 nF, $f_c \approx 16$ kHz.

Note: The common node connecting D505 and D506 may alternatively be connected to GNDA, as shown via the dotted line in the figure below. This may improve common mode noise rejection.

Figure 2-1. Analog Current Input Circuit



2.3 Analog Current Inputs for Rogowski Coil Connections

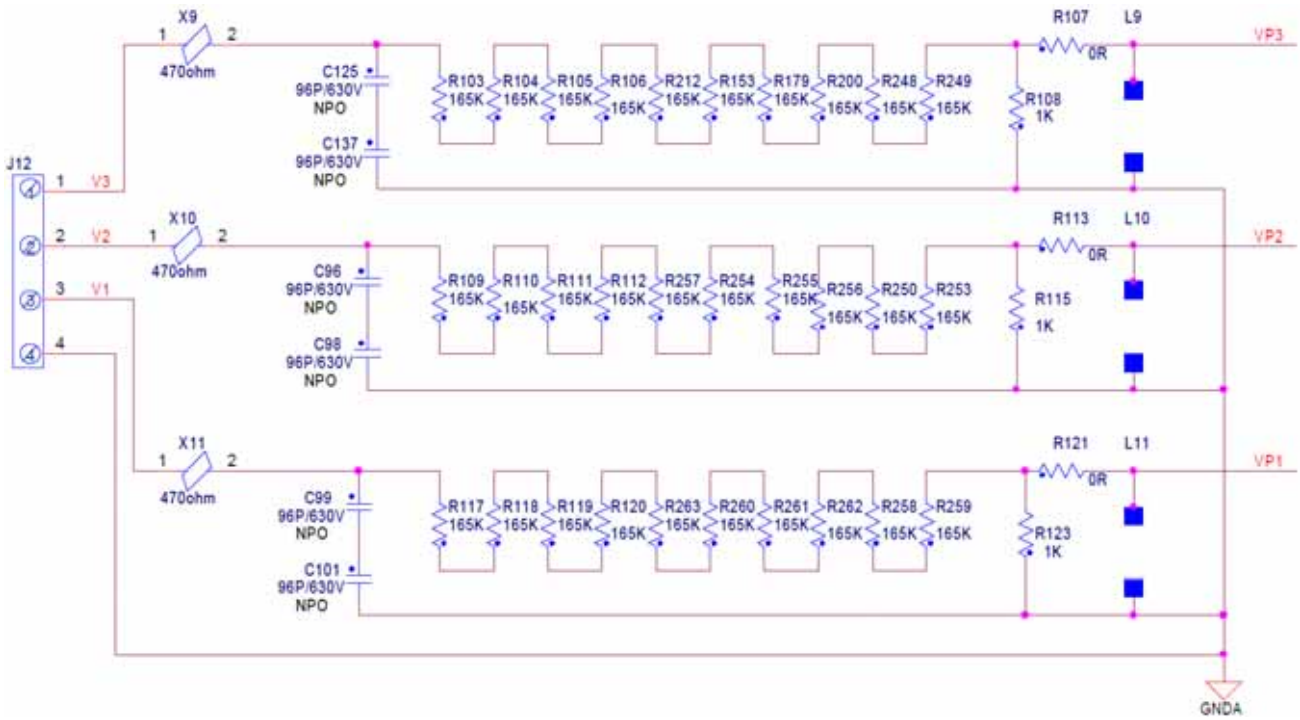
When using Rogowski coils for current sensing, the second pole R515/C515 must be mounted. As a rule of thumb, this second pole is placed one decade away from the first one. The burden resistors are removed.

2.4 Analog Voltage Inputs

For the example circuit below, the nets VP1, VP2, VP3, and GNDA connect to the same-name pins of the ATSENSE. The ATSENSE VN pin connects to GNDA.

The resistor-divider chains allow the VPx signal to meet the ATSENSE input range limits (-0.25V to +0.25V.) The values for the series resistors may be adjusted to accommodate different voltage inputs. The “bottom” resistor in the divider (e.g. R108) is recommended to be 1 kΩ.

Figure 2-2. Analog Voltage Input Circuit



3. Host Microcontroller

3.1 Interrupt Signal

The ATSENSE interrupt output signal (ITOUT) connects to an interrupt input of the host MCU.

ITOUT is open drain. For best signal integrity, this signal should be pulled up with a relatively low value resistor (e.g., 2.7 kΩ.)

Some MCUs may offer internal pull-up resistors for their input ports. However, these internal pull-ups are typically higher value and hence not suitable for fast-changing signals like the ATSENSE interrupt. Also they are not yet programmed when power is first applied.

3.2 SPI Serial Port

The ATSENSE SPI port provides a high-speed bidirectional serial interface. The SPI signals should preferably be connected to the corresponding signals of the host MCU's SPI peripheral. The table below provides the list of SPI port signals and their recommended connections.

ATSENSE-301 Signal Name	Serial Peripheral Interface (SPI) Usage	Host MCU Connection
NPCS	SPI Chip Select	SPI Select
MISO	SPI Master-In-Slave-Out	MISO
MOSI	SPI Master-Out-Slave-In	MOSI
SPCK	SPI Clock	SPI Clock

3.2.1 Recommended Operating Frequencies

The ATSENSE SPI clock is specified to work up to a maximum frequency of 10 MHz. For most applications, a somewhat lower clock frequency meets the timing requirements. For example, when using the SAM4CMx and the Atmel-provided Metrology Firmware, the firmware initializes the SPI clock frequency to 8.33 MHz.

3.3 Master Clock

The ATSENSE was designed to provide a nominal 16 kSamples/second for each of the ADC inputs; the sampling rate is driven by the Master Clock (MCLK) value of (nominal) 4.096 MHz.

While it is possible to operate the ATSENSE at different MCLK rates, the ATSENSE has only been characterized at the specified rate. Designers are advised to keep MCLK within the frequency bounds as specified in the datasheet. For designers considering the use of an unspecified MCLK frequency, contact the Atmel support team for additional guidance.

3.4 Example Host MCU Connection - SAM4C

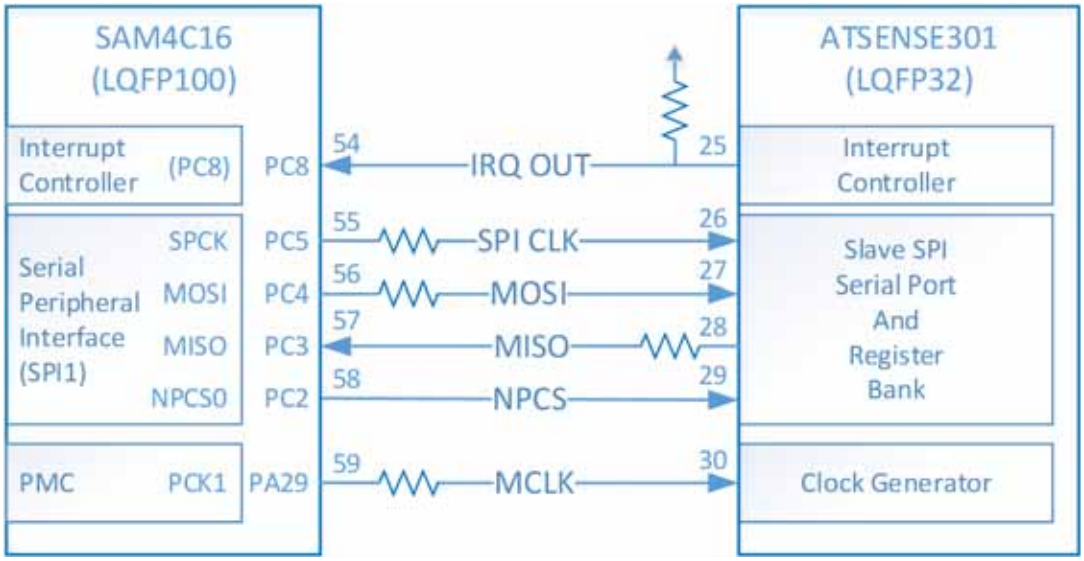
This section provides a sample connection for SAM4C.

The diagram below illustrates how to connect the SAM4C to the ATSENSE-301. This specific interface is required when using the Atmel Metrology firmware for the SAM4C (Core1.)

Atmel offers complete, ready-to-use Metrology Firmware that runs on SAM4C Core1. Correspondingly, Atmel also provides applications firmware (for Core0), as well as a PC GUI tool for interfacing with the SAM4C. Implemented together, the above described firmware/software provides a full complement of tools to facilitate a

faster development process. The tools run on the SAM4C-EK evaluation kits for a quick path for getting started. (Note that for the EK, the SAM4CM is used, which integrates the ATSENSE with the SAM4C in a System-on-Chip (SoC) solution.)

Figure 3-1. SAM4C to ATSENSE-301 Connection Diagram



4. General Recommendations

4.1 Using Different MCLK Frequencies

The ATSENSE was designed to provide a nominal 16 kSamples/second for each of the ADC inputs; the sampling rate is driven by the MCLK value of (nominal) 4.096 MHz.

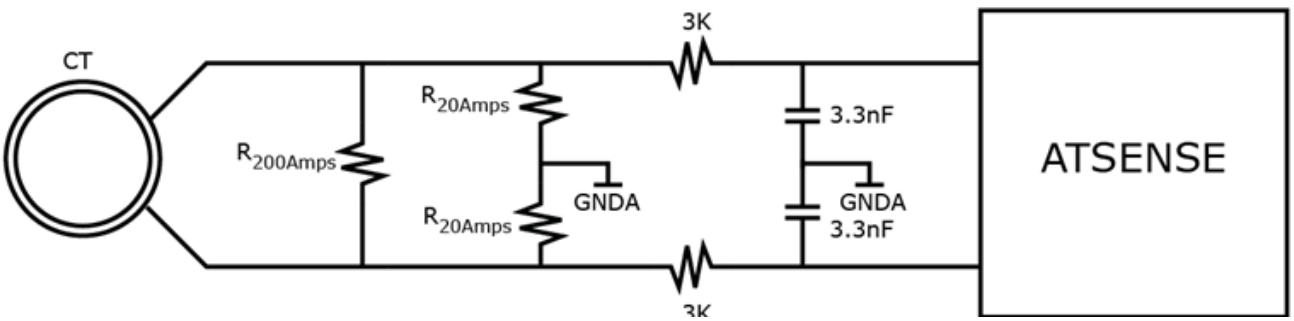
Conceivably, the sampling rate may be adjusted by changing the MCLK frequency. For example, an MCLK rate of ~2 MHz would yield a sampling rate of ~8 KHz. This may be useful for some designs, where higher sampling rates are not required, lessening the processing burden on the host microcontroller.

Different MCLK frequencies (and their corresponding sampling rates) have not been characterized and there are no plans for Atmel to do this.

4.2 Circuit Design for Handling Multiple Current Ranges

In this example, it is desirable to design a PCB to handle either a 20A or a 200A current input. In this case, the (simplified) circuit below may meet the criteria.

Figure 4-1. Multiple-Range Current Input Circuit



Use two “common mode” resistors (R20Amps) that are installed for both the 20A and the 200A versions. For the 200A version, include a differential resistor (R200Amps).

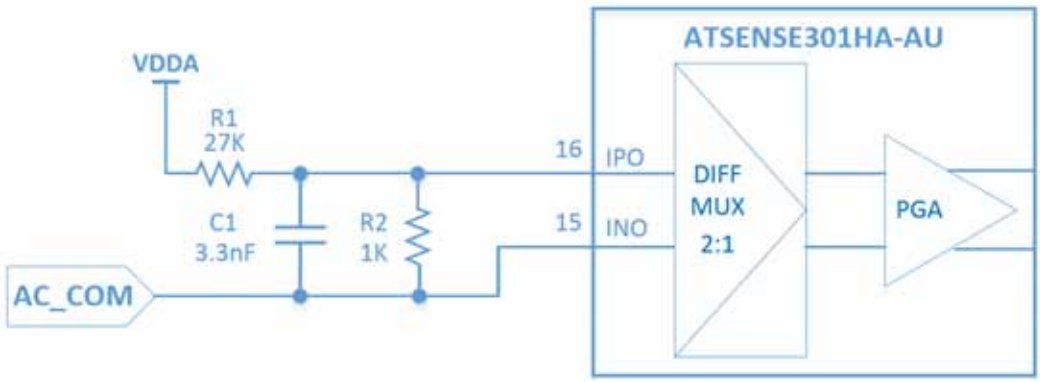
Note: When calculating the effective burden resistor for the 200A version, the R20Amps resistors need to be factored in.

The ATSENSE ADC inputs need to be DC-biased to ground; i.e., there must be a DC path to ground from each ATSENSE inputs. So the permanent resistors on the PCB must be the ones from each input to ground.

4.3 Decoupling for VDDA Monitor

Note: Only for use with FW that reads ADC current input 0 as a DC input. When using this input to measure (for example) VDDA, make sure to add a decoupling capacitor across the IP0 to IN0 inputs.

Figure 4-2. Supply Voltage Monitoring Circuit



Revision History

Table 4-1. ATSENSE-301 Interfacing Guidelines Revision History

Doc. Rev.	Date	Changes
44084A	29-Jun-16	First issue

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