AN26.2

Implementation Guidelines for Microchip's USB 2.0 and USB 3.1 Gen 1 and Gen 2 Hub and Hub-Combo Devices

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1.0 INTRODUCTION

This application note provides information on general printed circuit board layout considerations for Microchip's many families of USB Hub Controller devices. This information is broadly applicable to any of Microchip's USB 2.0 and USB 3.1 Gen 1 and Gen 2 device implementations.

1.1 Audience

This application note is written for readers that are familiar with PCB design, including signal integrity, differential signaling, and thermal management implementation concepts.

1.2 Objective

The goal of this document is to provide implementation information that specifically applies to designing PCBs using Microchip's High Speed and faster families of USB Hub Controller devices. Careful implementation of these guidelines enables successful designs.

1.3 Overview

Successful operation of Microchip's USB Hub Controllers requires special consideration for printed circuit board (PCB) layout. All Microchip USB Hub controllers contain a mix of sensitive analog circuitry, digital core logic, and high speed I/O circuitry. The PCB's design is part of the system circuit for all of these subsystems that can either enhance or detract from desired operation.

General issues such as placement and stack up are covered. Additionally, subsystem issues such as USB 2.0 / 3.1 Gen 1 and Gen 2 signaling/impedance, crystal connections, and other critical circuits are discussed. Controlling EMI, system power distribution, and signal return path management will also be addressed.

The guidelines presented supersede earlier notes for the applicable devices. The following recommendations are based on Microchip's experience and knowledge and may be accepted or rejected. Microchip does not guarantee any design. Each company is ultimately responsible for determining the suitability of its own design.

1.4 References

- Data Sheets: USB55xx, USB57xx, USB58xx, USB59xx, USB7xxx, USB38xx, USB25xx and USB46xx USB Hub Controller and Hub-Combo devices
- Application Note: *AN 26.21*
- Application Note: *AN 18.15*
- Evaluation designs that are referenced in this document can be found on the Microchip web site.

2.0 SCHEMATIC GUIDELINES

Specific requirements and suggestions for the schematic implementation of Microchip's USB hub controllers are indicated in this section. Product data sheets specify basic circuit needs.

2.1 Chassis and Cable Ground

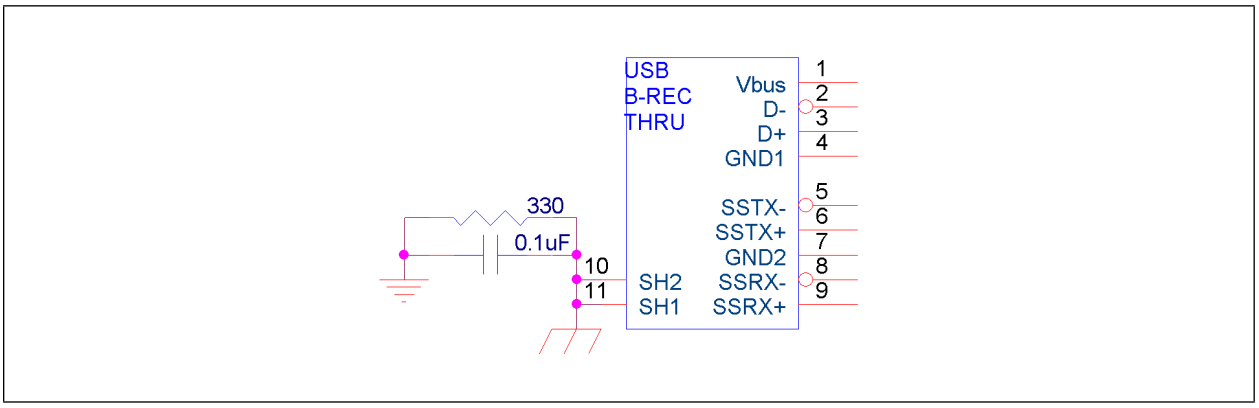
USB hub devices can be implemented in the following ways:

- Embedded with a host controller
- Embedded with a mix of inaccessible ports with embedded devices and user-accessible ports
- Embedded with a mix of a host, inaccessible ports with embedded devices, and user-accessible ports
- A stand-alone hub

Each of these implementation details can affect the best method to use for connecting the chassis and USB cable shields to digital ground. The best way to make these connections will depend on the design's system details. Refer to the many reference documents and white papers on this topic available on the Internet, especially those published by members of the USB consortium and providers of USB-enabled motherboards and devices.

Microchip has observed positive EMI and ESD behavior on stand-alone designs when connecting the USB cable shield to digital ground with an RC network (330 Ω resistor and a 0.1 μF capacitor in parallel) at each USB connector.

FIGURE 1: EXAMPLE CHASSIS GROUND CONNECTION



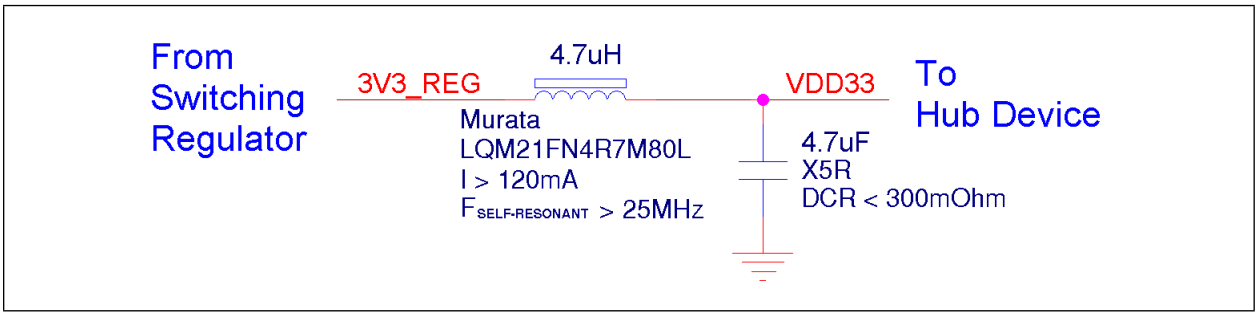
2.2 VDD12 and VDD33 Power Regulator

The USB57x4 & USB553x family of hubs use two external power voltages: VDD12 at 1.25 V, and VDD33 at 3.3 V.

The VDD12 rail is used for core digital functions and for the USB 3.1 Gen 1 PHYs. The VDD12 current consumed by the hub device will vary greatly. When the device is in "suspend" it will consume very little current. It will consume maximum current when all USB 3.1 Gen 1 SuperSpeed interfaces are active. The selected regulator must be stable, low noise, and accurate across all power consumption ranges.

The VDD33 rail for the USB57x4 & USB553x devices are used by the PLL and other circuitry. Additionally, USB25xx devices derive core and other rails from VDD33. Therefore, the VDD33 supply must be very clean. Noise on VDD33 must be filtered out before it is received by the hub device. Some systems require < 5 mV of ripple on VDD33 at the hub device pins to pass SSC certification of the USB 3.1 Gen 1 test suite. Switching regulators are a common source for VDD33 noise. The example in Figure 2 shows an effective filter to block switching regulator noise from VDD33.

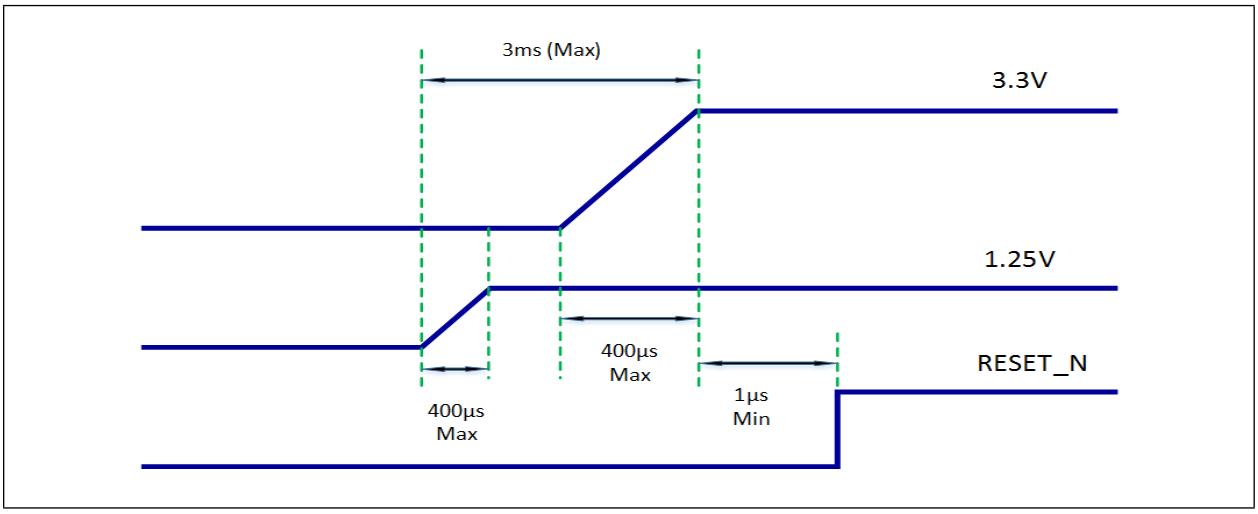
FIGURE 2: EXAMPLE SWITCHING REGULATOR NOISE FILTER



2.3 Power Sequence and RESET

Controlled power and RESET sequencing is critical to the operation of many Microchip USB devices. The VDD12 power rail should be applied prior to the VDD33 power rail. The device must be held in a RESET condition until after the power rails are valid and stable. Refer to Figure 3 for the typical power-up timing sequence for USB 3.1 Gen 1 hub devices.

FIGURE 3: POWER SEQUENCING



2.4 RESETn

RESETn is used to force a reconfigure cycle and restart within the hub. This signal should be driven high only when all power rails are stable and within operational conditions.

For stand-alone applications, **RESETn** should be connected to a supervisory circuit that monitors VDD12 and VDD33. **RESETn** should be asserted when either voltage is below its threshold. **RESETn** could also be asserted under manual or host control. A simple RC circuit may be used for stand-alone applications, but this only follows one voltage rail and may not work well when power is quickly removed then reapplied to the system, and is therefore not recommended.

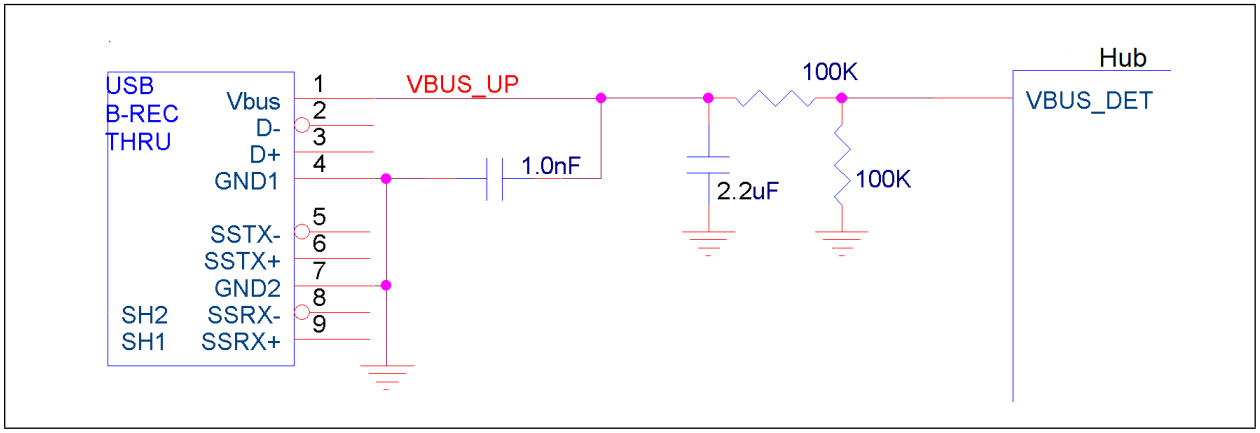
For embedded applications, **RESETn** should be slaved to both a supervisory circuit and to the host controller.

2.5 VBUS_DET

VBUS_DET is used to initiate a connect event to the hub device. The hub must be powered up, fully configured, and running before it receives the VBUS_DET signal for deterministic behavior.

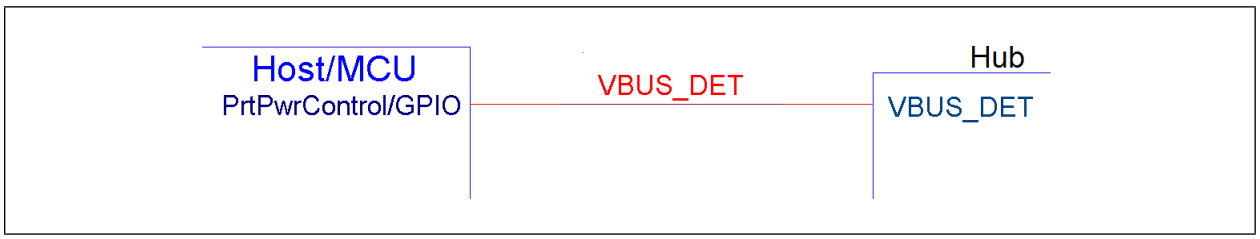
For stand-alone applications, this should be connected to the upstream VBUS through a resistor divider. The divider prevents back-powering the hub and reduces the VIN on the **VBUS_DET** pin. The USB specification requires between 1.0 µF and 10 µF of capacitance on the upstream VBUS signal. In order to meet that requirement, we suggest a 2.2 µF capacitor, as shown in Figure 4.

FIGURE 4: STAND-ALONE VBUS_DET CONNECTION



Embedded applications should actively control this pin with a 3.3 V signal.

FIGURE 5: EMBEDDED VBUS_DET CONNECTION



VBUS_DET may also be tied directly to 3.3 V for certain always-on applications. However, this is not usually recommended.

2.6 In-System OTP Programming

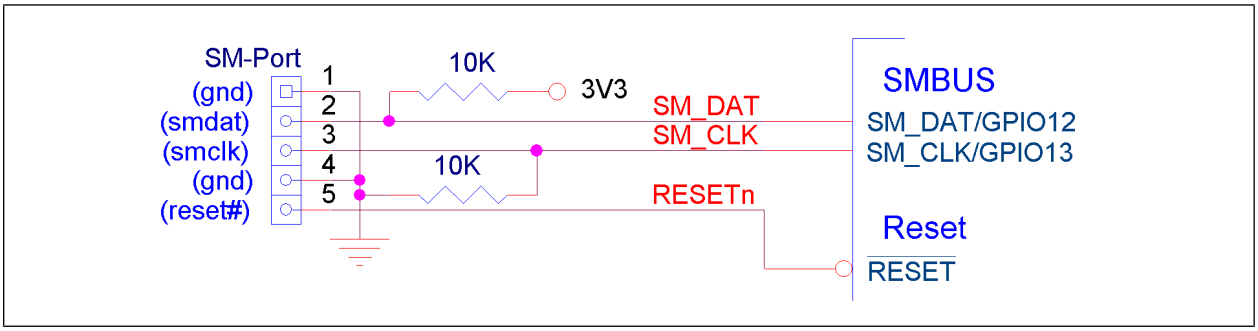
In-system programming of more modern hubs is primarily and preferably done through the USB link using the ProTouch™ or ProTouch2™ tools. Refer to the applicable device data sheet to confirm support.

Alternatively, and for older devices, programming can be done through the **SM_DAT** and **SM_CLK** pins and by manipulating the **RESETn** pin. Be sure to provide access to these signals on the system board (plus ground) to program the hub device.

To operate normally, disable the SMBus interface by pulling up **SM_DAT** and pulling down **SM_CLK** with external resistors of 10 KΩ - 20 KΩ. To program, pull up **SM_CLK** and **SM_DAT** to 1 KΩ - 4.7 KΩ (usually with resistors in the programming tool), then assert and de-assert **RESET#**, then run your programmer's routine with the desired code.

To run the new code, restore **SM_CLK** and **SM_DAT** to normal operation condition, assert then de-assert **RESET#**.

FIGURE 6: EXAMPLE PROVISION FOR IN-SYSTEM PROGRAMMING



3.0 PCB LAYOUT GUIDELINES

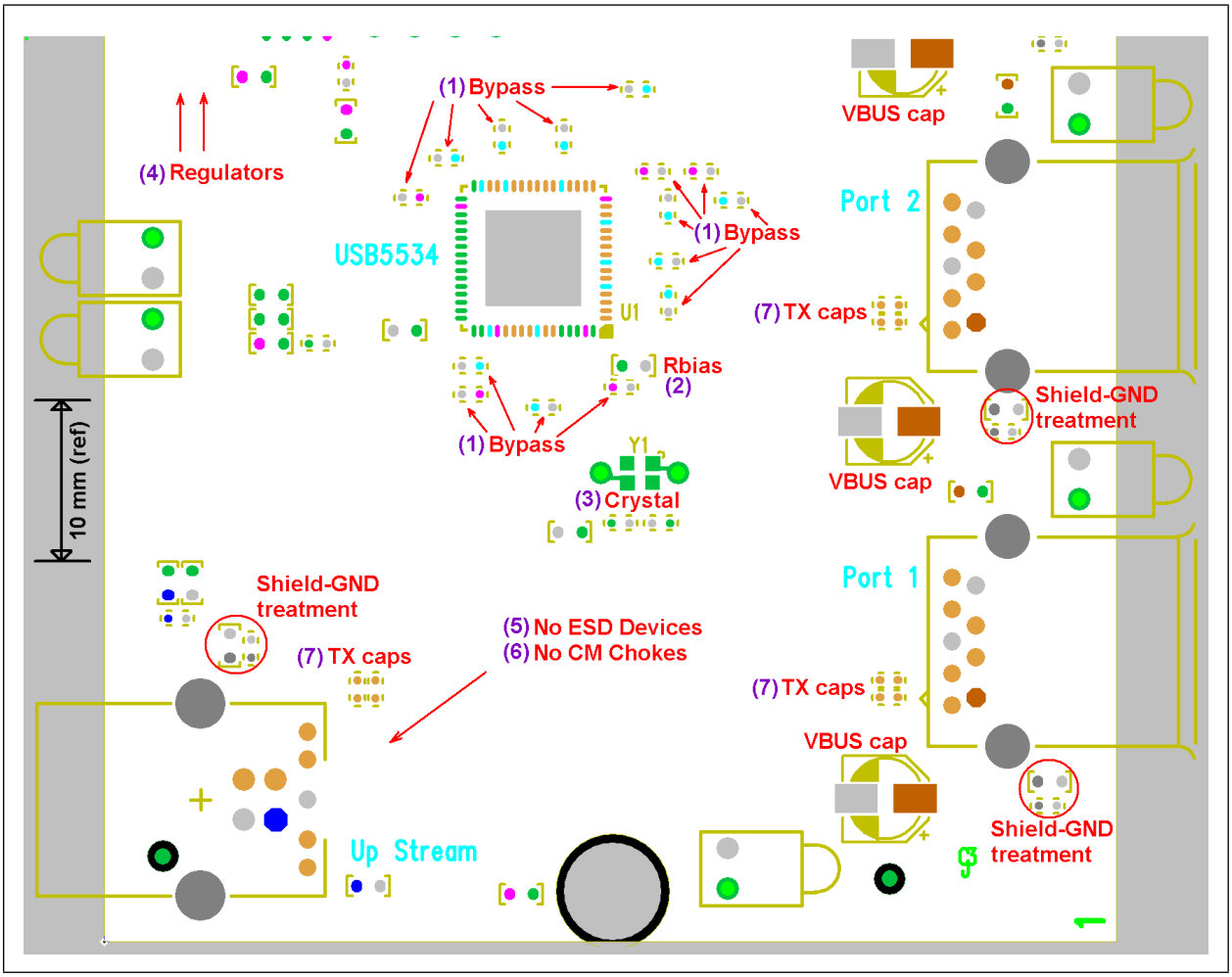
Specific requirements and suggestions for the PCB system implementation of the USB57x4 & USB553x family are indicated in this section.

3.1 Placement

Microchip USB hubs are designed to allow placement of all support components on the top side (the same side as the hub device) of the PCB. Be sure to prevent placement details from causing the signal routing to introduce unwanted currents into sensitive lines.

- Place the bypass capacitors as close as possible to the hub power pins. The 1.0 μF and larger capacitors indicated in the data sheets are part of the internal regulator circuits and should also be placed near the pins indicated. These capacitors are usually less effective if they are placed on the bottom of the PCB because of the intervening via inductances.
- Place the **RBIAS** resistor close to its pin.
- Place the crystal components near the related hub device crystal pins.
- Place electrically noisy devices, including switching regulators, far away from the hub device and support circuits. Avoid placing or routing noisy circuits near the sensitive **RBIAS** resistor, its signal trace, its ground return path, the crystal circuit, and the USB differential pair signals.
- ESD protection devices on the USB SuperSpeed lines will degrade SuperSpeed Signaling, and therefore should only be used if needed. Place any ESD devices for the USB lines near the USB connectors. Follow the manufacturer's recommendations for placement and use.
- Common mode chokes that are used for EMI or ESD purposes will degrade SuperSpeed (SS) signaling, and should only be used if proven to be needed. USB High-Speed (HS) Signaling is somewhat less sensitive. Both the SuperSpeed (SS) (USB 3.1 Gen 1) and High-Speed (HS) (USB 2.0 and 3.1 Gen 1) chokes must be chosen carefully and must match the USB differential impedance of 90 Ω. Manufacturers typically only specify the common mode impedance. Special devices are currently advertised for USB 2.0 and USB 3.1 Gen 1 use, but must be confirmed for use in each application.
- Place the **SS_TX** AC coupling capacitors near the USB connectors for more effective common-mode noise rejection. The USB specification calls out 0.1 μF ceramic capacitors for this application.

FIGURE 7: EXAMPLE ANALOG SIGNAL CONSIDERATIONS



3.2 PCB Construction

Elements of the PCB fabrication impact proper implementation of USB hub and hub-combo devices. USB SuperSpeed hub devices are particularly sensitive, due to their very fast signal rates.

3.2.1 PCB MATERIALS

Signal losses for copper traces running on FR-4 materials can be very significant at USB 3.1 Gen 1 and Gen 2 Super-Speed (SS) signaling rates. Any imperfections in routing, PCB fabrication, cables or other system elements will add other sources of loss and interference, reducing the potential line length maximum for the PCB routing or requiring the use of PCB material with lower Df (dissipation factor, also called loss tangent) ratings. The following list provides ways to mitigate these losses:

- Keep SS traces as short as practical, prioritizing the upstream port first. This is the single most practical and cost-effective solution for reducing signal loss.
- Route SS traces on outer layers, rather than on inner layers.
- Consider laminates with low Df ratings at 10 GHz. These lower loss materials include FR408HR, FR408HRIS, N4000-13SI, Rogers, Polyimide, etc. 370HR, NP-175 and IT-180 (or equivalent) with Df ratings of ~1.5 may usually be used for SS paths of 10 cm or less on carefully designed platforms.
- Try to route SS signals at a 45^{o} angle to the material weave direction so that the trace does not occasionally line up with a high-resin, high-loss path.
- Use materials with “tight” or “spread” weaves. Avoid materials with “open” weaves. Your PCB fabricator can help with this selection.

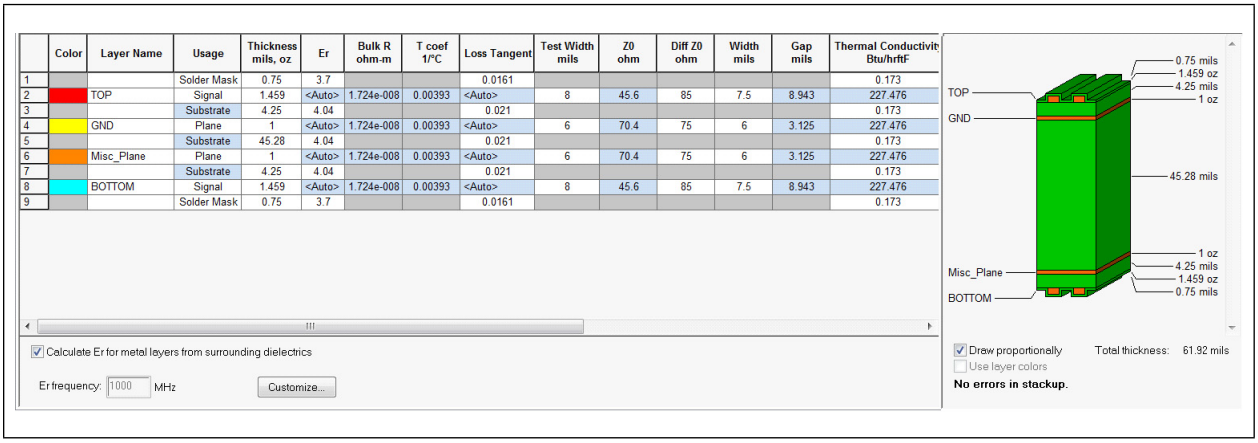
3.2.2 STACK UP

The pinouts of Microchip's hub devices allow for possible implementation on a two-layer structure. However, using more than two layers will provide greater control of impedances, return paths, and thermal management. The side on which the Microchip Hub device is mounted is designated layer one for reference.

- When designing with greater than two layers, assign ground to layer two and flood the bottom layer with ground. For two-layer structures, flood the bottom layer with ground. (*Note: A two-layer structure will require a heat spreader, heat sink, or other specific thermal management for many Microchip Hub and Hub-Combo devices.)
- Choose a thin dielectric between layer one and ground to simplify attaining accurate impedance for critical lines, especially for the USB differential pairs. Make the boards as thin as practical.
- Choose copper thicknesses of at least 1 oz./ft.^{2} to help with power delivery and thermal conduction.
- Use a trace width of 7.5 mil or wider for SS signals while maintaining the target Zdiff and Z0 to improve losses and control fabrication variants.

Figure 8 provides a sample stack-up for a 4-layer PCB structure using Isola 370HR laminate with Er and Dk values for 2 GHz:

FIGURE 8: EXAMPLE 4-LAYER PCB STACK-UP



3.2.3 IMPEDANCE CONTROL

Several signals in a USB hub design need to be impedance controlled, including the differential USB lines. Control the trace widths, spacings, copper thickness, and dielectric type and thicknesses to meet the following requirements:

- Control the single-ended characteristic impedance (Z0) of USB signals to between 40 Ω and 55 Ω.
- Control the differential impedance (Zdiff) of the DP/DM signals to 90 Ω, +5/-10 Ω.
- Control the differential impedance (Zdiff) of the SS_TX+/- and SS_RX+/- signals to 85 Ω, +10/-5 Ω
- The connection of bypass capacitors to their pins, and to power and ground, must be low inductance (short and very wide).
- Due to relatively high operational load currents (from 900 mA to several Amps), the VBUS path to each down-stream USB connector must be very low impedance.
- The **RBIAS** connection and return path need to be relatively low inductance (short).
- Adhere to the Section 3.4, "Power Distribution" guidelines.

3.3 Ground Distribution

The USB environment requires that the ground return paths across the system be implemented carefully and that they be substantial and contiguous. Connect ground floods on different layers with multiple vias and ensure narrow ground floods are terminated with a via at all flood corners and ends.

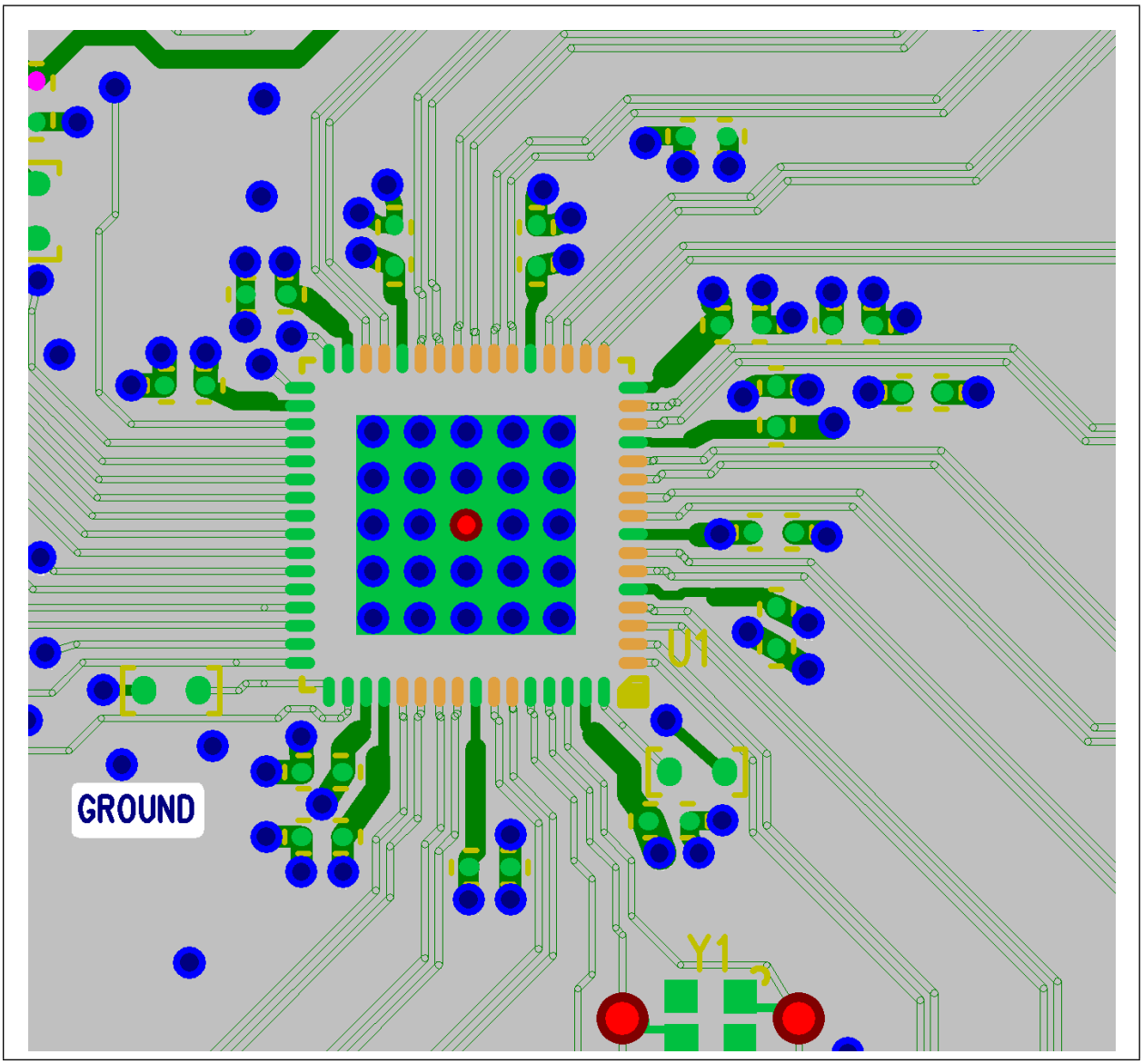
3.3.1 FLAG IS THE ONLY GROUND AND THERMAL PAD

QFN packages have one row of perimeter pads (*pads*) around a larger central pad (*flag* or *ePAD*) encapsulated in a plastic body. All ground connections from the Microchip Hub Controllers in QFN packaging are done through the device's *flag*. The flag is used for the following:

- The device's **only** signal ground (VSS)
- The primary thermal conduction path to remove package heat

To address these issues, constraints are imposed for the use of these packages, including filling the GND flag with a pattern of vias, especially around the periphery of the flag. Microchip strongly suggests using 1 oz. or higher copper weights on inner plane layers and 1.5 oz. or higher copper weights for outer layers, with a large, uninterrupted ground flood on the bottom layer.

FIGURE 9: EXAMPLE GROUND ON PLANE LAYER 3 WITH VIA FIELD IN FLAG PAD



3.3.2 RETURN PATH

A return path exists for each signal flowing between circuit nodes, and controlling these paths is advantageous. To control these paths, a solid ground plane on the layer just below the device is preferred. All ground floods should connect together and careful consideration should be given to the integrity of the return path for each signal connection.

3.3.3 BYPASS GROUND CONNECTIONS

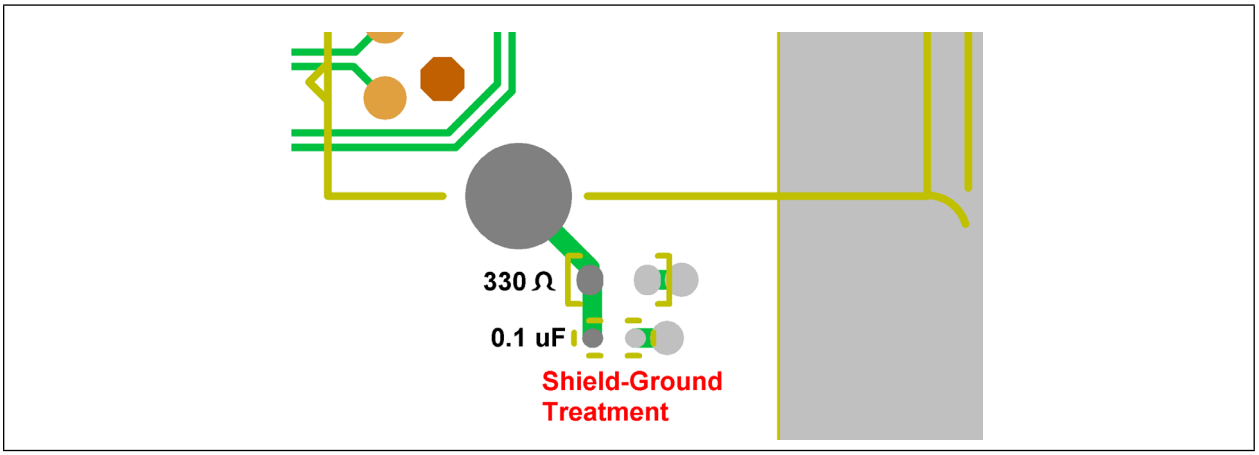
All ground connections from the bypass capacitors should be low inductance. To reduce bypass GND inductance:

- Make the fanout to ground short and wide.
- Place bypass vias within or as close as possible to the bypass capacitor pad.
- Use 0402 or smaller capacitors, where possible, that have lower package inductance.
- Use vias with as large a hole diameter as practical -- up to 0.5 mm FHS.
- Use multiple ground vias per capacitor to divide the effect of the fanout trace's and via's impedances (see **FIGURE 14: "Bypass Capacitors"**).
- For system bulk large value capacitors, use at least two vias to connect to power & ground.

3.3.4 CHASSIS GND CONNECTIONS

The shield of the USB connectors (Chassis Ground) must be considered carefully. Some kind of shield-ground isolation is usually desired for EMI or ESD reasons. Embedded systems may require a direct ground connection. An RC network of 330 Ω and 0.1 μF is used on most of Microchip's hub evaluation boards for this purpose.

FIGURE 10: EXAMPLE CHASSIS-GROUND CONNECTION



3.4 Power Distribution

3.4.1 HUB DEVICE POWER

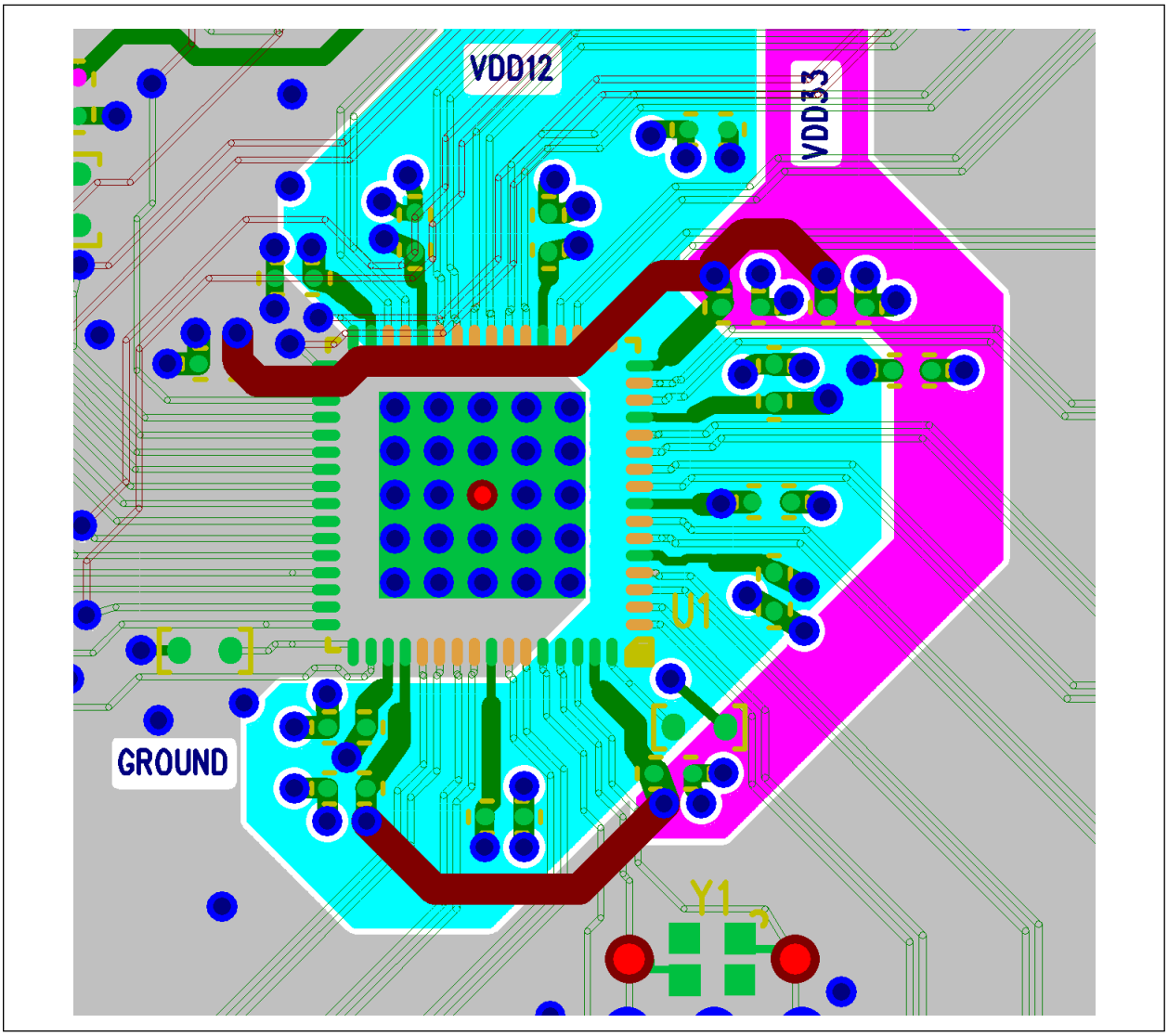
The USB57x4 & USB553x families of devices are supplied by both a VDD33 supply and a VDD12 supply (1.25V nominal). Microchip strongly suggests using four or more PCB layers. This greatly simplifies proper power delivery, as well as improved thermal management. Other Microchip hubs use a single VDD33 supply.

The sensitive analog circuitry inside the hub devices requires a clean power and ground system for best operation. Control supply ripple carefully and make sure that the supply voltages are within specifications for both light and heavy power loads at all power pins. The hub device will represent a light load to the power supply when it is in "suspend" and a heavy load when the device is running all downstream ports at their highest speed. See the applicable data sheets for details.

- A power plane or flood structure should be implemented to provide a low impedance path for each of the power rails to the Hub, especially for the VDD12 supply of USB57x4 & USB553x hubs which can draw 900 mA.
- Connect the Hub *flag* to the ground plane with many vias, especially around the periphery of the *flag*. (The ground *flag* is the device's only connection to signal ground [VSS].)

Figure 11 illustrates an example of good power distribution to the power pins using flood structures on a plane (layer 3). Note that layer 2 is a complete ground plane layer. The ground shown on layer 3 is to improve thermal and signal return performance of the board.

FIGURE 11: EXAMPLE POWER FLOODS ON PLANE LAYER 3



3.4.2 DISTRIBUTED USB POWER

VBUS is distributed to each downstream connector for use by attached devices. The current is limited by specification to +5 V, 900 mA for USB 3.1 Gen 1 ports and to 500 mA for USB 2.0 ports. Systems with battery charging enabled, or that comply with USB Power Delivery (PD), may supply even more current.

It is important that the power distribution meets the “droop” and “drop” elements of the USB specifications. Short and very wide paths, plus large value capacitors, are provided on the reference EVBs to satisfy this requirement.

3.5 Thermal Management

3.5.1 POWER CONSUMPTION

SuperSpeed Signaling drives the internal switching rates up for USB 3.1 Gen 1 devices vs. USB 2.0 devices. This, in turn, drives up the power consumption for USB 3.1 Gen 1 devices. Systems must prevent these devices from overheating.

For example, while operating at maximum capacity, the USB5534 consumes about 1.45 W of power. The USB5537 consumes slightly more.

3.5.2 QFN PACKAGE THERMAL PROPERTIES

QFN packages were chosen for these devices partly because of their excellent thermal properties and package sizes. The flag pad is very efficient at transferring heat to the PCB through a proper via field. This heat energy can then be pulled out of the system.

3.5.3 PLANES AND FLOODS

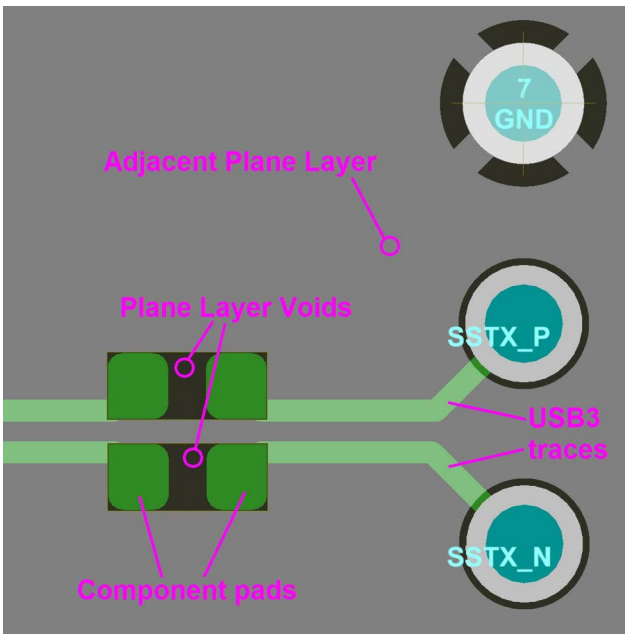
Generally, planes or flood structures should be used to deliver power and ground to the hub device, not only to help with power distribution, but to also improve thermal conduction.

Thermal guidelines for planes and floods:

- Specify a minimum of 1 oz./ft. copper for outer and plane layers.
- Flood the bottom layer with a solid ground at least 4 square inches in area.
- Fill the flag pad with a field of vias (See Figure 9).
- Fill inner layers with floods, preferably ground floods, in the region under and around the hub device.
- Flood the region around the hub device on the top layer with ground.
- Stitch all ground floods together with vias.
- For SS signals, void adjacent planes under wide component pads.

Be particularly careful to avoid impedance mis-matches along the SS paths. One source of impedance change is the pad geometry of any devices placed along the SS paths if they are wider than the SS trace width. These ‘wide’ pads and their components cause an impedance drop. A common technique to correct impedance drop from pads is to void the adjacent plane layer underneath the component pads.

FIGURE 12: VOIDED ADJACENT PLANES UNDER COMPONENT PADS



3.6 Routing

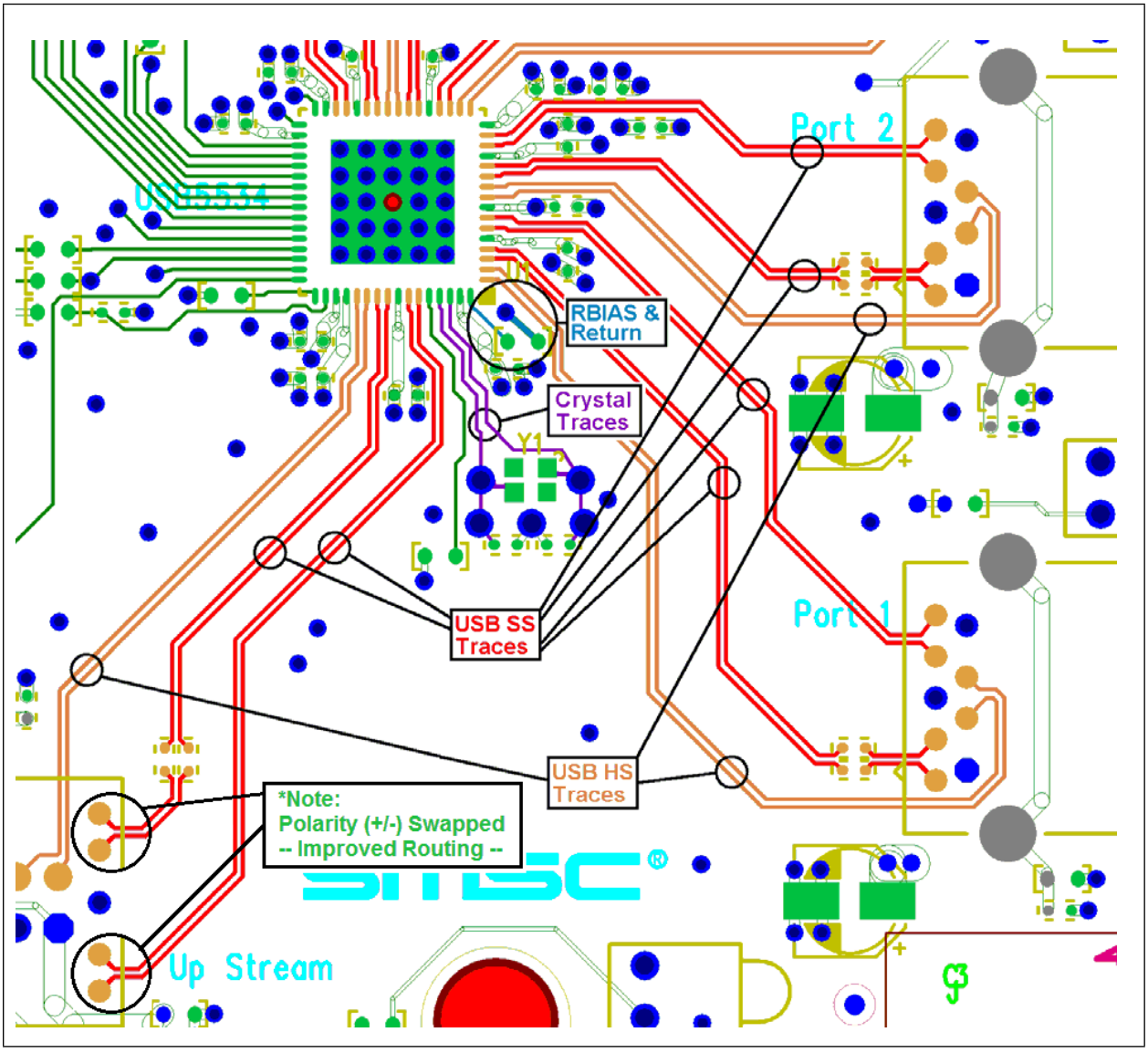
3.6.1 GENERAL ROUTING RULES

- Route critical signals over unbroken reference (power or ground) planes.
- Avoid 90 degree trace corners and use arcs or 45 degree mitered routing instead.
- Always consider the ground return path for each critical signal.
- SuperSpeed signal traces should not be within 5X trace width of the reference plane edge or of the splits in the ground/voltage plane.
- Remove unused pads on internal layers for component pins and for vias.

3.6.2 ANALOG SIGNAL CONSIDERATIONS

Isolate the current paths of each analog circuit (the USB signal pairs, crystal circuit, and **RBIAS** circuit) from each other. Also ensure that currents flowing through the digital VDD circuits are not also flowing through the analog VDDA circuits, including return currents. Control this with layout and placement, power/ground “moating”, circuit and ground isolation, or other techniques, as needed. See Figure 13.

FIGURE 13: ANALOG SIGNAL CONSIDERATIONS



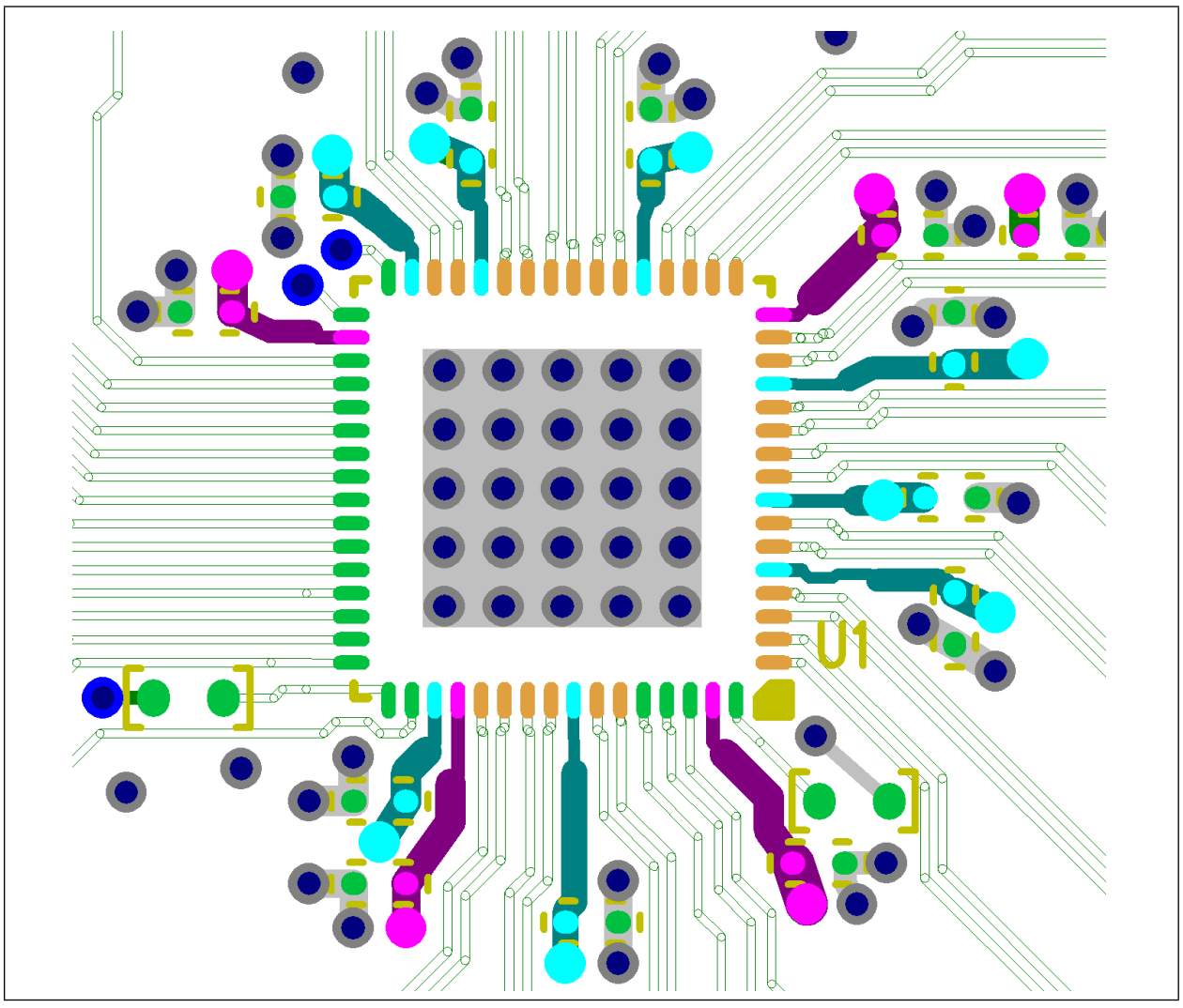
3.6.3 BYPASS CAPACITORS

Ideally, all of the capacitors used for bypass should be connected such that the power signal originates at the voltage rail source, then to the capacitor, then to the Hub Controller pin. Consider using double ground vias for each bypass capacitor to reduce the inductance of the connection. The power and ground traces to the bypass capacitors should be short and wide (low inductance).

MLCC capacitors of 0402 size or less have lower parasitic inductance and fit closer to the hub device pins, making proper placement easier. Use capacitors with appropriate temperature coefficients (Ex., X7R -- not Y5V).

Note:	The less the bypass routing conforms to this ideal, the less effective it will be.

FIGURE 14: BYPASS CAPACITORS



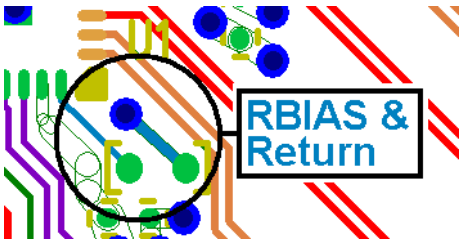
3.6.4 RBIAS RESISTOR

The USB57x4 & USB553x products use an external resistor to set a bias current for internal circuitry, similar to many other Microchip devices. This is a very sensitive analog input.

3.6.4.1 RBIAS Signal Routing

The resistor should be connected with a short trace to the **RBIAS** pin of the device to reduce signal coupling from other circuits.

FIGURE 15: RBIAS RETURN ROUTING

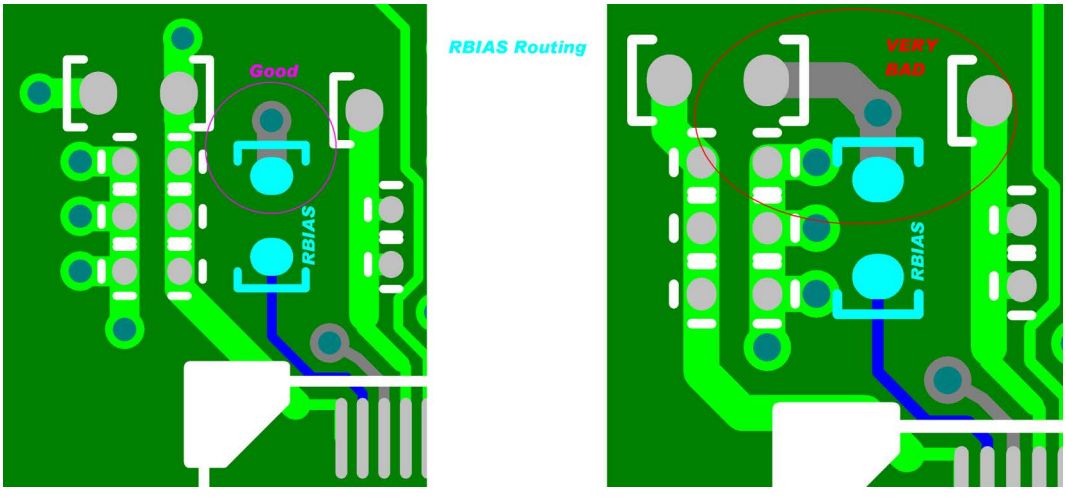


3.6.4.2 RBIAS Return Routing

The return ground on the **RBIAS** resistor should flow directly to the ground flag nearest to the **RBIAS** pin on the Hub controller.

Note:	The ground via on the **RBIAS** resistor, if any, should not be shared with any other devices, particularly the bypass capacitors.

FIGURE 16: RBIAS RETURN ROUTING



3.6.5 USB SIGNAL ROUTING

The USB lines are constrained by the USB 2.0 and USB 3.1 Gen 1 specifications. Critical conditions for the lines are detailed in this section.

3.6.5.1 USB Differential Impedance

The differential impedance of the USB differential pairs needs to be controlled to 90Ω (nominal). These paired signals are DP and DM for each USB 2.0 interface, and also SS_TX+ and SS_TX-, and SS_RX+ and SS_RX- for each USB 3.1 Gen 1 interface. See the applicable USB specifications for further details.

3.6.5.2 USB Differential Routing

These differential routing guidelines are critical for maintaining good signal integrity for the USB signals. Refer to Figure 13.

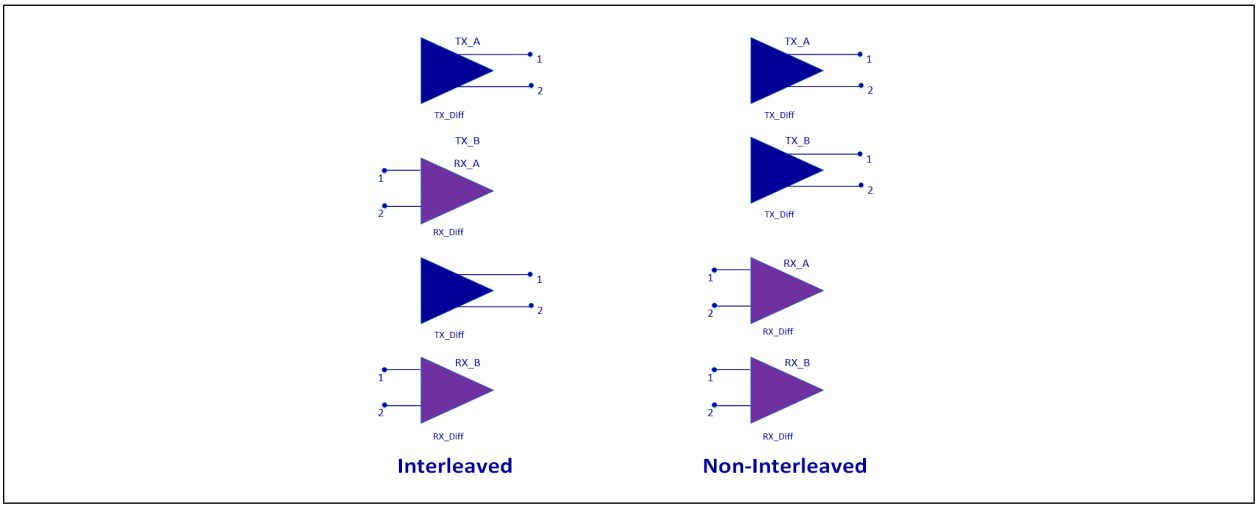
- All of the USB traces must be routed as differential pairs. Avoid using any stubs on these lines.
- The SuperSpeed (SS) USB signals may be routed with their polarity swapped to simplify routing. (E.g., RX- may be swapped with RX+ and /or may be swapped with TX+ for any port.) DP and DM on a particular port may only be swapped if PortSwap is configured for that port.
- The USB traces must not be exposed to cross-talk from adjacent lines. For this purpose we will define this gap in terms of either the USB trace width or the dielectric height between the signal and its reference plane, whichever is greater. 3X would be 3 times the width or height. 5X would be 5 times the width or height.

  For example, if the USB trace width is 8 mil and the dielectric height is 4.3 mil, the minimum gap to signals not in that pair would be 3 x 8 mil = 24 mil (3X). 5X would be 40 mil.

  If the USB trace width is 12 mil and the dielectric height is 22 mil, the minimum gap to signals not in that pair would be 3 x 22 mil = 66 mil (3X). 5X would be 110 mil.
- Maintain a routing spacing (gap) of at least 3X between High-Speed USB signals (DP and DM) to the signals outside of the USB pair.

  Maintain a routing spacing (gap) of as wide as practicable and at least 5X between SuperSpeed USB signals (RX+/- and TX+/-) to the signals outside of each USB pair. This means that the spacing between the RX signals and the TX signals and the DP/DM signals must be at least 5X. For example, if the differential spacing is 0.178 mm (7 mil), the minimum spacing to all signals not in that USB pair will be at least 0.89 mm (35 mil).
- Use non-interleaved routing for TX & RX through flat cables, inter-system connections, and otherwise where possible.

FIGURE 17: INTERLEAVED AND NON-INTERLEAVED TRACES

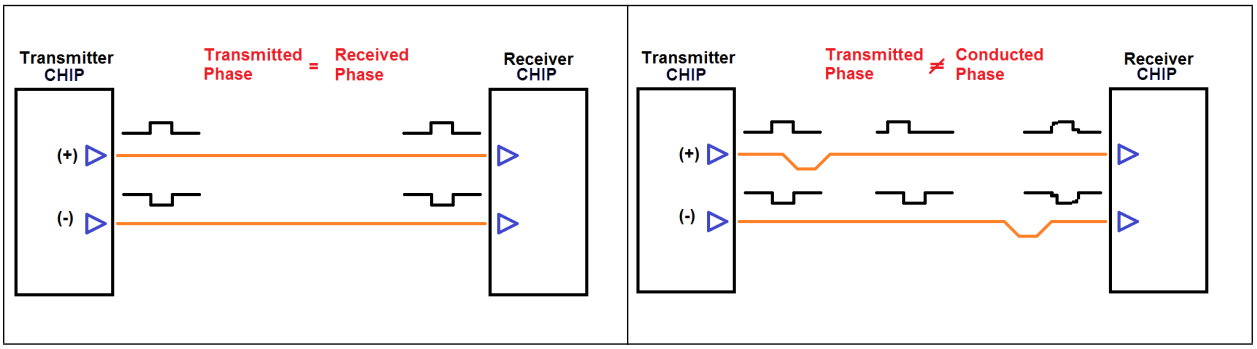


- The USB differential traces must be length-matched very carefully. Add any needed length so that minimal phase skew is introduced between pair members.

  Each member of a High-Speed differential pair should be no more than 1.25 mm (50 mil) longer than the other member. Each member of a SuperSpeed differential pair should be no more than 0.05 mm (2 mil) longer than the other member. The transmit differential pair (TX+ and TX-) does not have to be the same length as the receive differential pair (RX+ and RX-).
- Avoid 90 degree trace corners for USB signals and use arcs or 45 degree mitered routing instead.
- Route USB differential signals over unbroken reference (power or ground) planes.
- Keep USB pairs as short as possible to reduce signal loss. High Speed signal traces longer than ~15 cm (~6 in), and SS traces longer than ~10 cm (4”) may significantly degrade signal quality.
- Vias are not typically needed to route the USB signal pairs for Microchip hubs. Minimize the number of vias used and balance the number and placement of them between the signals within the pair if used.
- If vias are necessary for any SuperSpeed signals, add complementary ground vias. See Figure 20, "Length Matched Considering Phase".
- Add any need serpentines very near where the length error is introduced into the line.
- Add serpentine bends (meanders) at existing bends to reduce their negative effects. See Figure 20, "Length Matched Considering Phase".
- SuperSpeed signal elements must be kept in phase as the signal transitions across the PCB. Length matching must be corrected as errors are induced to maintain phase matching.

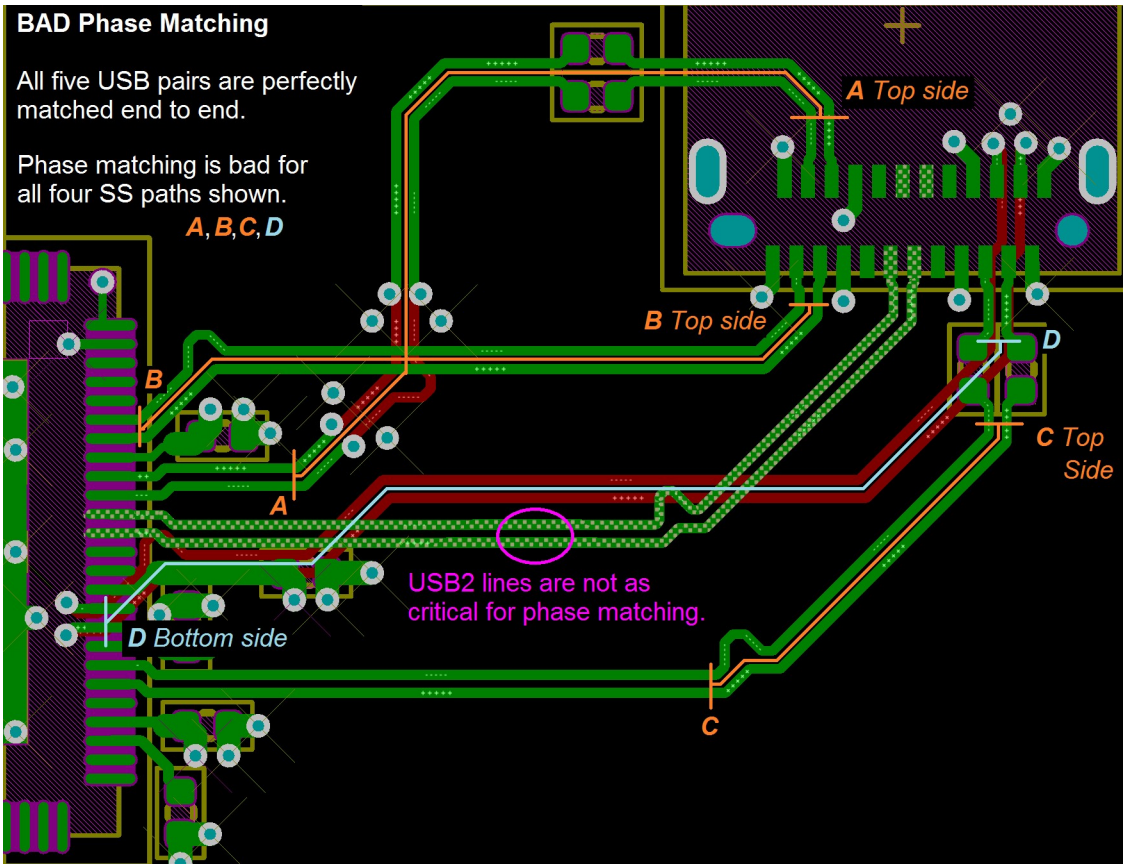
  The (+) and (-) lines of each SS signal pair are transmitted at the same time by the IC manufacturer and these signals will travel together across the entire system on two traces that make up a diff-pair transmission line to the destination IC for reception and decoding. If either trace is significantly longer than the other anywhere along the diff-pair path, it will be out of phase with the other. This will cause signal phase distortion as shown in Figure 18.

FIGURE 18: MATCH SIGNAL PHASE AND TOTAL LENGTHS TO REDUCE SS SIGNAL DISTORTION



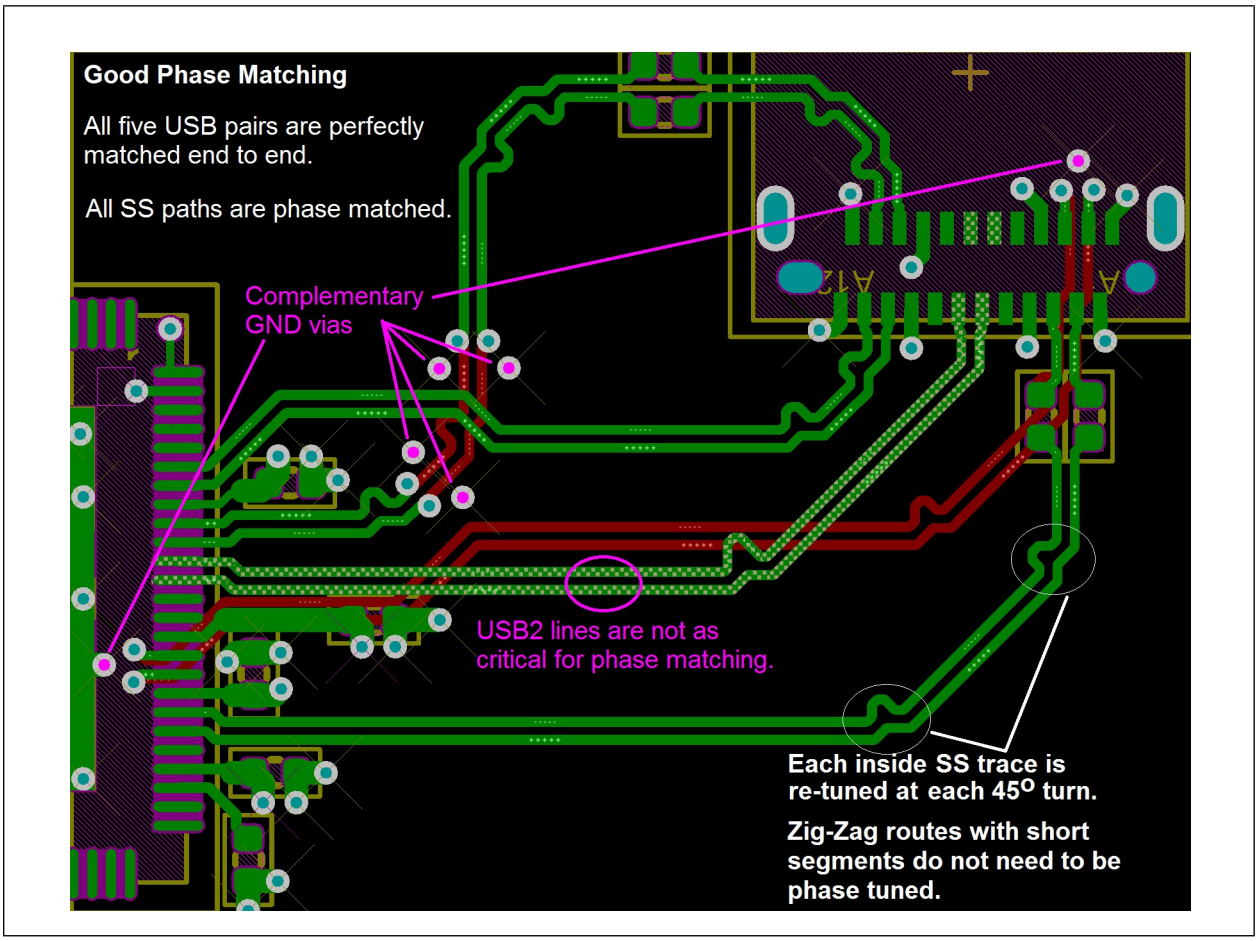
Here are two examples of “perfectly matched” sets of SS lines. The distortion of the SS signals in the first example significantly reduces the maximum system USB cable length that can be used.

FIGURE 19: LENGTH MATCHED WITHOUT CONSIDERING PHASE



The second example is FAR better, and allows a cable to be used that can exceed the USB-specified maximum.

FIGURE 20: LENGTH MATCHED CONSIDERING PHASE

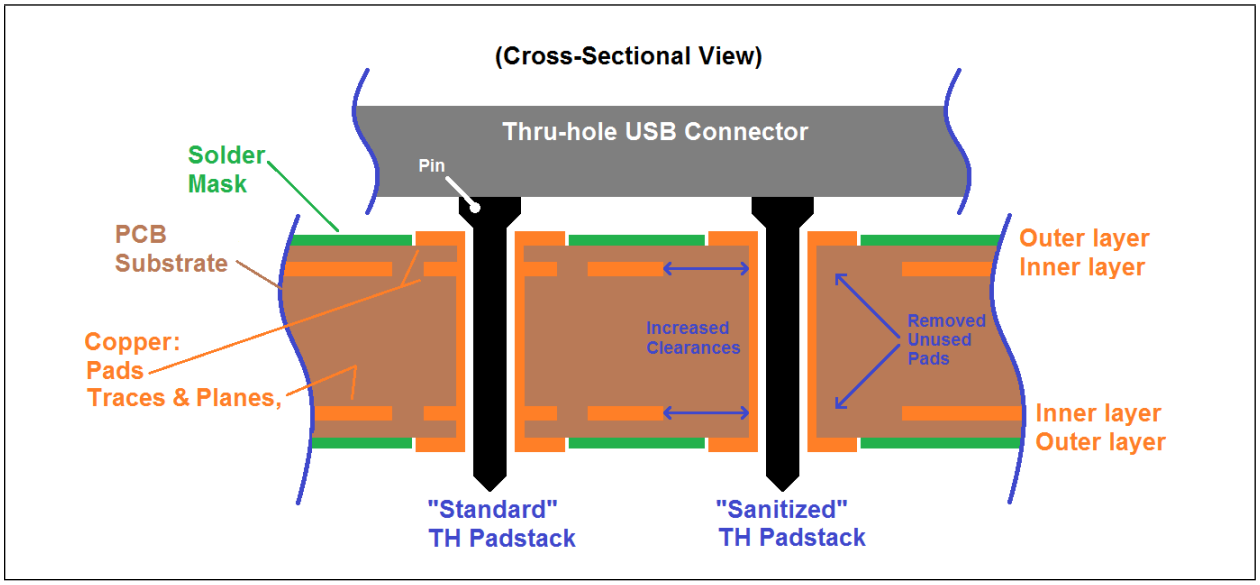


3.6.6 USB CONNECTORS

Selection of specific USB connectors can significantly impact the transmission line characteristics of the USB SS and HS signals. How the pin padstacks are defined and routed can also greatly impact USB transmission line integrity. These effects are more pronounced for USB 3.1 Gen 1 SuperSpeed signals than for USB 2.0 Hi-Speed signals.

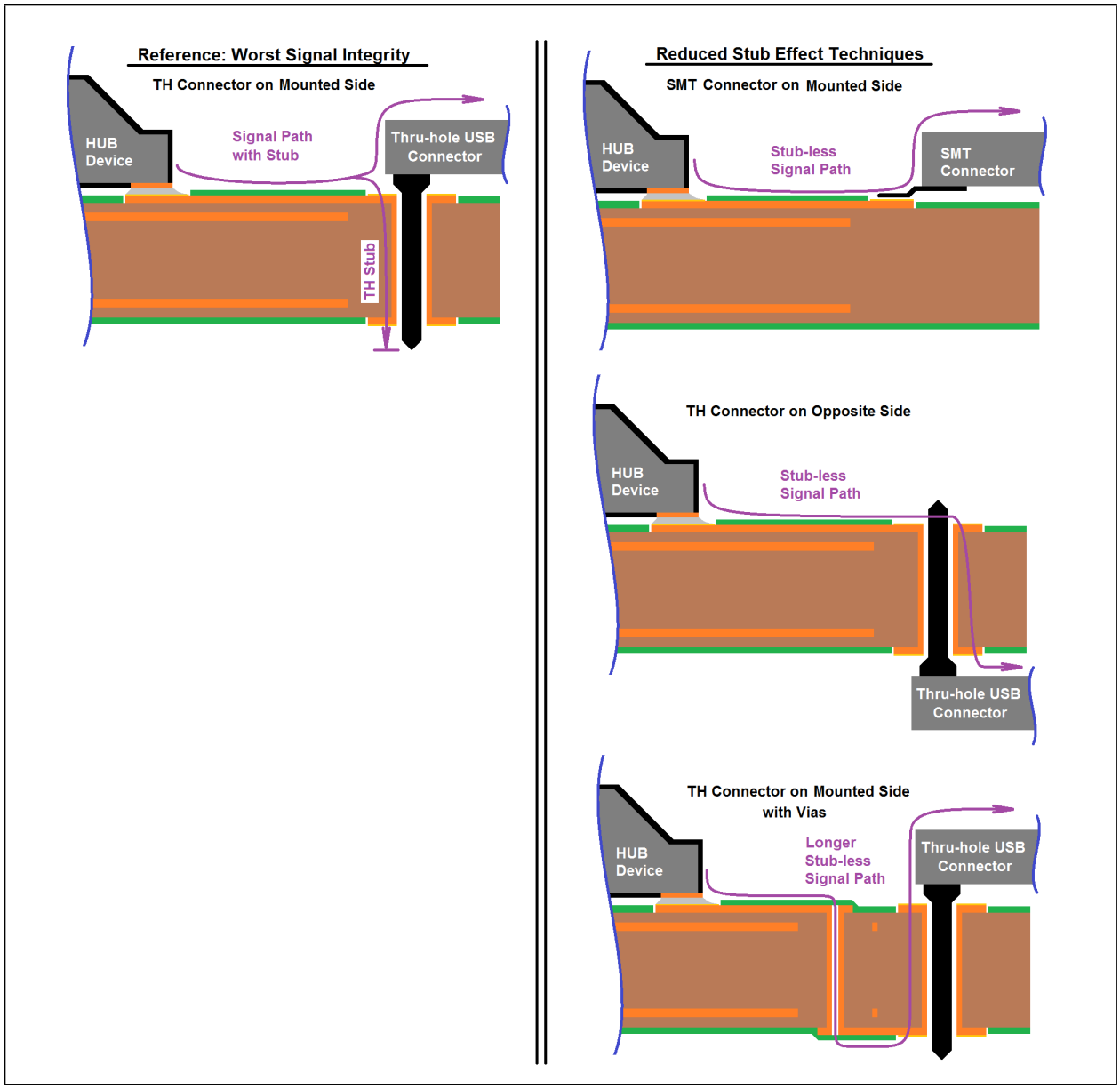
- If thru-hole (TH) USB connector(s) must be used, edit the thru-hole (TH) pad stacks of USB connector pins to simplify their effects on the USB transmission lines. (“Sanitize” the pad stacks.)
- Remove pin pads on unused layers to ease the task of controlling impedance discontinuities and capacitance caused by the hole geometries.
- Increase clearances around these pins to 0.5mm or more on all layers where possible.

FIGURE 21: “SANITIZING” A USB PIN PAD-STACK



- Reduce the stub effects of USB pins.

FIGURE 22: REDUCE THE STUB EFFECTS OF THRU-HOLE USB CONNECTOR PINS



- Transmission line characteristics of surface mount (SMT) USB connectors are easiest to control. Use surface mount USB connectors for optimal signal integrity.
- When possible, place any thru-hole USB connectors on the opposite side of the board from the USB hub -- especially on thicker PCBs -- to prevent the TH pins from acting as stubs that will degrade signal quality.
- Another method of controlling this stub effect is to use a via pair to allow the signal traces to enter the pin padstack on the side opposite the connector. This can be used when the USB connectors are placed on the same side as the hub device.

3.6.7 CRYSTAL OSCILLATOR

XTAL1 and **XTAL2** are the crystal oscillator connection pins. The circuit requires the use of two load capacitors. See the applicable data sheet for values and details.

Crystals for the USB57x4 & USB553x devices require a tolerance of +/- 30 ppm. See the applicable data sheet for additional details.

3.6.7.1 XTAL1 and XTAL2 Routing

The crystal oscillator pins should route directly to the crystal pins and their associated load capacitors, if required. Route foreign traces no closer than five times (5X) the minimum trace spacing to these traces.

A clock signal may be applied to the **XTAL1** pin instead of using a crystal. In this case, leave the **XTAL2** pin unconnected (open). See the applicable data sheet for voltage levels and other details of this clock signal.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001876D (02-09-24)		Replaced the following text in Section 3.2.3: “Control the differential impedance (Zdiff) of the SS_TX+/- and SS_RX+/- signals to 85 Ω, +5/-5 Ω” to “Control the differential impedance (Zdiff) of the SS_TX+/- and SS_RX+/- signals to 85 Ω, +10/-5 Ω”.
DS00001876C (09-18-19)	All	• Revised guidelines for USB3.1 Gen 2 implementation and expanded applicable product list to cover all High Speed and faster USB Hubs and Hub-Combo devices.
DS00001876B (08-05-15)	All	• Updated “USB 3.0” references to “USB 3.1 Gen 1” throughout the document
DS00001876A (01-05-15)	All	• Replaces previous SMSC version Rev. 2.0 (07-17-13) • Updated part references to include other Microchip families of USB hubs (USB57x4) • fixed grammar/syntax
	Section 2.3, "Power Sequence and RESET," on page 3	• Updated entire section, adding VDD12 and VDD33 power sequence information and figure
	Section 2.5, "VBUS_DET," on page 4	• Added additional sentence to first paragraph “The hub must be powered up, fully configured, and running before it receives the VBUS_DET signal for deterministic behavior.“
	Section 3.2.1, "PCB Materials," on page 7	• Added “...prioritizing the upstream port first.” to the first bullet.
	Section 3.2.2, "Stack Up," on page 8	• Added sentence “Use a trace width of 7.5 mil or wider for SS signals while maintaining the target Zdiff and Z0 to improve losses and control fabrication variants.”
	Section 3.2.3, "Impedance Control," on page 8	• Updated bullets for greater clarity
	Section 3.2.2, "Stack Up," on page 8 and Figure 8	• Removed EVB reference designs info and added sample stack-up Figure 8 and description
	Section 3.3, "Ground Distribution," on page 9	• Updated second sentence of first paragraph for clarity
	Section 3.3.1, "Flag is the Only Ground and Thermal Pad," on page 9	• Added “Microchip strongly suggests” to beginning of last sentence before Figure 9
	Section 3.3.3, "Bypass Ground Connections," on page 10	• Added cross-reference to Figure 14 in bullet: “Use multiple ground vias per capacitor to divide the effect of the fanout trace’s and via’s impedances (see **FIGURE 14: “Bypass Capacitors”**).” • Added bullet: “For system bulk large value capacitors, use at least two vias to connect to power & ground.”
	Section 3.4, "Power Distribution," on page 10	• Moved location of Figure 11

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
	Section 3.4.2, "Distributed USB Power," on page 11	• Removed “electrolytic” from capacitor description in second paragraph.
	Section 3.5.1, "Power Consumption," on page 12	• Modified sentences for clarity
	Section 3.6.1, "General Routing Rules," on page 13	• Updated section
	Section 3.6.4.1, "RBIAS Signal Routing," on page 15	• Updated Figure 15
	Section 3.6.5.2, "USB Differential Routing," on page 16	• Updated section with new information
	Section 3.6.6, "USB Connectors," on page 20	• Updated first three bullets
Rev. 2.0 (07-17-13)	Section 2.6, "In-System OTP Programming," on page 5	• Updated first sentence and added info on Pro-Touch tools • Updated section to more clearly define programming
	Section 3.6.6, "USB Connectors"	• Added sentence to end of paragraph
	All	• Updated references to parts to include other SMSC families of USB hubs (USB25xx and USB46xx)
	FIGURE 4: Stand-Alone VBUS_DET Connection on page 4	• Updated figure and sentence before to indicate a suggested 2.2 µF capacitor
	FIGURE 5: Embedded VBUS_DET Connection on page 4	• Updated figure to generic use case
	Section 2.6, "In-System OTP Programming," on page 5	• Updated section name • Updated SM_DAT and SM_CLK pull-down values • Updated figure title
	OCS Capacitors Section	• Removed OCS capacitors information
	Section 3.2.3, "Impedance Control," on page 8	• Updated item 1.
	Section 3.4.2, "Distributed USB Power," on page 11	• Added “...and to 500 mA for USB 2.0 ports” to the first sentence.
Rev. 1.1 (02-01-13)	All	• Co-branded document with Microchip logo, modified legal disclaimer • Corrected typos
	FIGURE 7: Example Analog Signal Considerations on page 7, FIGURE 13: Analog Signal Considerations on page 13	• Figures updated
	Section 3.6.6, "USB Connectors"	• New section created
Rev. 1.0 (04-23-12)	Initial release	

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