Application Note
Using Jumbo Packets with SimpliPHYs

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document.

2 Introduction

The IEEE 802.3 Ethernet standard specifies the maximum packet size that must be supported by a compliant 10/100/1000BASET/1000BASE-X PHY to be 1522 bytes. However, in order to increase the overall throughput of the link, system manufacturers may require that the Switch/MAC and PHYs support Jumbo packets, that is, packets with sizes greater than that allowed by the IEEE 802.3 standard.

Supporting Jumbo packets with Vitesse's SimpliPHYs depends on a number of variables such as:

- Reference clock offset of Local PHY.
- Reference clock offset of Link Partner PHY.
- Reference clock offset of Switch/MAC.
- Link speed – 10/100 or 1000.
- MAC/PHY interface standard – GMII, RGMII, TBI, RTBI, MII, 1000BASE-X, SGMII.
- PHY model – VSC8201, VSC8204, VSC8211, VSC8221, VSC8224, VSC8234, VSC8244.

However, by carefully implementing the guidelines found in this application note, systems designers can enable the use of Jumbo packets of varying sizes on system using Vitesse's SimpliPHY transceiver series.

All the constraints regarding Jumbo packet support specified in the following sections assume that the link partner PHY's reference clock is IEEE 802.3 compliant (that is, within the offset tolerance limits of ±100ppm). Reference clock tolerances worse than ±100ppm reduce the jumbo packet size directly.

3 Using Jumbo Packets in 1000BASE-T/1000BASE-X Mode

3.1 MAC Interface – GMII, RGMII, TBI, RTBI

In these modes, the maximum jumbo packet size supported depends on the frequency offset of the reference clock of the MAC/Switch connected to the Vitesse PHY from the ideal 25 MHz or 125 MHz frequency. Since this can be controlled on a system board, jumbo packets up to 16,000 bytes can be supported. This is summarized in the following table.

Table 1 • Frequency Offset vs. Max Packet Length

Vitesse PHY	Switch/MAC Reference Clock Offset Limit (ppm)	Max Packet Length (bytes)
VSC8201/VSC8204/VSC8211/VSC8224 /VSC8244	Less than ±12	16,000
	±78	10,000
	±86	9,600
	±100	8,989

To enable Jumbo packet support in these modes, set MII Register bits 24.9:7 to '011'.

3.2 MAC Interface – SerDes/SGMII

In these modes, the maximum jumbo packet size supported depends on two factors:

- The frequency offset of the reference clock of the local Vitesse PHY from an ideal 25 MHz or 125 MHz frequency.
- The frequency offset of the reference clock of the local Switch/MAC from an ideal 25 MHz or 125 MHz frequency.

The maximum size of the Jumbo packet supported will depend on the worse of the two aforementioned factors, so it is recommended that the local Vitesse PHY and the Switch/MAC be driven with a common clock source.

Since these can be controlled on a system board, jumbo packets of up to 16,000 bytes can be supported. This is summarized in the following table.

Table 2 • Frequency Offset vs. Max Packet Length

Vitesse PHY	Local PHY Reference Clock Offset Limit (ppm) and Local Switch/MAC Reference Clock Offset Limit (ppm)	Max Packet Length (bytes)
VSC8211/VSC8221 //VSC8234	Less than ±12	16,000
	±78	10,000
	±86	9,600
	±100	8,989

To enable Jumbo packet support in these modes, set MII Register bits 24.9:7 and 24.6:4 to '011'.

4 Using Jumbo Packets in 10/100BASE-T or 100FX Mode

4.1 MAC Interface – MII

The size of Jumbo packets supported in this mode does not depend on the clock frequency offset of the local and link partner devices forming the 10/100BASE-T or 100FX link. In the 10/100BASE-T or 100FX mode, the Vitesse PHYs support Jumbo packets up to 13,000 bytes.

Refer section Enabling Jumbo Packet Support in 10/100BASE-T or 100FX Mode for details on configuring the PHY to support Jumbo Packets in this mode.

4.2 MAC Interface – RGMII

In this mode, the maximum jumbo packet size supported depends on the clock frequency offset between the local Vitesse PHY and MAC/Switch connected to it. Since this can be controlled on a system board, jumbo packets can be supported. This is summarized in the following table.

Table 3 • Frequency Offset vs. Max Packet Length

Vitesse PHY	Clock Frequency Offset between Vitesse PHY and RGMII MAC/Switch (ppm)	Max Packet Length (bytes)
VSC8201/VSC8204/ VSC8211 /VSC8224/VSC8244	0 (common clock between MAC/Switch and PHY)	13,000
	40	9,600
	100	3,795
	200	1,898
	250	1,522

Refer section Enabling Jumbo Packet Support in 10/100BASE-T or 100FX Mode for details on configuring the PHY to support Jumbo Packets in this mode.

4.3 MAC Interface – SGMII (at 10/100 Mbps speed)

Jumbo Packets are not supported in this mode.

4.4 Enabling Jumbo Packet Support in 10/100BASE-T or 100FX Mode

The Vitesse PHYs support Jumbo packets up to 13,000 bytes in these modes. The steps to enable Jumbo Packet support in 10/100BASE-T or 100FX mode are listed as follows.

VSC8201

Enabled by default.

VSC8204

Enabled by default.

VSC8211

The following PHY register writes must be done:

- Write 0x2A30 to PHY Register 31.
- Write 0x0212 to PHY Register 8.
- Write 0x52B5 to PHY register 31.
- Write 0x0000 to PHY Register 2.
- Write 0x0E35 to PHY Register 1.
- Write 0x9786 to PHY Register 0.
- Write 0x2A30 to PHY Register 31.
- Write 0x0012 to PHY Register 8.
- Write 0x0000 to PHY Register 31.

VSC8224/VSC8244

The following PHY register writes must be done:

- Write 0x2A30 to PHY register 31.
- Write 0x0212 to PHY Register 8.
- Write 0x52B5 to PHY register 31.
- Write 0x0000 to PHY Register 18.
- Write 0x0E35 to PHY Register 17.
- Write 0x9786 to PHY Register 16.
- Write 0x2A30 to PHY Register 31.
- Write 0x0012 to PHY Register 8.
- Write 0x0000 to PHY Register 31.

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