MicroNotes

MicroNote #030

by:

Kent Walters
&
Al Russo

Metallurgical Bond Evaluation Methods for Diodes

Metallurgical bond evaluations of diodes have been a subject of interest for many years. It has stimulated the use of additional evaluation tools and methods over the last decade that are still evolving. This MicroNOTE will provide some added background and information on this topic.

Metallurgical bonding requirements for Category I, II, or III are defined in MIL-PRF-19500, Appendix A, paragraph A.3.19. Destructive Physical Analysis (DPA) procedures also exist to determine when bonds are acceptable. This has involved the MIL-STD-1580A and B revisions entitled "Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts", as well as method 2101 in MIL-STD-750 for diodes. In some respects, there have been notable differences between them that may have also resulted in different dispositions of DPAs. However with recent changes in MIL-STD-1580B including a section for "Detailed Requirements for Glass Bodied Diodes", these two methods now better support one another. We will review some of the previous possible conflicts and how they are now resolved.

The oldest method for bond evaluation involving MIL-STD-1580A provided for cross-sectional analysis with a minimum of 50% bond criteria of the available area. It did not separately recognize any of the three different metallurgical bond categories now identified in MIL-PRF-19500. This criterion may have been misleading unless multiple cross-sections were also performed.

The MIL-STD-750, Method 2101 is entitled "DPA Procedures for Diodes". It supports MIL-PRF-19500 by recognizing all three metallurgical bond categories and their different requirements. Although cross sectioning is still included for design verification in method 2101, it is not intended for the exclusive disposition of bond voids in the same manner as MIL-STD-1580A previously did. For example, method 2101 also provides a scribe-and-break procedure for glass-axial-lead and surface-mount diodes. It also recognizes thermal impedance as a bond indicator, particularly for Category III where cross-sectional analysis or scribe-and-break methods may not be as definitive.

This latter Category III example is where a "diffusion bond" is provided only between the outermost metallization layer of the elements being joined as defined in MIL-PRF-19500M, Appendix A. For Category I or II, the scribe-and-break method typically reveals the strength of the bond regions by showing pulled silicon at a die interface. If the glass package envelope contacting the die causes the silicon to break in an undesired location, the broken device may be further analyzed as described below.

The "Silver button with braze" construction is an example specifically defined in Method 2101 as a Category II metallurgical bond. Bonding in these products by Microsemi is achieved with braze preforms between the die and plugs. The preforms are designed to melt in a controlled manner during the sealing/braze process. When evaluations were sometimes made with the older MIL-STD-1580A, random voids in individual cross-sectional planes could appear to be 50% or greater. However when the entire die is removed and the actual bond is measured, there has been consistently greater than 60% bonds in Microsemi evaluations. This has also been confirmed by cross sectioning at a 2nd and 3rd plane (see *figures 1, 2, and 3* examples) as well as by using an additional scribe, break, and dig procedure.

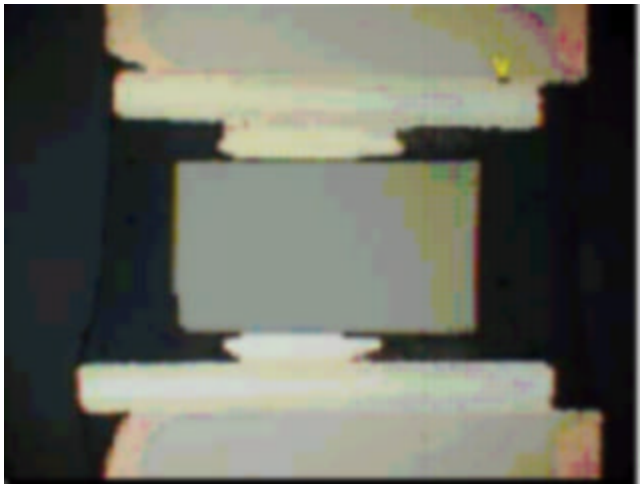

Figure 1
(25% location through die)

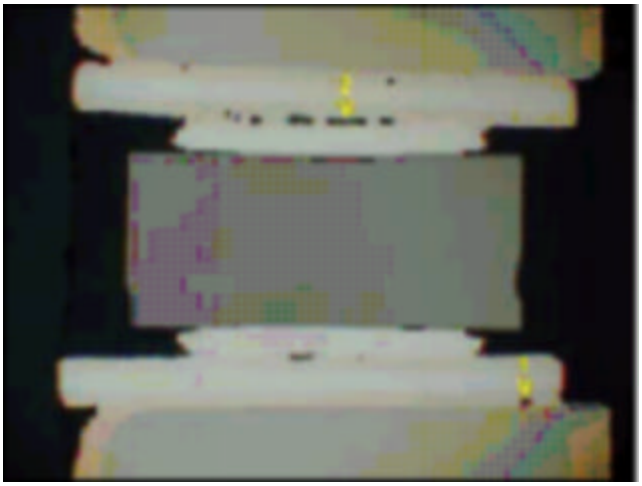

Figure 2
(50% location through die)

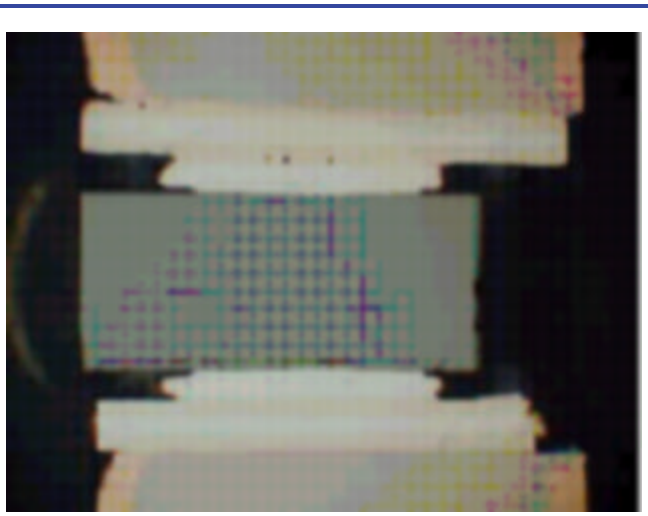

Figure 3
(75% location through die)

Although not a requirement of Method 2101 for scribe and break, Microsemi has also evaluated each bond by scraping or digging through all of the bond interfaces. All of these evaluations reveal bonding areas well beyond the requirements of Method 2101. To demonstrate this, Microsemi evaluated 3 devices that were cross-sectioned from a JANS assembly lot. These cross-sectional photos can sometimes exhibit bond-area voids at a single plane that exceed 75% as seen in *figures 4* and 5. Microsemi then performed a scribe, break, scrape, and dig procedure on additional samples to evaluate all of the device interfaces such as in *figures 6 and 7*. By taking the photo of the worst interface (*figure 7*), and running an imaginary line through it in various planes to simulate a cross-section photo, one can see the pitfalls of cross-sectional analysis

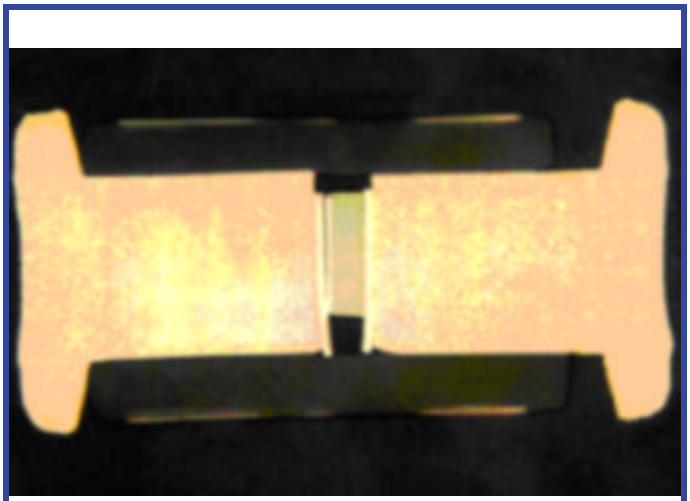

Figure 4

by itself as an acceptance tool as previously referenced in the older MIL-STD-1580A if done only on one plane.

Cross sectioning in a single plane is useful, but not as a stand-alone method for bond evaluation. This handicap also applies to other assembly designs including solder-bond contacts defined in Category II or diffused bonds in Category III. The MIL-STD-750 Method 2101 recognizes these limitations and offers other methods of confirming bond integrity. This includes scribe-and-break and thermal impedance testing to ensure thermal transfer qualities out of the die-bond region as described in MIL-STD-750, Method 3101. These additional analytical tools are also now cross-referenced in the latest revision of MIL-STD-1580B as described earlier.

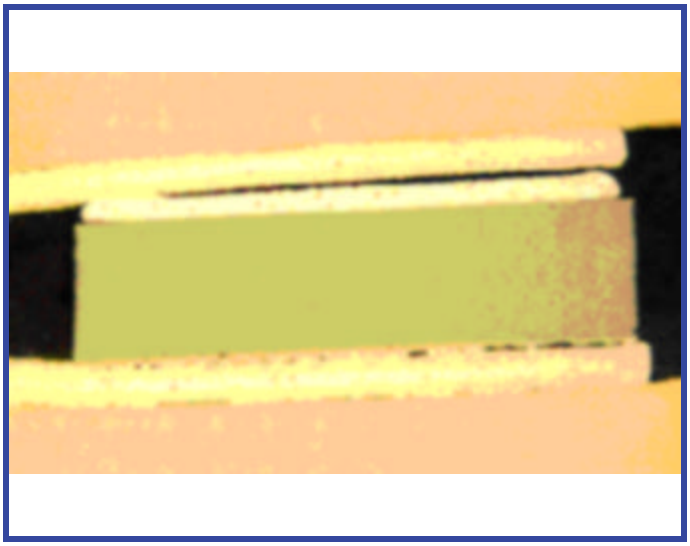

Figure 5

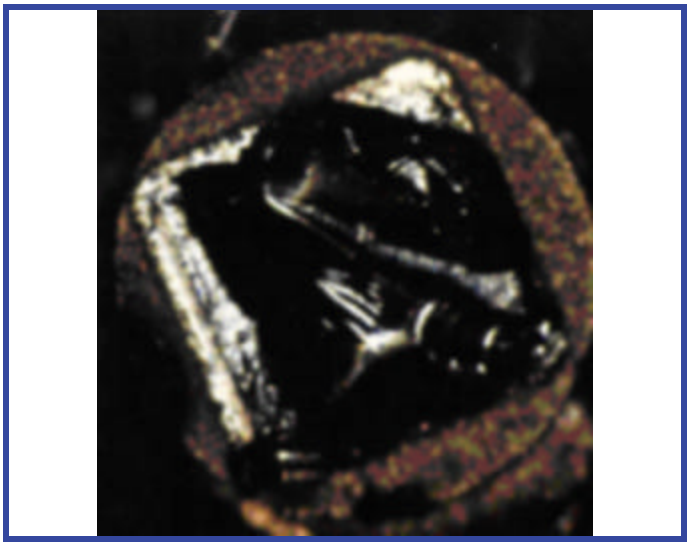

Figure 6

There are also many other considerations for a good quality bond analysis when using cross sectioning for glass encapsulated voidless construction such as those with Tungsten slugs for Category I bonds. For example, scribe-and-break techniques may not be practical for bond analysis since silicon will often shatter with these voidless designs. During cross sectioning, particular care must be taken to prevent inducing voids from die to slug during initial grinding when micro fracturing of silicon silicides occur from variations in the type of abrasive, grinding direction, pressure, etc. Also care must be taken to prevent crack damage during cross sectioning. For more details, refer to *Microsemi MicroNOTE 035* entitled "Metallographic Cross-Sectioning Techniques for the Performance of DPA of Glass Encapsulated Voidless Construction Diodes".

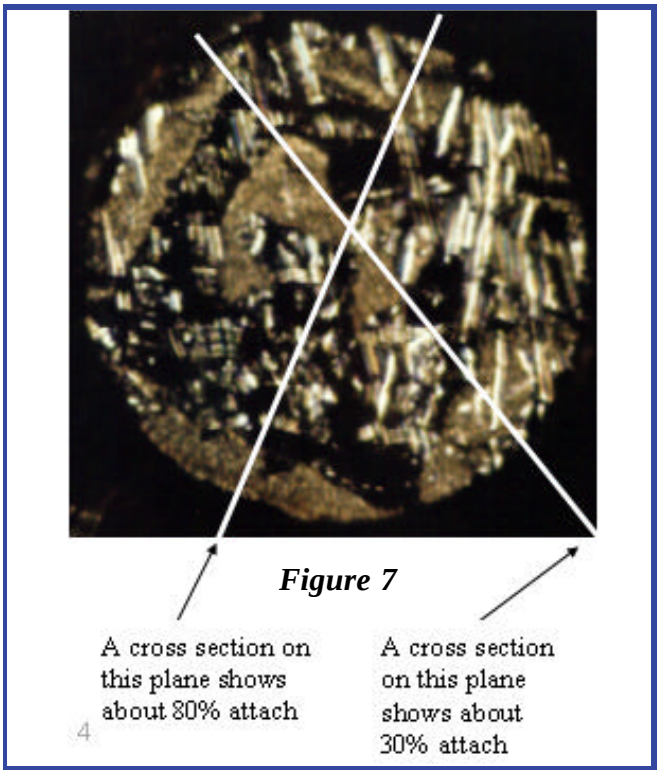

Figure 7