TB3272

Getting Started with External High-Frequency Oscillator on AVR® DB MCUs

Introduction

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The External High-Frequency Oscillator (XOSCHF) enables the use of an external crystal or an external clock signal up to 32 MHz. This can be used as a clock source for the Main Clock (CLK_MAIN), the Real-Time Counter (RTC), and the 12-Bit Timer/Counter Type D (TCDn).

The Clock Failure Detection (CFD) feature can be used to detect if the output from a clock source stops, and can switch the Main Clock to a different clock source to continue operation or shutdown operation safely. This feature is most useful in applications where XOSCHF is in use, for instance to allow safe shutdown of a Functional Safety application.

This technical brief describes how the XOSCHF and CFD is used on the AVR® DB family of microcontrollers and covers the following use cases:

- **XOSCHF with External Crystal:**
  Initialize XOSCHF for external crystal and change the main clock source to XOSCHF.
- **XOSCHF with External Clock:**
  Initialize XOSCHF for external clock signal and change the main clock source to XOSCHF.
- **RTC with XOSCHF:**
  Use XOSCHF as clock source for the RTC.
- **TCD with XOSCHF:**
  Use XOSCHF as clock source for TCD0.
- **TCD with XOSCHF and PLL:**
  Initialize the PLL with XOSCHF as clock source and use the PLL as clock source for TCD0.
- **CFD on XOSCHF:**
  Initialize the CFD to monitor XOSCHF, enable the interrupt, and toggle an LED if the clock source fails.
- **CFD on Main Clock with NMI:**
  Initialize the CFD to monitor Main Clock with XOSCHF as clock source, enable the interrupt as a Non-Maskable Interrupt (NMI), and toggle an LED with frequency derived from Main Clock.

The code examples are available in GitHub:

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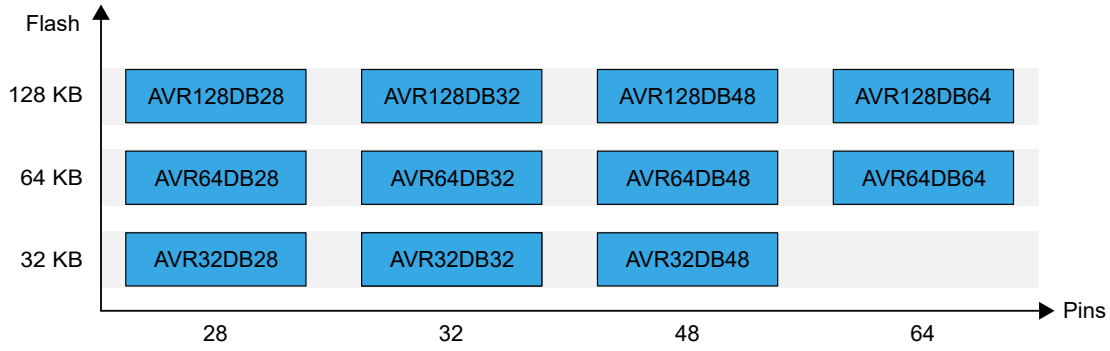
Table of Contents

1. Relevant Devices

This section lists the relevant devices for this document. The following figures show the different family devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features
- Horizontal migration to the left reduces the pin count and, therefore, the available features
- Devices with different Flash memory sizes typically also have different SRAM and EEPROM

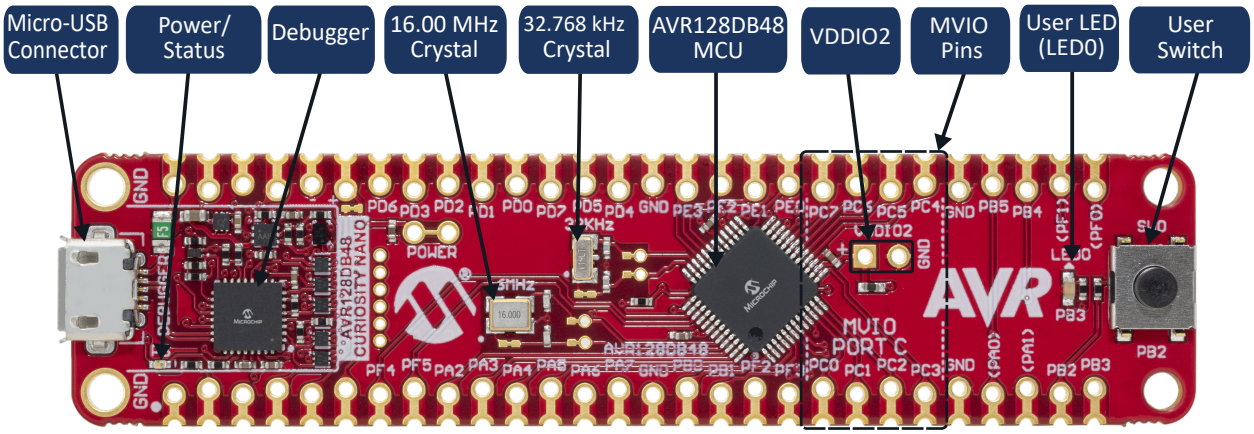
Figure 1-1. AVR® DB Family Overview



2. Hardware Configuration

The code examples were developed on the AVR128DB48 Curiosity Nano (EV35L43A) development board. It has a 16 MHz crystal on the board that can be used for most of the use-cases in this technical brief. The crystal must be disconnected if using the board with an external clock signal.

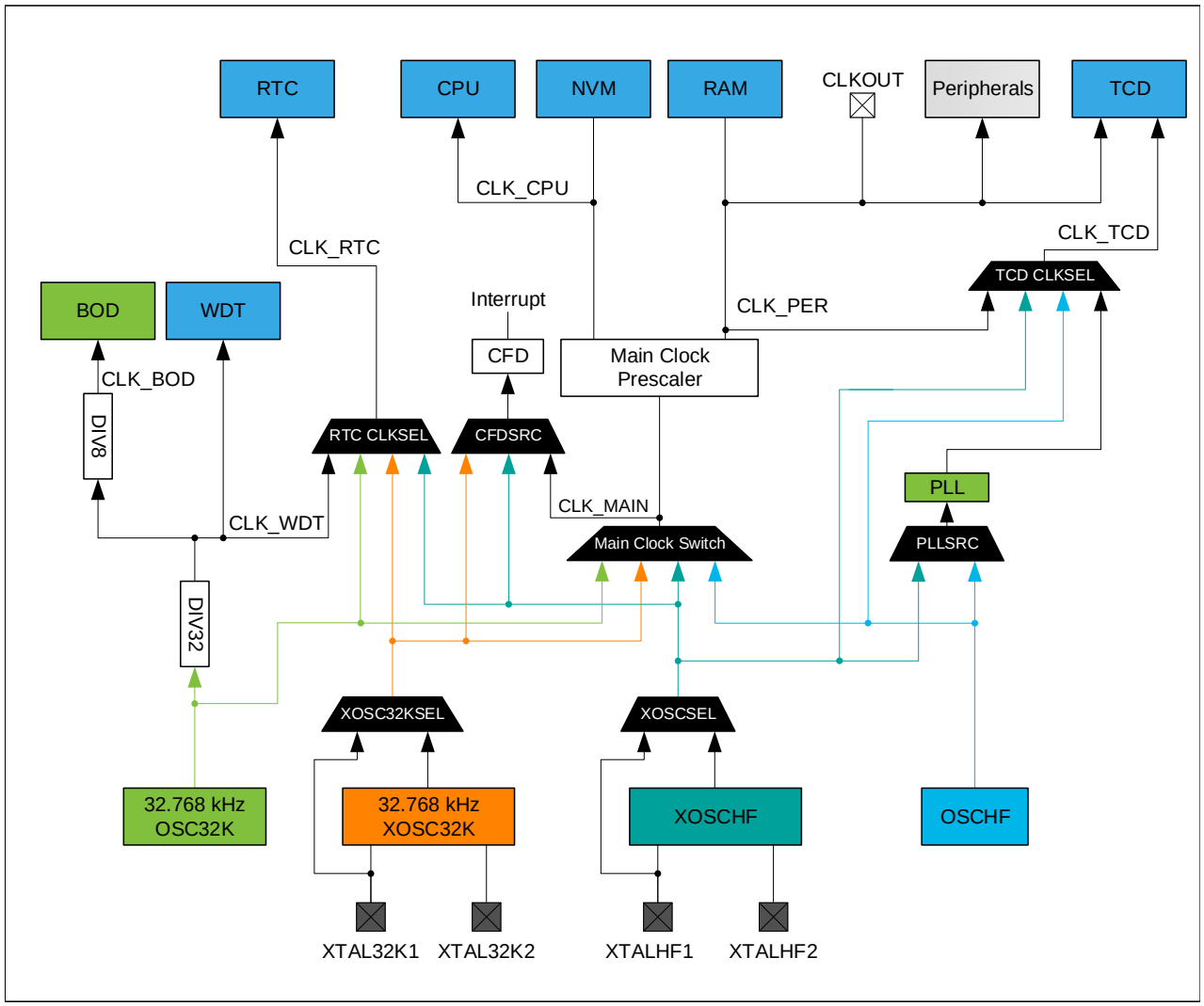
Figure 2-1. AVR128DB48 Curiosity Nano (EV35L43A) Development Board



3. Overview

The Clock Controller (CLKCTRL) block diagram shows how XOSCHF can be routed in AVR® DB family devices, as explained in the following sections.

Figure 3-1. CLKCTRL Block Diagram



4. XOSCHF with External Crystal

To use XOSCHF with external crystal, the SELHF bit in the External High-Frequency Oscillator Control A (CLKCTRL.XOSCHFCTRLA) register must be written to '0' and the ENABLE bit must be written to '1'.

In addition, the Frequency Range (FRQRANGE) bit field must be written to a setting equal to or higher than the frequency of the connected crystal, and the Crystal Start-up Time (CSUTHF) bit field can be written to select the number of cycles to wait before the clock is considered stable.

To make sure the oscillator runs as expected before it is requested by any modules, the Run Standby (RUNSTDBY) bit can be enabled.

This register has Configuration Change Protection (CCP), so the `ccp_write_io` function in `cpufunc.h` should be used to ensure correct timing for the unlock of the register.

Figure 4-1. CLKCTRL.XOSCHFCTRLA – Enable XOSCHF

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY		CSUTHF[1:0]		FRQRANGE[1:0]		SELHF	ENABLE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – RUNSTDBY Run Standby
This bit controls whether the External High-Frequency Oscillator (XOSCHF) is always running or not, when the ENABLE bit is '1'.

Value	Description
0	The XOSCHF oscillator will only run when requested by a peripheral or by the main clock (1)
1	The XOSCHF oscillator will always run in Active, Idle and Standby sleep modes (2)

Notes:

1. The requesting peripheral, or the main clock, must take the oscillator start-up time into account.
2. The oscillator signal is only available if requested, and will be available after two XOSCHF cycles, if the initial crystal start-up time has already ended.

Bits 5:4 – CSUTHF[1:0] Crystal Start-up Time
This bit field controls the start-up time for the External High-Frequency Oscillator (XOSCHF), when the Source Select (SELHF) bit is '0'.

Value	Name	Description
0x0	256	256 XOSCHF cycles
0x1	1K	1K XOSCHF cycles
0x2	4K	4K XOSCHF cycles
0x3	-	Reserved

Note: This bit field is read-only when the ENABLE bit or the External Crystal/Clock Status (XOSCHFS) bit in the Main Clock Status (MCLKSTATUS) register is '1'.

Bits 3:2 – FRQRANGE[1:0] Frequency Range
This bit field controls the maximum frequency supported for the external crystal. The larger the range selected, the higher the current consumption by the oscillator.

Value	Name	Description
0x0	8M	Max. 8 MHz XTAL frequency
0x1	16M	Max. 16 MHz XTAL frequency
0x2	24M	Max. 24 MHz XTAL frequency
0x3	32M	Max. 32 MHz XTAL frequency

Note: If a crystal with a frequency larger than the maximum supported CLK_CPU frequency is used and used as the main clock, it is necessary to divide it down by writing the appropriate configuration to the PDIV bit field in the Main Clock Control B register.

Bit 1 – SELHF Source Select
This bit controls the source of the External High-Frequency Oscillator (XOSCHF).

Value	Name	Description
0	CRYSTAL	External Crystal on the XTALHF1 and XTALHF2 pins
1	EXTCLOCK	External Clock on the XTALHF1 pin

Note: This bit field is read-only when the ENABLE bit or the External Crystal/Clock Status (XOSCHFS) bit in the Main Clock Status (MCLKSTATUS) register is '1'.

Bit 0 – ENABLE Enable
This bit controls whether the External High-Frequency Oscillator (XOSCHF) is enabled or not.

Value	Description
0	The XOSCHF oscillator is disabled
1	The XOSCHF oscillator is enabled, and overrides normal port operation for the respective oscillator pins

```
/* Enable crystal oscillator with frequency range 16 MHz and 4K cycles start-up time */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
             | CLKCTRL_CSUTHF_4K_gc
             | CLKCTRL_FRQRANGE_16M_gc
             | CLKCTRL_SELHF_CRYSTAL_gc
             | CLKCTRL_ENABLE_bm);
```

After enabling the XOSCHF, wait for the clock source to stabilize by polling the External Clock Status (EXTS) bit in the Main Clock Status (CLKCTRL.MCLKSTATUS) register until the bit is read as '1'.

Figure 4-2. CLKCTRL.MCLKSTATUS – Wait for XOSCHF to start

Bit	7	6	5	4	3	2	1	0
			PLLS	EXTS	XOSC32KS	OSC32KS	OSCHFS	SOSC
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 4 – EXTS External Crystal/Clock Status

Value	Description
0	The external high-frequency crystal is not stable, when the Source Select (SELHF) bit in the External High-Frequency Oscillator Control A (CLKCTRL.XOSCHFCTRLA) register is '0'. The external high-frequency clock is not running, when the SELHF bit is '1'.
1	The external high-frequency crystal is stable, when the SELHF bit is '0'. The external high-frequency clock is running, when the SELHF bit is '1'.

```
/* Confirm crystal oscillator start-up */
while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
{
    ;
}
```

The Main Clock prescaler shall be configured to give a maximum frequency of 24 MHz. If Main Clock will use XOSCHF with a crystal running faster than 24 MHz as the clock source, a prescaler setting can be written to the Prescaler Division (PDIV) bit field and '1' to the Prescaler Enable (PEN) bit in the Main Clock Control B (CLKCTRL.MCLKCTRLB) register. The AVR128DB48 Curiosity Nano has a 16 MHz crystal which allows disabling the prescaler by writing '0' to the PEN bit.

Main Clock Control B also has CCP.

Figure 4-3. CLKCTRL.MCLKCTRLB – Configure Main Clock prescaler

Bit	7	6	5	4	3	2	1	0
				PDIV[3:0]				PEN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:1 – PDIV[3:0] Prescaler Division
This bit field controls the division ratio of the Main Clock (CLK_MAIN) prescaler, when the Prescaler (PEN) bit is '1'.

Value	Name	Description
0x0	2X	Divide by 2
0x1	4X	Divide by 4
0x2	8X	Divide by 8
0x3	16X	Divide by 16
0x4	32X	Divide by 32
0x5	64X	Divide by 64
0x8	6X	Divide by 6
0x9	10X	Divide by 10
0xA	12X	Divide by 12
0xB	24X	Divide by 24
0xC	48X	Divide by 48
Other	-	Reserved

Note: Configuration of the input frequency (CLK_MAIN) and prescaler settings must not exceed the allowed maximum frequency of the peripheral clock (CLK_PER) or CPU clock (CLK_CPU). Refer to the *Electrical Characteristics* section for further information.

Bit 0 – PEN Prescaler Enable
This bit controls whether the Main Clock (CLK_MAIN) prescaler is enabled or not.

Value	Description
0	The CLK_MAIN prescaler is disabled
1	The CLK_MAIN prescaler is enabled, and the division ratio is controlled by the Prescaler Division (PDIV) bit field

```
/* Clear Main Clock Prescaler */
ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLB, 0x00);
```

Change Main Clock source by writing the EXTCLK setting to the Clock Select (CLKSEL) bit field in the Main Clock Control A (CLKCTRL.MCLKCTRLA) register. The Main Clock Out (CLKOUT) bit can be written to '1' to output the Main Clock on the CLKOUT pin. This register also has CCP.

Figure 4-4. CLKCTRL.MCLKCTRLA – Change source to XOSCHF

Bit	7	6	5	4	3	2	1	0
	CLKOUT				CLKSEL[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – CLKOUT Main Clock Out
This bit controls whether the main clock is available on the Main Clock Out (CLKOUT) pin or not, when the main clock is running.
This bit is cleared when a '0' is written to it or when a Clock Failure Detection (CFD) condition with the main clock as source occurs.
This bit is set when a '1' is written to it.

Value	Description
0	The main clock is not available on the CLKOUT pin
1	The main clock is available on the CLKOUT pin

Bits 3:0 – CLKSEL[3:0] Clock Select
This bit field controls the source for the Main Clock (CLK_MAIN).

Value	Name	Description
0x0	OSCHF	Internal high-frequency oscillator
0x1	OSC32K	32.768 kHz internal oscillator
0x2	XOSC32K	32.768 kHz external crystal oscillator
0x3	EXTCLK	External clock or external crystal, depending on the SELHF bit in XOSCHFCTRLA
Other	Reserved	Reserved

```
/* Set the main clock to use XOSCHF as source, and enable the CLKOUT pin */
ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLA,
             CLKCTRL_CLKSEL_EXTCLK_gc | CLKCTRL_CLKOUT_bm);
```

After changing the Main Clock source, wait for the switch to complete by polling the Main Clock Oscillator Changing (SOSC) bit in the Main Clock Status (CLKCTRL.MCLKSTATUS) register until the bit is read as '0'.

Figure 4-5. CLKCTRL.MCLKSTATUS – Wait for Main Clock to change

Bit	7	6	5	4	3	2	1	0
			PLLS	EXTS	XOSC32KS	OSC32KS	OSCHFS	SOSC
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 0 – SOSC Main Clock Oscillator Changing

Value	Description
0	The clock source for CLK_MAIN is not undergoing a switch
1	The clock source for CLK_MAIN is undergoing a switch and will change as soon as the new source is stable

```
/* Wait for system oscillator changing to complete */
while(CLKCTRL.MCLKSTATUS & CLKCTRL_SOSC_bm)
{
    ;
}
```

The Run Standby bit can now be cleared since the output is now is used by Main Clock and there is no need to force enable the oscillator.

```
    /* Clear RUNSTDBY for power save during sleep */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA,
                 CLKCTRL.XOSCHFCTRLA & ~CLKCTRL_RUNSTDBY_bm);
```

The code for this example is available in the **XOSCHF-with-external-crystal** folder in these github repositories:

5. XOSCHF with External Clock

To use XOSCHF with an external clock signal, the SELHF bit and the ENABLE bit in the External High-Frequency Oscillator Control A (CLKCTRL.XOSCHFCTRLA) register must be written to '1'.

This register has Configuration Change Protection (CCP), so the `ccp_write_io` function in `cpufunc.h` should be used to ensure correct timing for the unlock of the register.

Figure 5-1. CLKCTRL.XOSCHFCTRLA – Enable XOSCHF

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY		CSUTHF[1:0]		FRQRANGE[1:0]		SELHF	ENABLE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 1 – SELHF Source Select
This bit controls the source of the External High-Frequency Oscillator (XOSCHF).

Value	Name	Description
0	CRYSTAL	External Crystal on the XTALHF1 and XTALHF2 pins
1	EXTCLOCK	External Clock on the XTALHF1 pin

Note: This bit field is read-only when the ENABLE bit or the External Crystal/Clock Status (XOSCHFS) bit in the Main Clock Status (MCLKSTATUS) register is '1'.

Bit 0 – ENABLE Enable
This bit controls whether the External High-Frequency Oscillator (XOSCHF) is enabled or not.

Value	Description
0	The XOSCHF oscillator is disabled
1	The XOSCHF oscillator is enabled, and overrides normal port operation for the respective oscillator pins

```
/* Enable external clock input */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA,
             CLKCTRL_SELHF_EXTCLOCK_gc | CLKCTRL_ENABLE_bm);
```

If changing Main Clock to use XOSCHF as the clock source, first make sure to set the Main Clock prescaler to output maximum 24 MHz by writing a prescaler setting to the Prescaler Division (PDIV) bit field and '1' to the Prescaler Enable (PEN) bit in the Main Clock Control B (CLKCTRL.MCLKCTRLB) register. This register also has CCP.

Figure 5-3. CLKCTRL.MCLKCTRLB – Configure Main Clock prescaler

Bit	7	6	5	4	3	2	1	0
				PDIV[3:0]				PEN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:1 – PDIV[3:0] Prescaler Division
This bit field controls the division ratio of the Main Clock (CLK_MAIN) prescaler, when the Prescaler (PEN) bit is '1'.

Value	Name	Description
0x0	2X	Divide by 2
0x1	4X	Divide by 4
0x2	8X	Divide by 8
0x3	16X	Divide by 16
0x4	32X	Divide by 32
0x5	64X	Divide by 64
0x8	6X	Divide by 6
0x9	10X	Divide by 10
0xA	12X	Divide by 12
0xB	24X	Divide by 24
0xC	48X	Divide by 48
Other	-	Reserved

Note: Configuration of the input frequency (CLK_MAIN) and prescaler settings must not exceed the allowed maximum frequency of the peripheral clock (CLK_PER) or CPU clock (CLK_CPU). Refer to the *Electrical Characteristics* section for further information.

Bit 0 – PEN Prescaler Enable
This bit controls whether the Main Clock (CLK_MAIN) prescaler is enabled or not.

Value	Description
0	The CLK_MAIN prescaler is disabled
1	The CLK_MAIN prescaler is enabled, and the division ratio is controlled by the Prescaler Division (PDIV) bit field

```
/* Set Main Clock Prescaler */
ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLB,
             CLKCTRL_PDIV_2X_gc | CLKCTRL_PEN_bm);
```

Change Main Clock source by writing the EXTCLK setting to the Clock Select (CLKSEL) bit field in the Main Clock Control A (CLKCTRL.MCLKCTRLA) register. The Main Clock Out (CLKOUT) bit can be written to '1' to output the Main Clock on the CLKOUT pin. This register also has CCP.

Figure 5-4. CLKCTRL.MCLKCTRLA – Change source to XOSCHF

Bit	7	6	5	4	3	2	1	0
	CLKOUT				CLKSEL[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – CLKOUT Main Clock Out
This bit controls whether the main clock is available on the Main Clock Out (CLKOUT) pin or not, when the main clock is running.
This bit is cleared when a '0' is written to it or when a Clock Failure Detection (CFD) condition with the main clock as source occurs.
This bit is set when a '1' is written to it.

Value	Description
0	The main clock is not available on the CLKOUT pin
1	The main clock is available on the CLKOUT pin

Bits 3:0 – CLKSEL[3:0] Clock Select
This bit field controls the source for the Main Clock (CLK_MAIN).

Value	Name	Description
0x0	OSCHF	Internal high-frequency oscillator
0x1	OSC32K	32.768 kHz internal oscillator
0x2	XOSC32K	32.768 kHz external crystal oscillator
0x3	EXTCLK	External clock or external crystal, depending on the SELHF bit in XOSCHFCTRLA
Other	Reserved	Reserved

```
/* Set the main clock to use XOSCHF as source, and enable the CLKOUT pin */
ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLA,
             CLKCTRL_CLKSEL_EXTCLK_gc | CLKCTRL_CLKOUT_bm);
```

After changing the Main Clock source, wait for the switch to complete by polling the Main Clock Oscillator Changing (SOSC) bit in the Main Clock Status (CLKCTRL.MCLKSTATUS) register until the bit is read as '0'.

Figure 5-5. CLKCTRL.MCLKSTATUS – Wait for Main Clock to change

Bit	7	6	5	4	3	2	1	0
			PLLS	EXTS	XOSC32KS	OSC32KS	OSCHFS	SOSC
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 0 – SOSC Main Clock Oscillator Changing

Value	Description
0	The clock source for CLK_MAIN is not undergoing a switch
1	The clock source for CLK_MAIN is undergoing a switch and will change as soon as the new source is stable

```
/* Wait for system oscillator changing to complete */
while(CLKCTRL.MCLKSTATUS & CLKCTRL_SOSC_bm)
{
    ;
}
```

The code for this example is available in the **XOSCHF-with-external-clock** folder in these github repositories:

6. RTC with XOSCHF

To use XOSCHF as clock source for the Real-Time Counter (RTC), first enable the XOSCHF similarly to the first two use cases. The crystal or input clock frequency can be up to ¼ of the main clock frequency.

⚠WARNING The 16 MHz crystal on the ATtiny1627 Curiosity Nano will generate a too high frequency for this example. Replace the crystal or use an external clock with maximum ¼ of the main clock frequency to run within spec.

```
/* Enable crystal oscillator with frequency range 8 MHz and 1K cycles start-up time */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
              | CLKCTRL_CSUTHF_1K_gc
              | CLKCTRL_FRQRANGE_8M_gc
              | CLKCTRL_SELHF_CRYSTAL_gc
              | CLKCTRL_ENABLE_bm);

/* Confirm crystal oscillator start-up */
while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
{
    ;
}

/* Clear RUNSTDBY for power save during sleep */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA,
             CLKCTRL.XOSCHFCTRLA & ~CLKCTRL_RUNSTDBY_bm);
```

To select the XOSCHF as clock source for RTC, the EXTCLK setting must be written to the Clock Select (RTC.CLKSEL) register.

Figure 6-1. RTC.CLKSEL – Select XOSCHF as source

Bit	7	6	5	4	3	2	1	0
							CLKSEL[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – CLKSEL[1:0] Clock Select
Writing these bits select the source for the RTC clock (CLK_RTC).
When configuring the RTC to use either XOSC32K or the external clock on XTAL32K1, XOSC32K needs to be enabled, and the Source Select (SEL) bit and Run Standby (RUNSTDBY) bit in the XOSC32K Control A of the Clock Controller (CLKCTRL.XOSC32KCTRLA) register must be configured accordingly.

Value	Name	Description
0x0	OSC32K	32.768 kHz from OSC32K
0x1	OSC1K	1.024 kHz from OSC32K
0x2	XTAL32K	32.768 kHz from XOSC32K or external clock from XTAL32K1
0x3	EXTCLK	External clock from the EXTCLK pin

```
/* Configure RTC to use XOSCHF as source */
RTC.CLKSEL = RTC_CLKSEL_EXTCLK_gc;
```

Now the RTC can be configured and enabled with XOSCHF as clock source.

The code for this example is available in the **RTC-with-XOSCHF** folder in these github repositories:

View Code Example on GitHub
Click to browse repository

7. TCD with XOSCHF

To use XOSCHF as clock source for TCD0, first enable the XOSCHF similarly to the first two use cases. The crystal or input clock frequency can be up to 32 MHz.

```
/* Enable crystal oscillator with frequency range 16 MHz and 4K cycles start-up time */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
             | CLKCTRL_CSUTHF_4K_gc
             | CLKCTRL_FRQRANGE_16M_gc
             | CLKCTRL_SELHF_CRYSTAL_gc
             | CLKCTRL_ENABLE_bm);

/* Confirm crystal oscillator start-up */
while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
{
    ;
}

/* Clear RUNSTDBY for power save during sleep */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA,
             CLKCTRL.XOSCHFCTRLA & ~CLKCTRL_RUNSTDBY_bm);
```

To select the XOSCHF as clock source for TCD0, the EXTCLK setting must be written to the Clock Select (CLKSEL) bit field in the Control A (TCD0.CTRLA) register.

Figure 7-1. TCD0.CTRLA – Enable TCD0 with PLL as source

Bit	7	6	5	4	3	2	1	0
		CLKSEL[1:0]		CNTPRES[1:0]		SYNCPRES[1:0]		ENABLE
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:5 – CLKSEL[1:0] Clock Select
The Clock Select bits select the clock source of the TCD clock.

Value	Name	Description
0x0	OSCHF	Internal High-Frequency Oscillator
0x1	PLL	PLL
0x2	EXTCLK	External clock
0x3	CLK_PER	Peripheral clock

Bits 4:3 – CNTPRES[1:0] Counter Prescaler
The Counter Prescaler bits select the division factor of the TCD counter clock.

Value	Name	Description
0x0	DIV1	Division factor 1
0x1	DIV4	Division factor 4
0x2	DIV32	Division factor 32
0x3	-	Reserved

Bits 2:1 – SYNCPRES[1:0] Synchronization Prescaler
The Synchronization Prescaler bits select the division factor of the TCD clock.

Value	Name	Description
0x0	DIV1	Division factor 1
0x1	DIV2	Division factor 2
0x2	DIV4	Division factor 4
0x3	DIV8	Division factor 8

```
/* Configure the TCD with XOSCHF (16 MHz) as source */
TCD0.CTRLA = TCD_CLKSEL_EXTCLK_gc | TCD_CNTPRES_DIV1_gc | TCD_SYNCPRES_DIV1_gc;

/* Replace with your application configuration */

/* Enable TCD0 */
TCD0.CTRLA |= TCD_ENABLE_bm;
```

The code for this example is available in the **TCD-with-XOSCHF** folder in these github repositories:

8. TCD with XOSCHF and PLL

To use XOSCHF as clock source for the Phase-Lock Loop (PLL), first enable the XOSCHF similarly to first two use cases. The crystal or input clock frequency must be at least 16 MHz and can be multiplied two or three times, giving an output frequency up to 48 MHz.

```
/* Enable crystal oscillator with frequency range 16 MHz and 4K cycles start-up time */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
              | CLKCTRL_CSUTHF_4K_gc
              | CLKCTRL_FRQRANGE_16M_gc
              | CLKCTRL_SELHF_CRYSTAL_gc
              | CLKCTRL_ENABLE_bm);

/* Confirm crystal oscillator start-up */
while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
{
    ;
}

/* Clear RUNSTDBY for power save during sleep */
ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA,
             CLKCTRL.XOSCHFCTRLA & ~CLKCTRL_RUNSTDBY_bm);
```

Select XOSCHF as source by writing a '1' to the SOURCE bit in the PLL Control A (CLKCTRL.PLLCTRLA) register, and select the multiplication factor by writing to the MULFAC bit field in the same register.

This register has Configuration Change Protection (CCP), so the `ccp_write_io` function in `cpufunc.h` should be used to ensure correct timing for the unlock of the register.

Figure 8-1. CLKCTRL.PLLCTRLA – Enable PLL with XOSCHF as source

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY	SOURCE					MULFAC[1:0]	
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0

Bit 6 – SOURCE Select Source for PLL
This bit controls the Phase-Locked Loop (PLL) clock source.

Value	Name	Description
0	OSCHF	High-frequency internal oscillator as PLL source
1	XOSCHF	High-frequency external clock or external high-frequency oscillator as PLL source

Bits 1:0 – MULFAC[1:0] Multiplication Factor
This bit field controls the multiplication factor for the Phased-Locked Loop (PLL).

Value	Name	Description
0x0	DISABLE	PLL is disabled
0x1	2x	2 x multiplication factor
0x2	3x	3 x multiplication factor
0x3	-	Reserved

```
/* Set the PLL to use XOSCHF as source, and select 3x multiplication factor */
ccp_write_io((uint8_t *) &CLKCTRL.PLLCTRLA,
             CLKCTRL_SOURCE_bm | CLKCTRL_MULFAC_3x_gc);
```

To select the PLL as clock source for TCD0, the PLL setting must be written to the Clock Select (CLKSEL) bit field in the Control A (TCD0.CTRLA) register.

Figure 8-3. TCD0.CTRLA – Enable TCD0 with PLL as source

Bit	7	6	5	4	3	2	1	0
		CLKSEL[1:0]		CNTPRES[1:0]		SYNCPRES[1:0]		ENABLE
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:5 – CLKSEL[1:0] Clock Select
The Clock Select bits select the clock source of the TCD clock.

Value	Name	Description
0x0	OSCHF	Internal High-Frequency Oscillator
0x1	PLL	PLL
0x2	EXTCLK	External clock
0x3	CLK_PER	Peripheral clock

Bits 4:3 – CNTPRES[1:0] Counter Prescaler
The Counter Prescaler bits select the division factor of the TCD counter clock.

Value	Name	Description
0x0	DIV1	Division factor 1
0x1	DIV4	Division factor 4
0x2	DIV32	Division factor 32
0x3	-	Reserved

Bits 2:1 – SYNCPRES[1:0] Synchronization Prescaler
The Synchronization Prescaler bits select the division factor of the TCD clock.

Value	Name	Description
0x0	DIV1	Division factor 1
0x1	DIV2	Division factor 2
0x2	DIV4	Division factor 4
0x3	DIV8	Division factor 8

```
/* Configure the TCD with PLL (48 MHz) as source */
TCD0.CTRLA = TCD_CLKSEL_PLL_gc | TCD_CNTPRES_DIV1_gc | TCD_SYNCPRES_DIV1_gc;

/* Replace with your application configuration */

/* Enable TCD0 */
TCD0.CTRLA |= TCD_ENABLE_bm;
```

The code for this example is available in the **TCD-with-XOSCHF-and-PLL** folder in these github repositories:

View Code Example on GitHub
Click to browse repository

9. CFD on XOSCHF

To use Clock Failure Detection (CFD) on the External High-Frequency Oscillator (XOSCHF), write the XOSCHF setting to the Clock Failure Detection Source (CFDSRC) bit field and '1' to the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register.

This register has Configuration Change Protection (CCP), so the `ccp_write_io` function in `cpufunc.h` should be used to ensure correct timing for the unlock of the register.

Figure 9-1. CLKCTRL.MCLKCTRLC – Enable CFD on XOSCHF

Bit	7	6	5	4	3	2	1	0
					CFDSRC[1:0]		CFDTST	CFDEN
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:2 – CFDSRC[1:0] Clock Failure Detection Source
This bit field controls which clock source to monitor, when the Clock Failure Detection Enable (CFDEN) bit is '1'.

Value	Name	Description
0x0	CLKMAIN	Main Clock
0x1	XOSCHF	External High Frequency Oscillator
0x2	XOSC32K	External 32.768 kHz Oscillator
Other	Reserved	Reserved

Note: This bit field is read-only when the CFDEN bit is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and Interrupt Type (INTTYPE) bit in the Main Clock Interrupt Control (CLKCTRL.MCLKINTCTRL) are '1'. This bit will remain read-only until a System Reset occurs.

Bit 0 – CFDEN Clock Failure Detection Enable
This bit controls whether Clock Failure Detection (CFD) is enabled or not.

Value	Description
0	CFD is disabled
1	CFD is enabled

Note: This bit is read-only when this bit is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and Interrupt Type (INTTYPE) bit in the Main Clock Interrupt Control (CLKCTRL.MCLKINTCTRL) are '1'. This bit will remain read-only until a System Reset occurs.

```
/* Enable Clock Failure Detection on XOSCHF */
ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLC,
             CLKCTRL_CFDSRC_XOSCHF_gc | CLKCTRL_CFDEN_bm);
```

To enable the regular CFD interrupt, write '0' to the Interrupt Type (INTTYPE) bit and '1' to the Clock Failure Detection (CFD) bit in the Main Clock Interrupt Control (CLKCTRL.MCLKINTCTRL) register. This register also has CCP.

Figure 9-2. CLKCTRL.MCLKINTCTRL – Enable regular CFD interrupt

Bit	7	6	5	4	3	2	1	0
	INTTYPE							CFD
Access	R/W							R/W
Reset	0							0

Bit 7 – INTTYPE Interrupt Type
This bit controls the type of the Clock Failure Detection (CFD) interrupt.

Value	Name	Description
0	INT	Regular Interrupt
1	NMI	Non-Maskable Interrupt

Note: This bit is read-only when the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and this bit are '1.' This bit will remain read-only until a System Reset occurs.

Bit 0 – CFD Clock Failure Detection Interrupt Enable
This bit controls whether the Clock Failure Detection (CFD) interrupt is enabled or not.

Value	Description
0	The CFD interrupt is disabled
1	The CFD interrupt is enabled

Note: This bit is read-only when the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register is '1', and both the Interrupt Type (INTTYPE) bit and this bit are '1.' This bit will remain read-only until a System Reset occurs.

```
    /* Enable regular interrupt for CFD */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKINTCTRL, CLKCTRL_CFD_bm);
```

The CFD vector will be called when the interrupt is triggered. Before returning from the Interrupt Service Routine (ISR), the Clock Failure Detection (CFD) interrupt flag in the Main Clock Interrupt Flags (CLKCTRL.MCLKINTFLAGS) register must be cleared. This is done by writing a '1' to the flag.

Figure 9-3. CLKCTRL.MCLKINTFLAGS – Clear CFD interrupt flag

Bit	7	6	5	4	3	2	1	0
								CFD
Access								R/W
Reset								0

Bit 0 – CFD Clock Failure Detection Interrupt Flag
This flag is cleared by writing a '1' to it.
This flag is set when a clock failure is detected.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Clock Failure Detection (CFD) interrupt flag.

```
ISR(CLKCTRL_CFD_vect)
{
    /* This interrupt will trigger every time the CFD detects XOSCHF has stopped
     * The Main Clock source is OSCHF so the CPU is not affected
     */
    LED0_toggle();

    /* Clear the CFD interrupt flag */
    CLKCTRL.MCLKINTFLAGS = CLKCTRL_CFD_bm;
}
```

The code for this example is available in the **CFD-on-XOSCHF** folder in these github repositories:

10. CFD on Main Clock with NMI

To use Clock Failure Detection (CFD) on the Main Clock, write the CLKMAIN setting to the Clock Failure Detection Source (CFDSRC) bit field and '1' to the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register.

This register has Configuration Change Protection (CCP), so the `ccp_write_io` function in `cpufunc.h` should be used to ensure correct timing for the unlock of the register.

Figure 10-1. CLKCTRL.MCLKCTRLC – Enable CFD on Main Clock

Bit	7	6	5	4	3	2	1	0
					CFDSRC[1:0]		CFDTST	CFDEN
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:2 – CFDSRC[1:0] Clock Failure Detection Source
This bit field controls which clock source to monitor, when the Clock Failure Detection Enable (CFDEN) bit is '1'.

Value	Name	Description
0x0	CLKMAIN	Main Clock
0x1	XOSCHF	External High Frequency Oscillator
0x2	XOSC32K	External 32.768 kHz Oscillator
Other	Reserved	Reserved

Note: This bit field is read-only when the CFDEN bit is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and Interrupt Type (INTTYPE) bit in the Main Clock Interrupt Control (CLKCTRL.MCLKINTCTRL) are '1'. This bit will remain read-only until a System Reset occurs.

Bit 0 – CFDEN Clock Failure Detection Enable
This bit controls whether Clock Failure Detection (CFD) is enabled or not.

Value	Description
0	CFD is disabled
1	CFD is enabled

Note: This bit is read-only when this bit is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and Interrupt Type (INTTYPE) bit in the Main Clock Interrupt Control (CLKCTRL.MCLKINTCTRL) are '1'. This bit will remain read-only until a System Reset occurs.

```
/* Enable Clock Failure Detection on main clock */
ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLC,
             CLKCTRL_CFDSRC_CLKMAIN_gc | CLKCTRL_CFDEN_bm);
```

To enable the CFD interrupt as a Non-Maskable Interrupt (NMI), write '1' to both the Interrupt Type (INTTYPE) bit and the Clock Failure Detection (CFD) bit in the Main Clock Interrupt Control (CLKCTRL.MCLKINTCTRL) register. This register also has CCP.

Figure 10-2. CLKCTRL.MCLKINTCTRL – Enable CFD interrupt as NMI

Bit	7	6	5	4	3	2	1	0
	INTTYPE							CFD
Access	R/W							R/W
Reset	0							0

Bit 7 – INTTYPE Interrupt Type
This bit controls the type of the Clock Failure Detection (CFD) interrupt.

Value	Name	Description
0	INT	Regular Interrupt
1	NMI	Non-Maskable Interrupt

Note: This bit is read-only when the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and this bit are '1.' This bit will remain read-only until a System Reset occurs.

Bit 0 – CFD Clock Failure Detection Interrupt Enable
This bit controls whether the Clock Failure Detection (CFD) interrupt is enabled or not.

Value	Description
0	The CFD interrupt is disabled
1	The CFD interrupt is enabled

Note: This bit is read-only when the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register is '1', and both the Interrupt Type (INTTYPE) bit and this bit are '1.' This bit will remain read-only until a System Reset occurs.

```
    /* Enable Non-Maskable Interrupt for CFD */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKINTCTRL,
                 CLKCTRL_INTTYPE_bm | CLKCTRL_CFD_bm);
```

When the CFD interrupt has been configured as an NMI, the NMI interrupt vector will be called instead of the CFD vector when the interrupt is triggered.

When entering the Interrupt Service Routine (ISR) for the NMI, the interrupt source must be found if more than one NMI source is enabled. The CFD interrupt flag in the Main Clock Interrupt Flags (CLKCTRL.MCLKINTFLAGS) register is '1' if the CFD was the trigger.

Figure 10-3. CLKCTRL.MCLKINTFLAGS – Check CFD interrupt flag

Bit	7	6	5	4	3	2	1	0
								CFD
Access								R/W
Reset								0

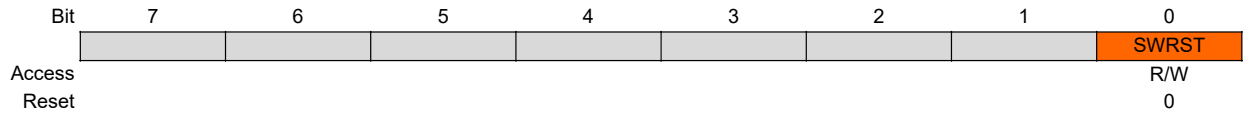
Bit 0 – CFD Clock Failure Detection Interrupt Flag
This flag is cleared by writing a '1' to it.
This flag is set when a clock failure is detected.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Clock Failure Detection (CFD) interrupt flag.

```
ISR(NMI_vect)
{
    /* Check which NMI has triggered*/
    if(CLKCTRL.MCLKINTFLAGS & CLKCTRL_CFD_bm)
    {
        /* This interrupt will trigger if the source for the main clock fails
        * and the CFD is able to switch to a different working clock.
```

```
        * In this case that means XOSCHF has failed and is replaced by OSCHF.
        * The main clock is therefore reduced to 4 MHz / 2 = 2 MHz.
        */

        /* Toggle the LED forever */
        while(1)
        {
            LED0_toggle();
            _delay_ms(200); // 200 ms calculated from 16 MHz == 1600 ms
        }

    }
    else
    {
        /* A different NMI has been triggered */
    }

    /* Non-Maskable Interrupt bits can only be cleared by a reset */
}
```

A software reset can be triggered by writing a '1' to the Software Reset (SWRST) bit in the Software Reset Register (RSTCTRL.SWRR). This register also has CCP.

Figure 10-4. RSTCTRL.SWRR – Trigger Software Reset



Bit 0 – SWRST Software Reset
When this bit is written to '1', a Software Reset will occur.
This bit will always read as '0'.

```
    /* Software Reset */
    ccp_write_io((uint8_t *) &RSTCTRL.SWRR, RSTCTRL_SWRST_bm);
```

The code for this example is available in the **CFD-on-main-clock-with-NMI** folder in these github repositories:

View Code Example on GitHub
Click to browse repository

11. Revision History

Revision	Date	Description
A	9/2020	Initial document release

12. Appendix

Here are the code examples for each case used in the technical brief.

Example 12-1. XOSCHF with External Crystal

```
#define F_CPU 16000000ul

#include <avr/io.h>
#include <avr/cpufunc.h>

void CLOCK_XOSCHF_crystal_init(void);

static inline void LED0_init(void)
{
    PORTB.DIRSET = PIN3_bm;
}

int main(void)
{
    CLOCK_XOSCHF_crystal_init();

    /* Turn on LED0 to show successful clock init */
    LED0_init();

    /* Replace with your application code */
    while(1)
    {
    }
}


void CLOCK_XOSCHF_crystal_init(void)
{
    /* Enable crystal oscillator with frequency range 16 MHz and 4K cycles
start-up time */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
                 | CLKCTRL_CSUTHF_4K_gc
                 | CLKCTRL_FRQRANGE_16M_gc
                 | CLKCTRL_SELHF_CRYSTAL_gc
                 | CLKCTRL_ENABLE_bm);

    /* Confirm crystal oscillator start-up */
    while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
    {
        ;
    }

    /* Clear Main Clock Prescaler */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLB, 0x00);

    /* Set the main clock to use XOSCHF as source, and enable the CLKOUT pin */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLA, CLKCTRL_CLKSEL_EXTCLK_gc |
CLKCTRL_CLKOUT_bm);

    /* Wait for system oscillator changing to complete */
    while(CLKCTRL.MCLKSTATUS & CLKCTRL_SOSC_bm)
    {
        ;
    }

    /* Clear RUNSTDBY for power save during sleep */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL.XOSCHFCTRLA &
~CLKCTRL_RUNSTDBY_bm);

    /* Change complete and the main clock is 16 MHz */
}
```

Example 12-2. XOSCHF with External Clock

```
#define F_CPU 16000000ul

#include <avr/io.h>
#include <avr/cpufunc.h>

void CLOCK_XOSCHF_clock_init(void);

static inline void LED0_init(void)
{
    PORTB.DIRSET = PIN3_bm;
}

int main(void)
{
    CLOCK_XOSCHF_clock_init();

    /* Turn on LED0 to show successful clock init */
    LED0_init();

    /* Replace with your application code */
    while(1)
    {
    }
}


void CLOCK_XOSCHF_clock_init(void)
{
    /* Enable external (32 MHz) clock input */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_SELHF_EXTCLOCK_gc |
CLKCTRL_ENABLE_bm);

    /* Set Main Clock Prescaler */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLB, CLKCTRL_PDIV_2X_gc |
CLKCTRL_PEN_bm);

    /* Set the main clock to use XOSCHF as source, and enable the CLKOUT pin */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLA, CLKCTRL_CLKSEL_EXTCLK_gc |
CLKCTRL_CLKOUT_bm);

    /* Wait for system oscillator changing to complete */
    while(CLKCTRL.MCLKSTATUS & CLKCTRL_SOSC_bm)
    {
        ;
    }

    /* Change complete and the main clock is 32 MHz / 2 = 16 MHz */
}
```

Example 12-3. RTC with XOSCHF

```
#include <avr/io.h>
#include <avr/cpufunc.h>
#include <avr/interrupt.h>

void CLOCK_XOSCHF_crystal_init(void);
void TIMER_RTC_init(void);

static inline void LED0_init(void)
{
    PORTB.DIRSET = PIN3_bm;
    PORTB.OUTSET = PIN3_bm;
}

static inline void LED0_toggle(void)
{
    PORTB.OUTTGL = PIN3_bm;
}

int main(void)
```

```
{
    CLOCK_XOSCHF_crystal_init();
    TIMER_RTC_init();
    LED0_init();

    /* Enable global interrupts */
    sei();

    /* Replace with your application code */
    while(1)
    {
    }
}


void CLOCK_XOSCHF_crystal_init(void)
{
    /* Enable crystal oscillator with frequency range 8 MHz and 1K cycles
start-up time */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
                | CLKCTRL_CSUTHF_1K_gc
                | CLKCTRL_FRQRANGE_8M_gc
                | CLKCTRL_SELHF_CRYSTAL_gc
                | CLKCTRL_ENABLE_bm);

    /* Confirm crystal oscillator start-up */
    while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
    {
        ;
    }

    /* Clear RUNSTDBY for power save during sleep */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL.XOSCHFCTRLA &
~CLKCTRL_RUNSTDBY_bm);
}


void TIMER_RTC_init(void)
{
    while(RTC.STATUS > 0)
    {
        /* Wait for RTC registers to synchronize */
    }

    /* Configure RTC to use XOSCHF as source */
    RTC.CLKSEL = RTC_CLKSEL_EXTCLK_gc;

    /* Replace with your application configuration */
    RTC.PER = 0xffff;
    RTC.INTCTRL = RTC_OVF_bm;
    RTC.CTRLA = RTC_PRESCALER_DIV32_gc | RTC_RTCEN_bm;
}


ISR(RTC_CNT_vect)
{
    /* This interrupt will trigger every time the RTC overflows */
    LED0_toggle();

    /* Clear the RTC overflow interrupt flag */
    RTC.INTFLAGS = RTC_OVF_bm;
}
```

Example 12-4. TCD with XOSCHF

```
#include <avr/io.h>
#include <avr/cpufunc.h>

void CLOCK_XOSCHF_crystal_init(void);
void TIMER_TCD0_init(void);

int main(void)
{
```

```
    CLOCK_XOSCHF_crystal_init();
    TIMER_TCD0_init();

    /* Replace with your application code */
    while(1)
    {
    }
}


void CLOCK_XOSCHF_crystal_init(void)
{
    /* Enable crystal oscillator with frequency range 16 MHz and 4K cycles
start-up time */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
                | CLKCTRL_CSUTHF_4K_gc
                | CLKCTRL_FRQRANGE_16M_gc
                | CLKCTRL_SELHF_CRYSTAL_gc
                | CLKCTRL_ENABLE_bm);

    /* Confirm crystal oscillator start-up */
    while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
    {
        ;
    }

    /* Clear RUNSTDBY for power save during sleep */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL.XOSCHFCTRLA &
~CLKCTRL_RUNSTDBY_bm);
}


void TIMER_TCD0_init(void)
{
    /* Configure the TCD with XOSCHF (16 MHz) as source */
    TCD0.CTRLA = TCD_CLKSEL_EXTCLK_gc | TCD_CNTPRES_DIV1_gc |
TCD_SYNCPRES_DIV1_gc;

    /* Replace with your application configuration */

    /* Enable TCD0 */
    TCD0.CTRLA |= TCD_ENABLE_bm;
}
```

Example 12-5. TCD with XOSCHF and PLL

```
#include <avr/io.h>
#include <avr/cpufunc.h>

void CLOCK_XOSCHF_crystal_PLL_init(void);
void TIMER_TCD0_init(void);

int main(void)
{
    CLOCK_XOSCHF_crystal_PLL_init();
    TIMER_TCD0_init();

    /* Replace with your application code */
    while(1)
    {
    }
}


void CLOCK_XOSCHF_crystal_PLL_init(void)
{
    /* Enable crystal oscillator with frequency range 16 MHz and 4K cycles
start-up time */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
                | CLKCTRL_CSUTHF_4K_gc
                | CLKCTRL_FRQRANGE_16M_gc
                | CLKCTRL_SELHF_CRYSTAL_gc
                | CLKCTRL_ENABLE_bm);
```

```
    /* Confirm crystal oscillator start-up */
    while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
    {
        ;
    }

    /* Set the PLL to use XOSCHF as source, and select 3x multiplication
factor */
    ccp_write_io((uint8_t *) &CLKCTRL.PLLCTRLA, CLKCTRL_SOURCE_bm |
CLKCTRL_MULFAC_3x_gc);

    /* Clear RUNSTDBY for power save during sleep */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL.XOSCHFCTRLA &
~CLKCTRL_RUNSTDBY_bm);
}


void TIMER_TCD0_init(void)
{
    /* Configure the TCD with PLL (48 MHz) as source */
    TCD0.CTRLA = TCD_CLKSEL_PLL_gc | TCD_CNTPRES_DIV1_gc |
TCD_SYNCPRES_DIV1_gc;

    /* Replace with your application configuration */

    /* Enable TCD0 */
    TCD0.CTRLA |= TCD_ENABLE_bm;
}
```

Example 12-6. CFD on XOSCHF

```
#define F_CPU 16000000ul

#include <avr/io.h>
#include <avr/cpufunc.h>
#include <avr/interrupt.h>

void CLOCK_XOSCHF_crystal_init(void);
void CLOCK_CFD_XOSCHF_init(void);

static inline void LED0_init(void)
{
    PORTB.DIRSET = PIN3_bm;
    PORTB.OUTSET = PIN3_bm;
}

static inline void LED0_toggle(void)
{
    PORTB.OUTTGL = PIN3_bm;
}

int main(void)
{
    CLOCK_XOSCHF_crystal_init();
    CLOCK_CFD_XOSCHF_init();
    LED0_init();

    /* Enable global interrupts */
    sei();

    /* Replace with your application code */
    while(1)
    {
    }
}


void CLOCK_XOSCHF_crystal_init(void)
{
    /* Enable crystal oscillator
     * with frequency range 16 MHz and 4K cycles start-up time
     */
```

```
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
                 | CLKCTRL_CSUTHF_4K_gc
                 | CLKCTRL_FRQRANGE_16M_gc
                 | CLKCTRL_SELHF_CRYSTAL_gc
                 | CLKCTRL_ENABLE_bm);

    /* Confirm crystal oscillator start-up */
    while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
    {
        ;
    }
}


void CLOCK_CFD_XOSCHF_init(void)
{
    /* Enable Clock Failure Detection on XOSCHF */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLC, CLKCTRL_CFDSRC_XOSCHF_gc |
CLKCTRL_CFDEN_bm);

    /* Enable regular interrupt for CFD */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKINTCTRL, CLKCTRL_CFD_bm);
}


ISR(CLKCTRL_CFD_vect)
{
    /* This interrupt will trigger every time the CFD detects XOSCHF has
stopped
     * The Main Clock source is OSCHF so the CPU is not affected
     */
    LED0_toggle();

    /* Clear the CFD interrupt flag */
    CLKCTRL.MCLKINTFLAGS = CLKCTRL_CFD_bm;
}
```

Example 12-7. CFD on Main Clock with NMI

```
#define F_CPU 16000000ul

#include <avr/io.h>
#include <avr/cpufunc.h>
#include <avr/interrupt.h>
#include <util/delay.h>

void CLOCK_XOSCHF_crystal_init(void);
void CLOCK_CFD_CLKMAIN_init(void);

static inline void LED0_init(void)
{
    PORTB.DIRSET = PIN3_bm;
}

static inline void LED0_toggle(void)
{
    PORTB.OUTTGL = PIN3_bm;
}

int main(void)
{
    CLOCK_XOSCHF_crystal_init();
    CLOCK_CFD_CLKMAIN_init();
    LED0_init();

    /* Enable global interrupts */
    sei();

    /* Replace with your application code */
    while(1)
    {
        LED0_toggle();
        _delay_ms(200);
```

```
    }
}


void CLOCK_XOSCHF_crystal_init(void)
{
    /* Enable crystal oscillator
     * with frequency range 16 MHz and 4K cycles start-up time
     */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL_RUNSTDBY_bm
                 | CLKCTRL_CSUTHF_4K_gc
                 | CLKCTRL_FRQRANGE_16M_gc
                 | CLKCTRL_SELHF_CRYSTAL_gc
                 | CLKCTRL_ENABLE_bm);

    /* Confirm crystal oscillator start-up */
    while(!(CLKCTRL.MCLKSTATUS & CLKCTRL_EXTS_bm))
    {
        ;
    }

    /* Clear Main Clock Prescaler */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLB, 0x00);

    /* Set the main clock to use XOSCHF as source, and enable the CLKOUT pin */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLA, CLKCTRL_CLKSEL_EXTCLK_gc
                 | CLKCTRL_CLKOUT_bm);

    /* Wait for system oscillator changing to complete */
    while(CLKCTRL.MCLKSTATUS & CLKCTRL_SOSC_bm)
    {
        ;
    }

    /* Clear RUNSTDBY for power save when not in use */
    ccp_write_io((uint8_t *) &CLKCTRL.XOSCHFCTRLA, CLKCTRL.XOSCHFCTRLA &
~CLKCTRL_RUNSTDBY_bm);

    /* Change complete and the main clock is 16 MHz */
}


void CLOCK_CFD_CLKMAIN_init(void)
{
    /* Enable Clock Failure Detection on main clock */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKCTRLC, CLKCTRL_CFDSRC_CLKMAIN_gc
                 | CLKCTRL_CFDEN_bm);

    /* Enable interrupt for CFD */
    ccp_write_io((uint8_t *) &CLKCTRL.MCLKINTCTRL, CLKCTRL_INTTYPE_bm
                 | CLKCTRL_CFD_bm);
}


ISR(NMI_vect)
{
    /* Check which NMI has triggered*/
    if(CLKCTRL.MCLKINTFLAGS & CLKCTRL_CFD_bm)
    {
        /* This interrupt will trigger if the source for the main clock fails
        * and the CFD is able to switch to a different working clock.
        * In this case that means XOSCHF has failed and is replaced by OSCHF.
        * The main clock is therefore reduced to 4 MHz / 2 = 2 MHz.
        */

        /* Toggle the LED forever */
        while(1)
        {
            LED0_toggle();
            _delay_ms(200); // 200 ms calculated from 16 MHz == 1600 ms
        }

    }
    else
    {
        /* A different NMI has been triggered */
```

```
    }

    /* Non-Maskable Interrupt bits can only be cleared by a reset */
}
```

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