ENT-AN1175
Application Note
Protocol Transfer Mode

June 2016

Microsemi
a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

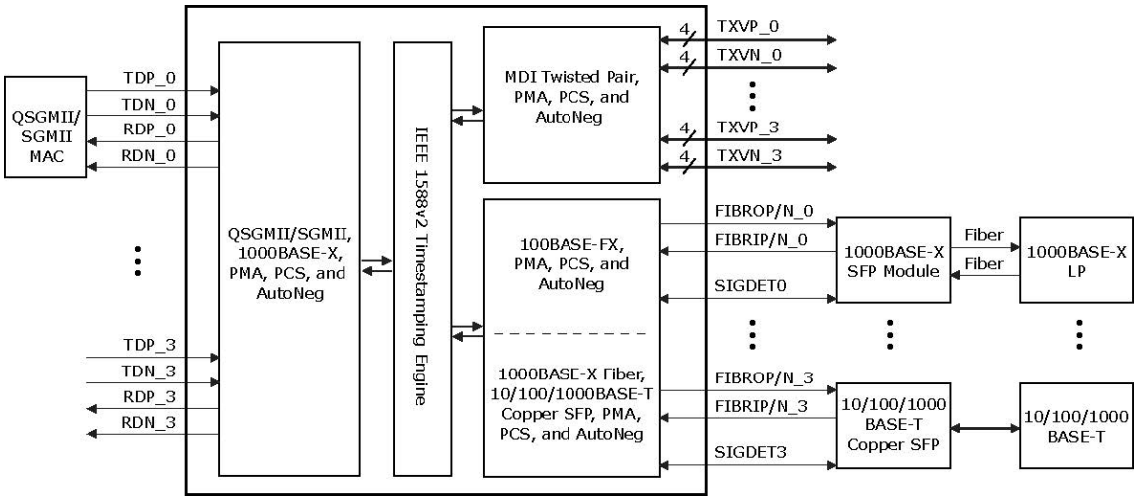
2 Protocol Transfer Mode

Protocol transfer mode is a feature that links a fiber module or triple-speed 10/100/1000BASE-T copper SFP to the QSGMII or SGMII MAC through a Gigabit Ethernet PHY. SGMII to QSGMII conversion can also be accomplished using this mode. Protocol transfer mode is supported in several newer generation Microsemi PHY devices.

This document describes important considerations for implementing protocol transfer mode. Refer to the Microsemi website for additional details regarding what devices support this feature. Additional information is available in the Microsemi PHY device datasheets, the IEEE 802.3 CSMA/CD Access Method and Physical Layer Specification, and ENG-46158 Serial SGMII Specification.

The following illustration shows the functional blocks of an example PHY supporting protocol transfer mode.

Figure 1 • Example PHY Block Diagram



2.1 Half-Duplex Mode in Protocol Transfer

Half-duplex mode has an inherently higher latency compared to full-duplex mode, thus we recommend to set the packet length less than 1518 bytes. The larger frame size may possibly cause CRC errors due to increased delay.

2.2 Device-Specific Considerations

Some early device revisions contain protocol transfer mode limitations. Additional details can be found in each device's datasheet. For these devices, protocol transfer is not functional at 10 Mbps link speed. At 100 Mbps, it is only functional within a limited range of PPM offsets. Protocol transfer is functional at 1000 Mbps in standard mode (Basic Protocol Transfer Mode, page 6) as auto-negotiation must be enabled on the MAC device, PHY, and copper SFP module whereas forced-speed protocol transfer mode cannot be used.

The following table lists the devices affected by this limitation.

Table 1 • Affected Devices

Device	Affected Device Model Number (3.9:4)	Affected Device Revision Number (3.3:0)
VSC8504XKS	0x0C	0x0 or 0x1
VSC8504XKS-03	0x0C	0x0 or 0x1

Device	Affected Device Model Number (3.9:4)	Affected Device Revision Number (3.3:0)
VSC8552XKS	0x0E	0x0 or 0x1
VSC8552XKS-03	0x0E	0x0 or 0x1
VSC8572XKS	0x0D	0x0 or 0x1
VSC8572XKS-03	0x0D	0x0 or 0x1
VSC8574XIC-03	0x0A	0x0 or 0x1
VSC8574XIC-10	0x0A	0x0 or 0x1
VSC8574XKS-03	0x0A	0x0 or 0x1
VSC8574XKS-10	0x0A	0x0 or 0x1

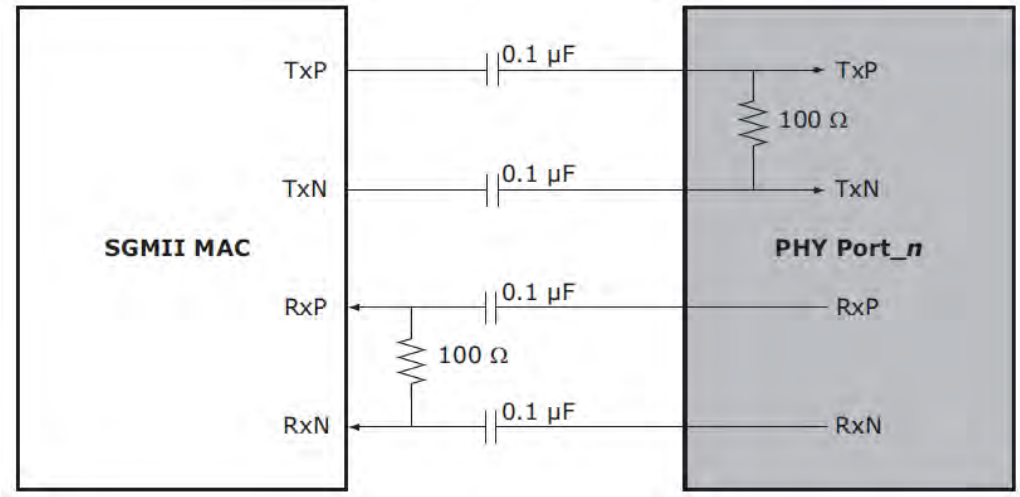
3 Hardware Overview

3.1 SGMII MAC Interface

When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the PHYs can be connected to an SGMII-compatible MAC. To configure the devices for SGMII MAC mode, set register 19G, bits 15:14 = 00, register 18G = 0x80F0 (to enable all four ports), and register 23, bit 12 = 0.

The following illustration shows the SGMII MAC interface connection.

Figure 2 • SGMII MAC Interface Connection

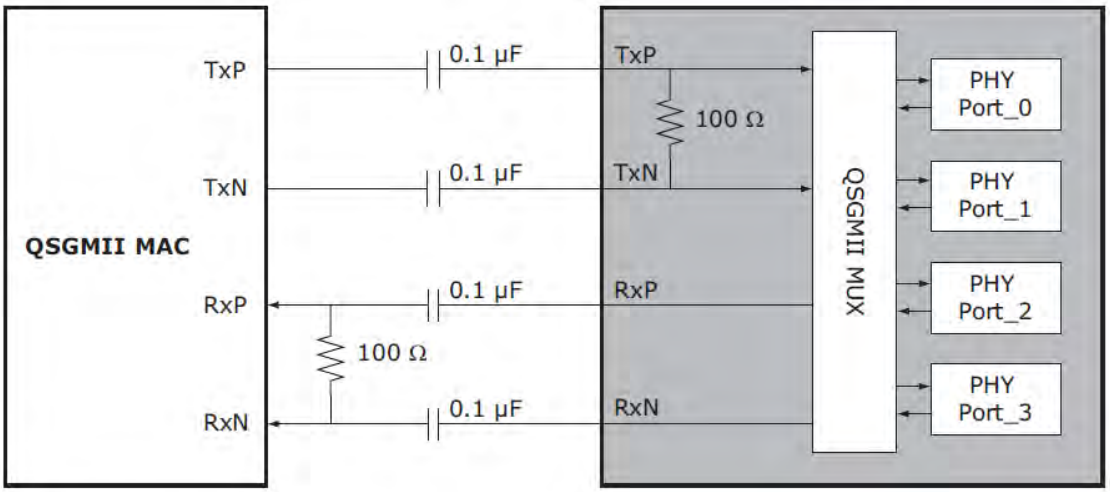


3.2 QSGMII MAC Interface

Several Microsemi PHY devices support a QSGMII MAC to convey four ports of network data and port speed between 10BASE-T, 100BASE-T, and 1000BASE-T data rates. They operate in both half-duplex and full-duplex at all port speeds. To configure the devices for QSGMII MAC mode, set register 19G, bits 15:14 = 01, and register 18G = 0x80E0.

The following illustration shows the QSGMII MAC interface connection.

Figure 3 • QSGMII MAC Interface Connection

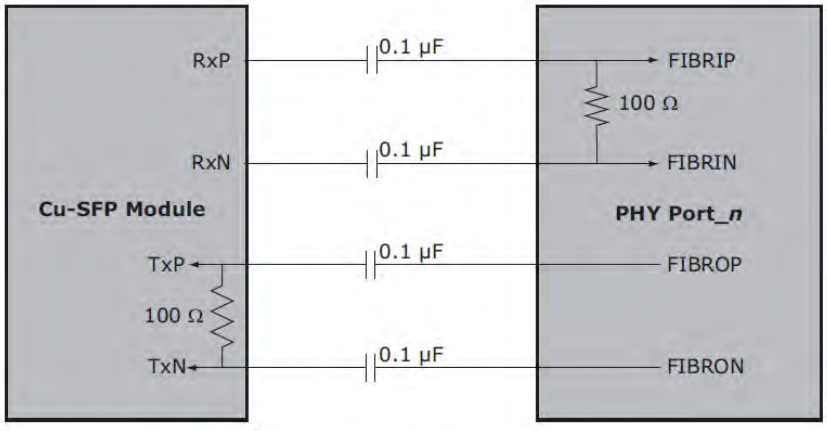


3.3 SerDes Media Interface

The SerDes media interface performs data serialization and de-serialization functions using an integrated SerDes block. This interface operates at 1.25 Gbps, providing full-duplex and half-duplex for 10/100/1000 Mbps bandwidth that can connect directly to 100BASE-FX/1000BASE-X-compliant optical devices as well as to 10/100/1000BASE-T copper SFP transceivers. The SerDes media block has the termination resistor integrated into the device. To enable the SerDes Media interface, set register 18G = 0x8FC1 (for all four ports). For more information, see the 18G register descriptions in the device datasheet.

The following illustration shows the SerDes media connection.

Figure 4 • SerDes Media Connection



Module may already contain AC coupling caps internally

3.4 SIGDET Pin Connection

The SIGDET pin should be connected to the LOS signal from an SFP module. SIGDET polarity is controlled by register 19E1, bit 0 and can be changed from the default active high (invert of LOS) to active low (compatible with LOS).

4 Basic Protocol Transfer Mode

4.1 Configuration

In order for protocol transfer mode to function properly with 10/100/1000BASE-T copper SFPs, it is important to have the MAC device (switch or ASIC), PHY, and copper SFP operate under the same speed assumption. The auto-negotiation of the MAC device needs to be enabled, clause 37 auto- negotiation on the SGMII MAC side of the copper SFP should be enabled, and auto-negotiation for both the media and MAC SerDes must be enabled for the Microsemi PHY.

The following register settings are required to configure the Microsemi PHY into protocol transfer mode.

- Register 23, bits 10:8 = 001. A soft reset is required after changing the PHY operating mode in register 23 (unless the PHY is currently in the COMA mode).
- Register 0, bit 12 = 1 (enable ANEG for media interface).
- Register 16E3, bit 7 = 1 (enable ANEG for MAC SerDes).

When using the unified PHY API, the following functions/parameters are used to enable protocol transfer mode. These sequences can be combined into the initialization sequence of the PHY when configuring MAC/media modes.

- vtss_phy_reset_get()- Retrieve the vtss_phy_reset_conf_t struct
- Set "media_if" = VTSS_PHY_MEDIA_IF_SFP_PASSTHRU
- vtss_phy_reset()- Reset the port with the appropriate media interface
- vtss_phy_conf_get()- Get the PHY configuration and update as appropriate
- Set "mode" = VTSS_PHY_MODE_ANEG
- Ensure "sigdet" is set appropriately with either VTSS_PHY_SIGDET_POLARITY_ACT_HIGH or VTSS_PHY_SIGDET_POLARITY_ACT_LOW
- vtss_phy_conf_set()- Set the PHY configuration for the updated media interface

After the unified PHY API sets the configuration for the PHY with protocol transfer mode enabled, one of two things will occur. For ports configured with ANEG enabled, the PHY sets into auto-negotiation mode and the ANEG configuration from the copper SFP module is passed through to the PHY through clause 37. For ports configured in forced mode (see Forced-speed Protocol Transfer Mode), the PHY remains set to auto-negotiation mode and the speed setting from the copper SFP is used to properly configure the PHY's rate adaptation block.

4.2 Status Monitoring

When all three entities have auto-negotiation enabled, register 26E3 provides the status of the clause 37 auto-negotiation. If register 26E3, bit 0 = 1, the media SerDes is in SGMII mode and the remaining bits on this register reflect the configuration code word of the SGMII standard. In this case, bit 15 indicates link status, bit 12 indicates duplex mode, and bits 11:10 indicate operating speed.

The link status will generally stay up, but will toggle down and then up upon any SFP link up or down event as a result of the change in autoneg codewords being sent. If enabled, an interrupt due to a change in link status will be generated in this situation.

When using the unified PHY API, the following function/parameter is used to retrieve status for protocol transfer mode.

- vtss_phy_status_get()- Retrieve the vtss_port_status_t struct

For API versions prior to 4.67.01, the link status, speed, and duplex reflected in the status are for the Microsemi PHY and not the PHY inside the SFP, which is the actual external interface. The user application will have to read these values as described. For API version 4.67.01 and later, the link status, speed, and duplex indication in the PHY status will be from the clause 37 auto-negotiation parameters relative to the external link partner.

5 Forced-speed Protocol Transfer Mode

5.1 Configuration

In the event that either the MAC device is not capable of auto-negotiation or the copper SFP auto-negotiation cannot be enabled, the Microsemi PHY has the capability to support forced link-speed in protocol transfer mode. To utilize this, the auto-negotiation on both the MAC device and the copper SFP SGMII must first be disabled and then auto-negotiation for both the media and MAC SerDes must be enabled for the Microsemi PHY. Set register 16E3, bit 11 =1 and then write the following values to register 18E3 (according to copper SFP link speed).

- If copper SFP operates at 1000 M - Set register 18E3 = 0x8801
- If copper SFP operates at 100 M - Set register 18E3 = 0x8401
- If copper SFP operates at 10 M - Set register 18E3 = 0x8001

When using the unified PHY API, the following functions/parameters are used to enable protocol transfer mode. These sequences can be combined into the initialization sequence of the PHY when configuring MAC/media modes

- vtss_phy_reset_get()- Retrieve the vtss_phy_reset_conf_t struct
- Set "media_if" = VTSS_PHY_MEDIA_IF_SFP_PASSTHRU
- vtss_phy_reset()- Reset the Port with the appropriate media interface
- vtss_phy_conf_get()- Get the PHY configuration and update as appropriate
- Set "mode" = VTSS_PHY_MODE_FORCED
- Ensure "sigdet" is set appropriately with either VTSS_PHY_SIGDET_POLARITY_ACT_HIGH or VTSS_PHY_SIGDET_POLARITY_ACT_LOW
- vtss_phy_conf_set()- Set the PHY configuration for the updated media interface

After the unified PHY API sets the configuration for the PHY with protocol transfer mode enabled, one of two things will occur. For unified PHY API 4.65 or later, when the port is configured in forced mode, the PHY remains set to auto-negotiation mode and the speed setting from the copper SFP is used to properly configure the PHY's rate adaptation block. For API versions prior to 4.65, when the port is configured in forced mode, the PHY would also be set to forced speed, which causes issues with the SFP as the forced speed is still passed through to the SFP module. To fix this particular issue, the register 0 settings must be reverted to enable ANEG.

5.2 Link Speed Monitoring

The Microsemi PHY also provides a link speed monitoring capability for forced-speed protocol transfer mode through register 24E3 bits 13:12:

- If bits 13:12 =00, then the port is in 1000 M
- If bits 13:12 =10, then the port is in 100 M
- If bits 13:12 =01, then the port is in 10 M

Link speed monitoring works in both auto-negotiation enabled and forced-speed modes. When using the unified PHY API, the following function/parameter is used to retrieve status for protocol transfer mode.

- vtss_phy_status_get()- Retrieve the vtss_port_status_t struct

For API versions prior to 4.67.01, the link status, speed, and duplex reflected in the status are for the Microsemi PHY and not the PHY inside the SFP, which is the actual external interface. The user application will have to read these values as described. For API version 4.67.01 and later, the link status, speed, and duplex indication in the PHY status will be from the clause 37 parameters relative to the external link partner.

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

VPPD-04180