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## PIC24FJXXGAXXX to PIC24FXXKAXXX Migration Guide

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### INTRODUCTION

The PIC24FXXKAXXX (PIC24F 'K') device family includes many new features and is the low-power extension of Microchip's PIC24FJXXGAXXX (PIC24F 'J') device family, with standby current as low as 20 nA.

The distinguishing features of the PIC24FJXXKAXXX devices include:

- Supply Voltage (VDD and VDDCORE)
- Internal MCLR Option
  - MCLR pin can be configured as an input pin
- CodeGuard™ Security Features with the Boot Segment
- Data EEPROM Memory
- Programmable Brown-out Reset (BOR)
- 500 kHz LPFRC Oscillator
- Dedicated Memory Block for Configuration Bits

This document highlights the similarities and differences between the PIC24F 'J' and PIC24F 'K' device families. It also covers the general principles for migrating PIC24F 'J' applications to PIC24F 'K' devices.

Each section of this document describes one peripheral or major feature of the PIC24F 'K' device family. The sections are organized with the following information, as applicable:

- Comparison of PIC24F 'K' and PIC24F 'J' Peripheral Features
- List of new PIC24F 'K' Features
- List of any Unsupported PIC24F 'J' Features
- Summary of Migration Considerations

For more information on new or modified modules, refer to the specific PIC24F 'K' device data sheet (see [References](#)).

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# PIC24FXXKAXXX

## PIC24F 'K' FAMILY OVERVIEW

The PIC24F 'K' is a device family with low-power features and nanoWatt XLP technology. This family of devices is available in 14-pin, 20-pin, 28-pin and 44-pin packages and is largely pin compatible with other PIC24F products for easy migration.

Table 1 compares different features of the PIC24F 'J' and PIC24F 'K' device families.

**TABLE 1: COMPARISON BETWEEN PIC24F 'J' AND PIC24F 'K'**

| Feature Description                          | PIC24F 'J'                                                                                                                                                                                   | PIC24F 'K'                                                                                                                                                                                           |
|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operating Voltage                            | 2V to 3.6V                                                                                                                                                                                   | 1.8V to 3.6V or 2V to 5.5V                                                                                                                                                                           |
| Internal MCLR Option                         | No                                                                                                                                                                                           | Yes                                                                                                                                                                                                  |
| Option to Configure $\overline{\text{MCLR}}$ | No                                                                                                                                                                                           | Yes; as an input pin                                                                                                                                                                                 |
| Program Memory                               | Only General Segment<br>(16 Kbytes to 256 Kbytes)                                                                                                                                            | General Segment and Configurable<br>Boot Segment with CodeGuard™<br>Security Feature<br>(4 Kbytes to 32 Kbytes)                                                                                      |
| Data EEPROM Memory                           | Emulated                                                                                                                                                                                     | Yes                                                                                                                                                                                                  |
| BOR                                          | Fixed BOR                                                                                                                                                                                    | Programmable BOR                                                                                                                                                                                     |
| Device Configuration Bit Locations           | End of User Program Memory                                                                                                                                                                   | Dedicated Memory Locations in<br>Configuration Memory Space                                                                                                                                          |
| Device Programming Modes                     | Supports only Low-Voltage<br>Programming                                                                                                                                                     | Supports both Low-Voltage and<br>High-Voltage Programming                                                                                                                                            |
| Packages                                     | <ul style="list-style-type: none"><li>• 28-pin SPDIP, SSOP, SOIC, QFN</li><li>• 44-pin TQFP, QFN</li><li>• 64-pin TQFP, QFN</li><li>• 80-pin TQFP, QFN</li><li>• 100-pin TQFP, QFN</li></ul> | <ul style="list-style-type: none"><li>• 14-pin PDIP, TSSOP</li><li>• 20-pin PDIP, SSOC, SOIC, QFN</li><li>• 28-pin SPDIP, SSOP, SOIC, QFN</li><li>• 44-pin TQFP, QFN</li><li>• 48-pin UQFN</li></ul> |

## New PIC24F 'K' Family Features

In addition to the rich feature set of the PIC24F 'J' device families, the following new features are available to improve flexibility.

- **Supply Voltage** – The PIC24F 'K' devices are available in either 5V or 3.3V devices. The 5V devices have an on-chip 3.3V regulator to power the core, whereas the 3.3V devices have no regulator.
- **Low-Power Technology** – The standby power consumption of this device family is reduced to around 20 nA.
- **Program Memory with Boot Segment** – The program memory of this device family is divided into a General Segment (GS) and Boot Segment (BS). If a Boot Segment is enabled, then the CodeGuard security feature is available.
- **Data EEPROM** – The dedicated data EEPROM module can save and retrieve data, even when the power cycle occurs.
- **Programmable BOR** – The BOR trip voltage can be selected, and also, the BOR can be enabled or disabled.

## Unsupported PIC24F 'J' Family Features

The I/O pins of the PIC24F 'K' device family cannot have an input of more than  $V_{DD} + 0.3V$ .

## Migration Considerations

Consider the following when migrating from the PIC24F 'J' to the PIC24F 'K' family:

- **Supply Voltage** – The PIC24F 'J' parts require a voltage regulator to operate between 2.75V and 3.6V. PIC24F 'K' parts do not require a voltage regulator to operate at these voltages. PIC24F 'J'  $V_{DDCORE}$  and regulator enable pins are available as general purpose I/O for the PIC24F 'K' devices. PIC24F 'FV' devices are available that support 5V operation. These devices use an internal regulator similar to PIC24F 'J' parts.
- **MCLR Pin** – No changes are needed to MCLR when migrating from PIC24F 'J' to 'K' device families. An additional feature for the PIC24F 'K' devices is that MCLR can be configured as an input pin. High-Voltage Programming Entry mode must be used to disable the MCLR function by its respective Configuration bit. Note that the Low-Voltage Programming entry is then no longer available.
- **I/O Ports** – The PIC24F 'J' devices pins are grouped as 3.3V and 5.5V tolerant inputs. Only PIC24 'FV' families support 5.5V input voltages. If input voltages greater than 3.3V are needed, PIC24 'FV' devices must be used.

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## MEMORY ORGANIZATION, PROGRAM MEMORY AND DATA EEPROM MEMORY

[Table 2](#) compares different features of the PIC24F 'J' and PIC24F 'K' memory organization.

The program memory of the PIC24F 'K' device family can be divided into two segments: Boot Segment and General Segment. Both the segments have dedicated protection bits. The length of the Boot Segment can be configured.

**TABLE 2: COMPARISON BETWEEN PIC24F 'J' AND PIC24F 'K' MEMORY ORGANIZATION**

| Feature Description                | PIC24F 'J'                                | PIC24F 'K'                                                        |
|------------------------------------|-------------------------------------------|-------------------------------------------------------------------|
| Program Memory Size                | 16 Kbytes to 256 Kbytes                   | 4 Kbytes to 32 Kbytes                                             |
| Program Memory Segment             | Only General Segment                      | General Segment and Boot Segment with CodeGuard™ Security Feature |
| Erase Size                         | 512 Instructions                          | Programmable, 32/64/128 Instructions                              |
| Write Size                         | 64 Instructions                           | 32 Instructions                                                   |
| Data EEPROM                        | Emulated                                  | Yes                                                               |
| Device Configuration Bit Locations | Last Few Locations of User Program Memory | Specific Memory Locations in Configuration Space                  |

## New PIC24F 'K' Family Features

In addition to program memory with the General Segment of the PIC24F 'J' device family, the following new features are available to improve flexibility.

### PROGRAM MEMORY WITH BOOT SEGMENT

The Boot Segment option, along with the CodeGuard security feature, are available in the PIC24F 'K' device family. The size and security level of the Boot Segment are determined by Configuration bits, BSS<2:0>, of the FBS Configuration Word.

When the Boot Segment is configured, it starts from the 0x0200 location and the size is defined by the bits, BSS<2:0>. The General Segment follows the Boot Segment.

The Boot Segment is equipped with enhanced securities. The code or data in the Boot Segment cannot be accessed from outside of the Boot Segment. The basic restricted operation includes:

- Read, write and erase operations on the Boot Segment space from outside the Boot Segment are not allowed when standard or high security is enabled.
- Program flow change into the Boot Segment from outside the Boot Segment is not allowed when high security is enabled.
- While executing in the Boot Segment, a special code sequence is required to handle the interrupts and traps.

### DATA EEPROM MEMORY

In addition to the program memory and volatile data RAM, the PIC24F 'K' device family also includes non-volatile, on-chip data EEPROM. This memory segment allows users to store application information, such as identification, calibration constants, etc.

## Unsupported PIC24F 'J' Family Features

None.

## Migration Considerations

Consider the following when migrating from the PIC24F 'J' to the PIC24F 'K' family:

- The PIC24F 'K' device family has 4 Kbytes to 32 Kbytes of program memory. Therefore, the applications that require more than 32 Kbytes of memory cannot be migrated to PIC24F 'K' devices at this time.
- In PIC24F 'J' devices, the erase size is 512 instructions and the write size is 64 instructions. While in PIC24F 'K' devices, the erase size is configurable for 32, 64 or 128 instructions and the write size is 32 instructions.
- By default, the program memory of the PIC24F 'K' device family is configured as a single General Segment. Therefore, migrating an application from the PIC24F 'J' family does not require any changes.
- If the application uses an emulated data EEPROM to save data, the dedicated data EEPROM available on PIC24F 'K' devices can be used.
- If the device Configuration bits are defined in the source file, then the Configuration register names need to be changed to match the registers of the PIC24F 'K' device family. Refer to the respective data sheet for the device Configuration register details.

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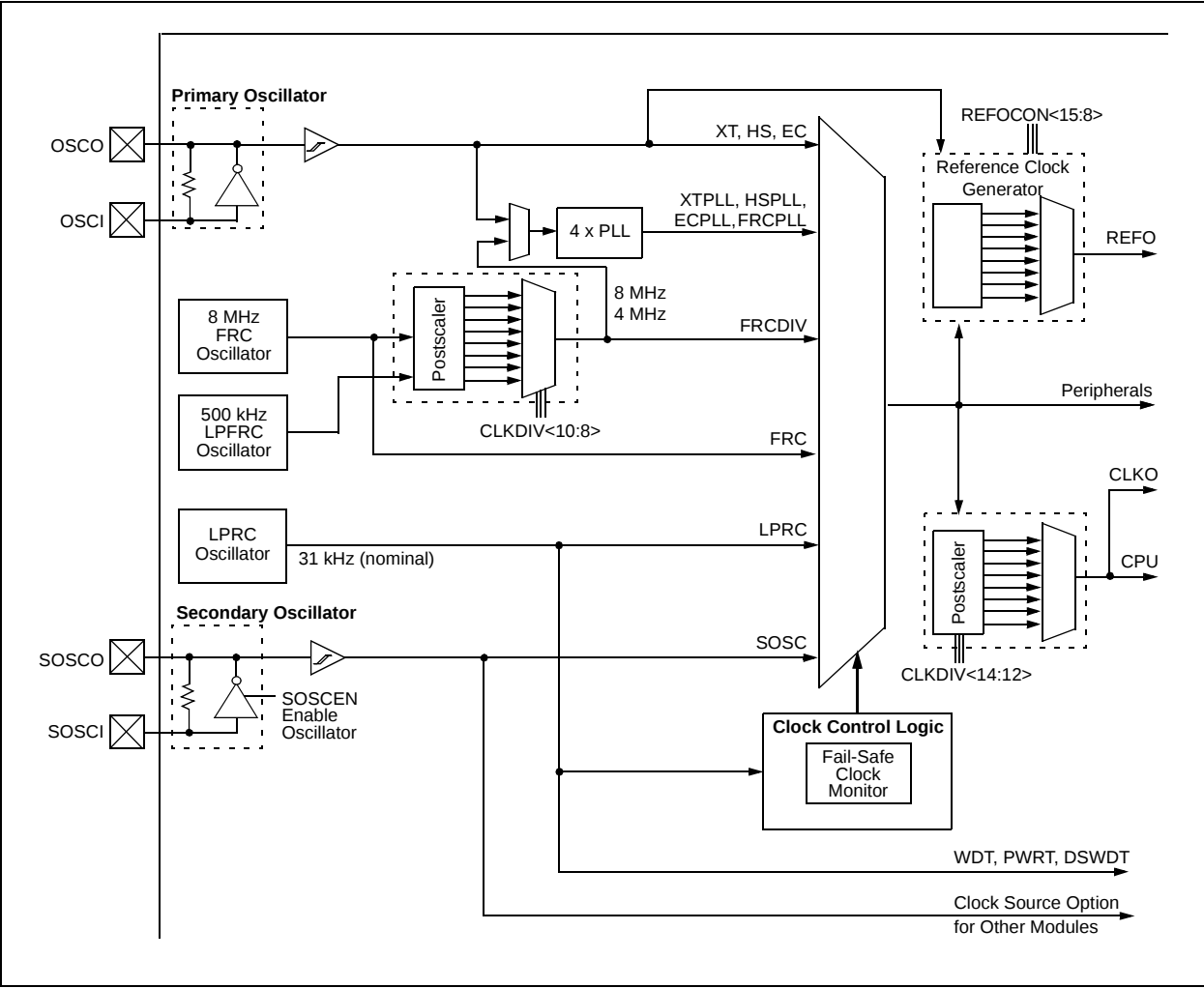
## POWER-MANAGED MODES/ OSCILLATOR CONFIGURATIONS

In addition to the PIC24F 'J' oscillator features, the PIC24F 'K' devices support an on-chip, 500 kHz LPRC oscillator.

TABLE 3: COMPARISON OF PIC24F 'J' AND PIC24F 'K' OSCILLATOR

| Feature Description                                  | PIC24F 'J' | PIC24F 'K' |
|------------------------------------------------------|------------|------------|
| Primary Oscillator with PLL Off (HS, XT, EC)         | Yes        | Yes        |
| Primary Oscillator with PLL On (HSPLL, XTPLL, ECPLL) | Yes        | Yes        |
| Secondary Oscillator                                 | Yes        | Yes        |
| 8 MHz FRC                                            | Yes        | Yes        |
| 8 MHz FRC with Postscaler                            | Yes        | Yes        |
| 8 MHz FRC with Postscaler and PLL                    | Yes        | Yes        |
| 500 kHz LPRC with Postscaler                         | No         | Yes        |
| 31 kHz LPRC                                          | Yes        | Yes        |

FIGURE 1: PIC24F 'K' OSCILLATOR BLOCK DIAGRAM



## New PIC24F 'K' Family Features

In addition to the 8 MHz FRC and 31 kHz LPRC internal RC oscillators, a 500 kHz LPFRC oscillator is added to the PIC24F 'K' device family. This oscillator shares the postscaler of 8 MHz FRC. Therefore, the operating frequency can be reduced to 1.95 kHz.

## Unsupported PIC24F 'J' Family Features

None.

## Migration Considerations

None.

## PROGRAMMABLE BROWN-OUT RESET (BOR)

The PIC24F 'J' device family has a fixed-point BOR circuitry, while the PIC24F 'K' device family has a BOR circuitry with four programmable trip points.

## New PIC24F 'K' Family Features

The BOR can be enabled or disabled, regardless of using or not using an on-chip regulator. The BOR trip point is programmable and one of the four trip points can be selected.

## Unsupported PIC24F 'J' Family Features

None.

## Migration Considerations

To migrate the 2V BOR feature to the PIC24F 'K' family, select the appropriate BOR trip point using the BOR<1:0> bits from the FPOR register.

### REGISTER 1: FPOR: RESET CONFIGURATION REGISTER

| R/P-1 | R/P-1                | R/P-1                | R/P-1   | R/P-1  | U-0 | R/P-1  | R/P-1  |
|-------|----------------------|----------------------|---------|--------|-----|--------|--------|
| MCLRE | BORV1 <sup>(1)</sup> | BORV0 <sup>(1)</sup> | I2C1SEL | PWRTEN | —   | BOREN1 | BOREN0 |
| bit 7 |                      |                      |         |        |     |        | bit 0  |

#### Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **MCLRE:**  $\overline{\text{MCLR}}$  Pin Enable bit

bit 6-5 **BORV<1:0>:** Brown-out Reset Enable bits<sup>(1)</sup>

11 = Brown-out Reset is set to the first trip voltage

10 = Brown-out Reset is set to the second trip voltage

01 = Brown-out Reset is set to the third trip voltage

00 = Low-power Brown-out Reset re-arms the POR circuit

bit 4 **I2C1SEL:** Alternate I2C1 Pin Mapping bit

bit 3 **PWRTEN:** Power-up Timer Enable bit

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits

11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled

10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled

01 = Brown-out Reset is controlled with the SBOREN bit setting

00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

**Note 1:** Refer to the electrical specifications in the specific device data sheet for BOR voltages. Note that the BOR voltages differ by device.

## SUMMARY

The preceding sections represent the most important considerations in migrating a PIC24F 'J' application to a PIC24F 'K' device. Although it is impractical to list every possible code to hardware implementation, this document should be considered as a check list of the most important differences and similarities.

Additional features, such as data EEPROM, provide new applications for the PIC24F 'K' family that were not possible with PIC24F 'J' device families. It is important to review an application, before migration, to decide how the code and hardware design must be changed to work on the PIC24F 'K' device family.

## REFERENCES

For more specific information on the device families referenced in this document, refer to the following data sheets and PIC24F reference manual:

- *"PIC24F16KA102 Family Data Sheet"* (DS39927)
- *"PIC24F04KA201 Family Data Sheet"* (DS39937)
- *"PIC24FJ64GA004 Family Data Sheet"* (DS39881)
- *"PIC24FJ64GA104 Family Data Sheet"* (DS39951)
- *"PIC24F Family Reference Manual", Section 2. CPU* (DS39703)
- *"PIC24F Family Reference Manual", Section 5. Data EEPROM* (DS39720)
- *"PIC24F Family Reference Manual", Section 6. Oscillator* (DS39700)
- *"PIC24F Family Reference Manual", Section 7. Reset* (DS39712)
- *"PIC24F Family Reference Manual", Section 38. Oscillator with 500 kHz Low-Power FRC* (DS39726)
- *"PIC24F Family Reference Manual", Section 40. Reset with Programmable Brown-out Reset* (DS39728)

There are other Microchip data sheets and reference materials available for PIC24F devices that may be helpful in planning the migration of an application. For a complete list of available materials, visit the Microchip corporate web site at:

[www.microchip.com](http://www.microchip.com)

## DOCUMENT REVISION HISTORY

### Revision A Document (2/2011)

This is the initial release of this document. This revision includes introduction to the PIC24F 'K' device family, the differences from the PIC24F 'J' device family and the migration considerations.

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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