FEATURES

The SY89875U features:

- **Integrated programmable clock divider and 1:2 fanout buffer**
- **Guaranteed AC performance over temperature and voltage**
- **Low jitter design**
- **Unique input termination and VT pin**
- **LVDS-compatible outputs**
- **TTL/CMOS inputs for select and reset**
- **Parallel programming capability with divider ratios of 1, 2, 4, 8, and 16**
- **2.5V low voltage operation**
- **Output disable function**
- **–40°C to +85°C temperature range**

The SY89875U evaluation board features:

- **AC-coupled I/O with SMA connectors**
- **DIP switch controlled select and reset**
- **Fully assembled and tested**

AVAILABLE MEASUREMENTS

The SY89875U evaluation board allows the following measurements:

- **Frequency performance**
- **Jitter**
- **Output rise/fall time**
- **Output amplitude**

EVALUATION BOARD

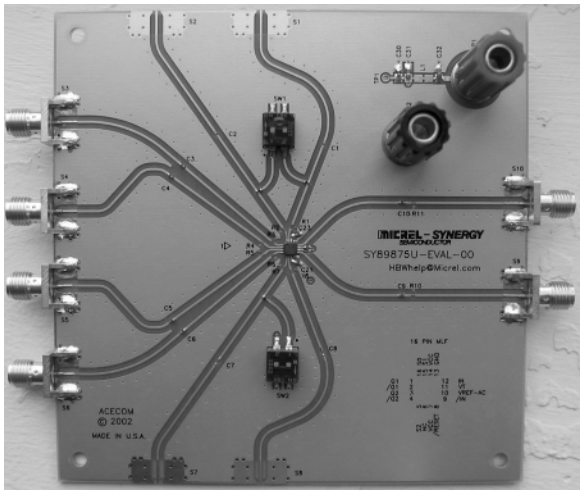

Figure 1. SY89875U Evaluation Board

DESCRIPTION

This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622MHz or higher) CML, LVPECL, LVDS or HSTL clock input signal and dividing down the frequency using a programmable divider to create a lower speed version of the input clock. Available divider ratios are 2, 4, 8 and 16, or straight pass-through.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN).

This manual provides information on the SY89875U evaluation board. It should be used in conjunction with the SY89875U data sheet, which contains full specifications of the SY89875U.

The SY89875U evaluation board enables fast and thorough evaluation of the SY89875U programmable clock driver. The board is an easy-to-use, 4-layer high-speed coplanar design that uses FR4 dielectric material to achieve high bandwidth. The layer stack is shown in Table 1.

The SY89875U evaluation board is designed to be driven by a high-speed 2GHz clock generator and is intended to be terminated to a 50Ω scope. These features allow the user to evaluate various parameters of the SY89875U, as listed in the “Available Measurements” section of this document.

Layer	Definition
1	Signal/GND
2	GND
3	VCC
4	GND

Table 1. SY89875U Evaluation Board Layer Stack-Up

MEASUREMENT SETUP

Equipment used for measurements:

1. Agilent 83752A Synthesized Sweeper
2. Agilent 70004A Display
3. Agilent 70843B Error Performance Analyzer
4. Agilent 86100A Wide-Bandwidth Oscilloscope
5. Agilent E3620A DC Power Supply
6. Matched High-Speed Cables w/SMA Connectors

Note:

Items 1 through 3 constitute the BERT stack.

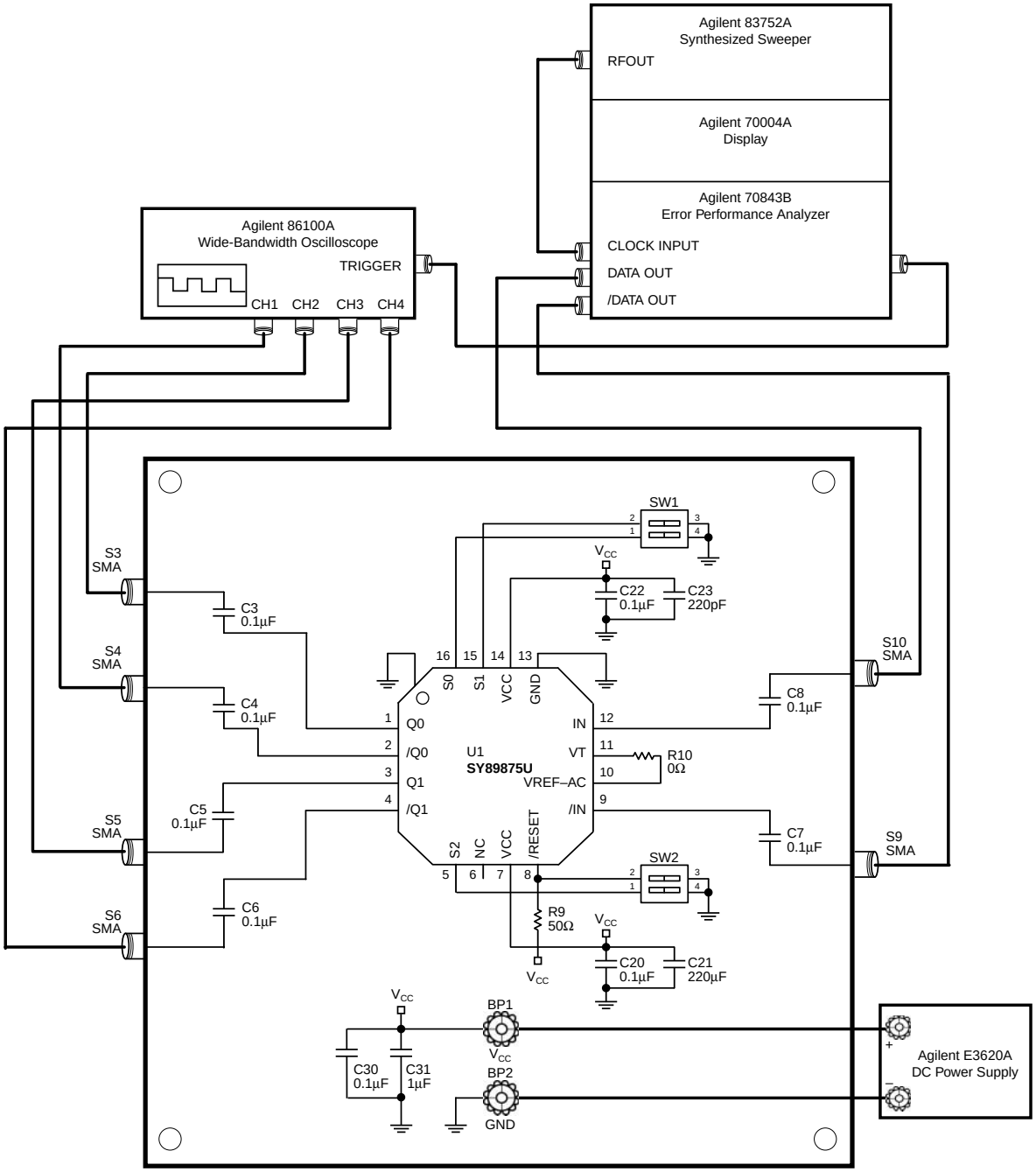

Figure 2. Setup for Measurements

SETUP FOR MEASUREMENTS

This section explains how to connect and setup the SY89875U evaluation board per Figure 2. Ensure proper ESD precautionary measures are taken before handling sensitive electronic equipment, including the SY89875U evaluation board.

1. Set E3620A to output 2.5V and then turn off E3620A. Connect E3620A's positive lead to BP1, negative lead to BP2.
2. Configure Agilent BERT stack:
   a. Set the 83752A Synthesized Sweeper to 2.0GHz.
   b. From the 70004A's Trigger menu:
      i. Choose clock as trigger output.
      ii. Choose CLK/8 for divider.
   c. From the 70004A's Clock menu:
      i. External Termination = DC termination 0V.
      ii. Attenuation = 0dB.
      iii. Amplitude = 400mV (800mV$_{pp}$).
      iv. Hi-Level = 0V.
      v. Polarity = NORMAL.
3. Connect 70843V's trigger output to 86100A's trigger input.
4. Connect IN, /IN (S10, S9) on SY89875U evaluation board to 70843V's clock outputs.
5. Connect both output pairs Q0, /Q0 and Q1, /Q1 (S3, S4 and S5, S6) on SY89875U evaluation board to 86100A's inputs.
   a. For best performance, both sets of outputs MUST be terminated even though they may not be used!
6. Choose desired divider operation.
   a. Set switch 1 of SW1 OFF to set S0 HIGH.
   b. Set switch 2 of SW1 OFF to set S1 HIGH.
   c. Set switch 1 of SW2 OFF to set S0 HIGH.
7. Set switch 2 of SW2 OFF to enable device.
8. Turn on E3620A. Typical power supply current should be ~70mA. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!
9. Configure 86100A oscilloscope.
   a. Verify a trigger signal is present by checking that the Trigger Source button is lit.
      i. Depress this button to choose external source if necessary.
      ii. Adjust trigger level if necessary.
   b. Press Oscilloscope Mode on front panel.
   c. Choose Time Measurements from onscreen display.
      i. Choose Rise Time, Fall Time and Jitter.
   d. Choose Amplitude Measurements from onscreen display.
      i. Choose Amplitude.

MEASUREMENTS

The SY89875U evaluation board assumes the use of a 50Ω scope to terminate the SY89875U. The following sections detail various measurements that the SY89875U evaluation board allows.

1. Set 70004's Data amplitude to 400mV (800mV$_{pp}$).
   b. Press Autoscale on oscilloscope. The eye pattern should automatically display on the scope. If not, verify that the steps listed in the "Setup for Measurements" section are completed. Sometimes the waveform needs to be manually adjusted to fit the display. Use the Time Scale and Voltage Scale knobs on the front panel of the scope to adjust this.
   c. Observe measurements on scope's display. The rise and fall times should be around 120ps, amplitude around 350mV (700mV$_{pp}$).

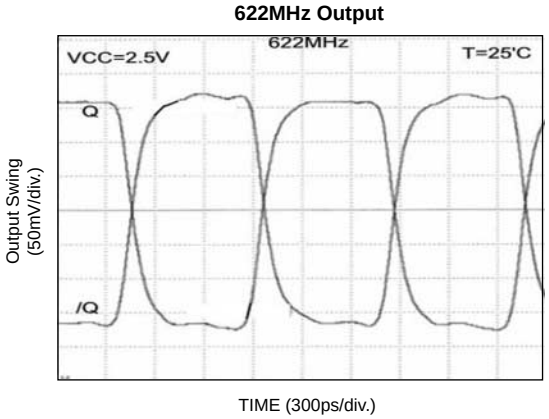

Figure 3. Typical SY89875U Output at 2.5V, 25°C, 622MHz

FREQUENTLY ASKED QUESTIONS

I just got my SY89875U evaluation board and I cannot get anything to work! Where should I start?

First, check the power supplies. Typical power supply current should be ~70mA. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!

If that looks okay, ensure the outputs are enabled by setting switch 2 of SW2 OFF.

Next, verify the 70004A's Clock outputs are enabled and there's sufficient amplitude (at least 200mV_{pp}) to drive the SY89875U.

If the above are okay and there's still nothing displaying on the scope, then there's most likely a trigger setup issue with the scope. Look on the scope's front panel and verify that the instrument is triggered. The Trigger Source button should be lit if a trigger signal is present. If not, press the button until the external trigger is selected. Also, try adjusting the level until a signal is found. If this does not work, verify the 70004A is set to output a CLK/8 trigger signal as described in the "Setup for Measurements" section of this document.

Can you suggest a bypass/decoupling scheme?

Figure 2 shows the power supply decoupling scheme used for the SY89875U evaluation board. The "Bill of Materials" at the end of this document lists the supplier and component values. We have found this arrangement to be an excellent starting point.

What layout tips do you have?

1. Establish controlled impedance stripline, microstrip or coplanar construction techniques for high-speed signal paths.

2. All differential paths are critical timing paths and skew should be matched to within ±10ps.

3. Signal trace impedance should not vary more than ±5%. If in doubt, perform Time Domain Reflectometry (TDR) analysis of signal traces.

4. Place power supply decoupling capacitors as close as possible to the device's power pins.

What is Time Domain Reflectometry (TDR)?

TDR is used to verify impedance continuity along a signal path. Many interconnects, such as SMA, if not launched correctly onto the PCB, will exhibit inductive-like resonance with an abrupt capacitive discontinuity. This discontinuity will subtract signal from the inputs and outputs, effectively closing the resulting data eye. The 86100A allows TDR testing and is a useful tool to help evaluate your PCB.

I still have questions. Who should I contact?

Micrel's HBW applications helpline is available to assist you. Please call (408) 955-1690 or email hbwhelp@micrel.com for assistance.

BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty
BP1	111-0702-001	Johnson(1)	red binding post	1
BP2	111-0703-001	Johnson(1)	black binding post	1
C3, C4, C5, C6, C9, C10, C20, C22, C30	PCC1731CT-ND	Panasonic(2)	0.1µF surface mount capacitor, size 0402	9
C21, C23	PCC1706CT-ND	Panasonic(2)	220pF surface mount capacitor, size 0402	2
C31, C32	PCC1915CT-ND	Panasonic(2)	1µF surface mount capacitor, size 0603	2
S3, S4, S5, S6, S9, S10	142-0701-851	Johnson(1)	end launch SMA	6
R9	CRCW040249R9F	Vishay(3)	49.9Ω surface mount resistor, size 0402	1
R10	CRCW04020R00F	Vishay(3)	0.0Ω surface mount resistor, size 0402	1
SW1, SW2	CKN3054-ND	Panasonic(2)	2-DIP switch	2
U1	SY89875U	**Micrel, Inc.**(4)	2.5V, 2.0GHz Programmable Clock Divider	1

Notes:

1. Johnson tel: 800-247-8256
2. Panasonic tel: 800-344-2112
3. Vishay tel: 402-563-6866
4. Micrel, Inc. tel: 408-944-0800

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