VSC7423/8/9

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC7423/8/9 Carrier Ethernet switches. These checklist items should be followed when utilizing the VSC7423/8/9 in a new design. A summary of these items is provided in Section 8.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power/Ground"
- Section 4.0, "Interfaces"
- Section 5.0, "Miscellaneous Signals"
- Section 6.0, "Port Configuration"
- Section 7.0, "Internal Copper PHY Ports"

2.0 GENERAL CONSIDERATIONS

The switches in this family can be summarized in Table 2-1.

TABLE 2-1: FAMILY SWITCHES

Caracal Family		Max	Port Breakdown			
Device	**Mode**	**Ports**	**#1G Copper**	**#1G SGMII**	**#2.5 SGMII**	**#QSGMII**
VSC7423	0	7	5	5	2	0
VSC7428	0	11	8	9	2	0
VSC7429	0	26	12	1	1	3
	1		12	10	2	0
	2		10	8	0	0

2.1 Required References

The VSC7423/8/9 implementor should have the following documents on hand:

- *VSC7423-02 Datasheet - Caracal Family - VMDS-10431*
- *VSC7428-02 and VSC7429-02 Datasheet - VMDS-10394*
- *Section 15 Design Considerations* in the VSC7424-02/5/6/7 Data Sheet (in lieu of an errata document)
- *VSC5611EV Reference Design Files for the SparX-III Managed/Caracal Evaluation Board*
- *ENT-AN1263-4.5 - Application Note – Flash Configuration Design Guide - VPPD-04628*
- *ENT-AN1015-1.0 - Application Note – Using the SparX-III Serial GPIO/LED Controller*

2.2 Pin Check

- Check the pinout of the part against the data sheet.
- Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Strapping Pins

- The pins **VCORE_CFG[2:0]** and **VCORE_ICE_NEN** control how the VCore-III CPU is supported. (There are no other strapping/configuration pins. See Table 2-2.)

TABLE 2-2: VCORE-III CONFIGURATION STRAPPING PINS

VCore_CFG [*n*]			Behavior
***n* = 2**	***n* = 1**	***n* = 0**	
Endian (Note 1)	0	0	MIPS is enabled and boots up from SI.
Endian (Note 1)	0	1	Automatic boot is disabled by forcing the MIPS into Reset. SI Client mode is enabled. The MIPS can be manually started from the DDR.
Endian (Note 1)	1	0	Automatic boot is disabled by forcing the MIPS into Reset. PI and SI Client modes are enabled. The MIPS can be manually started from the DDR or Flash on the SI interface.
Endian (Note 1)	1	1	Automatic boot is disabled by forcing the MIPS into Reset. SI Client mode is enabled. The MIPS can be manually started from the DDR or Flash on the SI interface.

Note 1: Little Endian mode: VCore_CFG [2] = 0; Big Endian mode: VCore_CFG [2] = 1

- The EJTAG interface of the VCore-III CPU and the device's Boundary Scan JTAG controller are both multiplexed onto the JTAG interface of the device. When the **VCORE_ICE_NEN** (**VCORE ICE NOTENABLED**) pin is low, the MIPS's EJTAG controller is selected. When the **VCORE_ICE_NEN** pin is high, the Boundary Scan JTAG controller is selected.

The reference clock is sourcing an internal 5 GHz PLL, which provides various clock outputs to the Switch core, MCU, and SerDes macros.

- The device reference clock can be a 25 MHz, 125 MHz, 156.25 MHz, or 250 MHz clock signal. It can be either a differential reference clock or a single-ended clock. However, 25 MHz single-ended operation is not recommended when using QSGMII due to the jitter specification requirements to this interface.

The reference clock speed is selected by the RefClk_Sel[2:0] pins. See Table 2-3.

TABLE 2-3: REFERENCE CLOCK SPEED

Name	Pin Coding	RefClk_Sel2	RefClk_Sel1	RefClk_Sel0
RefClk_Sel[2:0]	000:125 MHz (default)	Pull down or Float	Pull down or Float	Pull down or Float
	001:156.25 MHz	Pull down or Float	Pull down or Float	Pull up or VDDIO
	010:250 MHz	Pull down or Float	Pull up or VDDIO	Pull down or Float
	100:25 MHz	Pull up or VDDIO	Pull down or Float	Pull down or Float
	All others values are reserved.			

Refer to the data sheet for the device requirements for maximum clock jitter, which must be accounted for in board design when selecting clock source (oscillator) and clock distribution (buffer) components. For details on using a single-ended reference clock, see *Section 14.3.1 Single-Ended RefClk Input* in the data sheet.

3.0 POWER/GROUND

3.1 Power Supplies

The VSC7423/8/9 requires power at:

- 1.0 V power supply voltage for core (**VDD**)
- 1.0 V power supply voltage for analog circuits (**VDD_A**)
- 1.0 V power supply voltage for analog circuits for twisted pair interface (**VDD_AL**)
- 2.5 V power supply voltage for analog driver in twisted pair interface (**VDD_AH**)
- 2.5 V power supply for MII Management interface, parallel CPU interface, and misc. I/Os (**VDD_IO**)

Note: The 2V5 IO supply must be within -1% to+4% to meet the minimum high-level input signal on 3V3 sourced devices, such as the JTAG and SPI.

- 1.8 V power supply for DDR interface (**VDD_IODDR**)
- 1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interfaces (**VDD_VS**)

Note: When doing a SerDes backplane, 1.2V is recommended. For SGMII and QSGMII between Switch and PHY located on the same board 1.0V is sufficient.

3.2 Power Supply Decoupling

- Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended bulk decoupling capacitors are 10 µF, but 47 µF should be used for **VDD_A** due to initial load during power-up. High-frequency decoupling capacitors that are 0.1 µF are also recommended.
- Surface mount decoupling capacitors should be placed as close to the power supply pins as possible. Smaller form factor components are best (that is, 0402 is better than 0603).
- Analog supplies are recommended to be isolated from the digital supplies using ferrite beads for better performance.

3.3 Ground

- Make at least one unbroken ground plane (**GND**).
- Use the power and ground plane combination as an effective power supply bypass capacitor. The capacitance is proportional to the area of the two planes and inversely proportional to the separation between the planes. Typical values with a 0.25 mm (0.01 inch) separation are 100 pF/in2. This capacitance is more effective than a capacitor of equivalent value because the planes have no inductance or Equivalent Series Resistance (ESR).
- Do not cut up the power or ground planes to steer current paths. This usually produces more noise, not less. Furthermore, place vias and clearances in a configuration that maintains the integrity of the plane. Groups of vias spaced close together often overlap clearances. This can form a large slot in the plane. As a result, return currents are forced around the slot, which increases the loop area and EMI emissions. Signals should never be placed on a ground plane because the resulting slot forces return currents around the slot.
- Vias connecting power planes to the supply and ground balls must be at least 0.25 mm (0.010 inch) in diameter, preferably with no thermal relief and plated closed with copper or solder. Use separate (or even multiple) vias for each supply and ground ball.
- A chassis ground is necessary for the RJ45 connector for better EMI and ESD.

3.4 Power Supply Sequencing

- During power-on and power-off, **VDD_A** and **VDD_VS** must never be more than 300 mV above **VDD**.
- **VDD_VS** must be powered even if the associated interfaces are not used.
- These power supplies must not remain at ground or be left floating.
- There is no sequencing requirements for **VDD_IO**.

4.0 INTERFACES

4.1 General Recommendations

High-speed signals require excellent frequency and phase response up to the third harmonic. The best designs provide excellent frequency and phase response up to the seventh harmonic. The following recommendations can improve signal quality and minimize transmission distances:

- Keep traces as short as possible. Initial component placement should be extremely carefully considered.
- The impedance of the traces must match the impedance of the termination resistors, connectors, and cable. This reduces reflections due to impedance mismatches.
- Differential impedance must be maintained in a 100Ω differential application. Routing two 50Ω traces is not adequate. The two traces must be separated by enough distance to maintain differential impedance. When routing differential pairs, keep the two trace lengths identical. Differences in trace lengths translate directly into signal skew. Note that the differential impedance may be affected when separations occur.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities. In other words, avoid using vias.
- Do not group all the passive components together. The pads of the components add capacitance to the traces. At the frequencies encountered, this can result in unwanted reductions in impedance. Use surface-mounted 0603 (or smaller) components to reduce this effect.
- Eliminate or reduce stub lengths.
- Reduce, if not eliminate, vias to minimize impedance discontinuities. Remember that vias and their clearance holes in the power/ground planes can cause impedance discontinuities in nearby signals. Keep vias away from other traces.
- Keep signal traces away from other signals that might capacitively couple noise into the signals. A good rule of thumb is to keep the traces apart by ten times the width of the trace.
- Do not route digital signals from other circuits across the area of the high-speed transmitter and receiver signals.
- Using grounded guard traces is typically not effective for improving signal quality. A ground plane is more effective. However, a common use of guard traces is to route them during the layout but remove them prior to design completion. This has the benefit of enforcing keep-out areas around sensitive high-speed signals, so that vias and other traces are not accidentally placed incorrectly.
- When signals in a differential pair are mismatched, the result is a Common-mode current. In a well-designed system, Common-mode currents should make up less than one percent of the total differential currents. Mode currents represent a primary source of EMI emissions. To reduce Common-mode currents, route differential traces so that their lengths are the same. For example, a 5-mm (0.2-inch) length mismatch between differential signals having the rise and fall times of 200 ps results in the Common-mode current being up to 18% of the differential current.

Note: Due to the high application frequency, proper care must be taken when choosing components (such as the termination resistors) in the designing of the layout of a printed circuit board. The use of surface-mount components is highly recommended to minimize parasitic inductance and lead length of the termination resistor.

- Matching the impedance of the PCB traces, connectors, and balanced interconnect media is also highly recommended. Impedance variations along the entire interconnect path must be minimized because these degrade the signal path and may cause reflections of the signal.

4.2 Serial CPU Interface

The Serial Interface (SI) bus consists of the SI_Clk clock signal, the SI_DO and SI_DI data signals, and the SI_nCS0 device select signal.

- When routing the SI_Clk signal, be sure to create clean edges. If the SI bus is connected to more than one client devices, route it in a daisy-chain configuration with no stubs. Terminate the SI_Clk signal properly to avoid reflections and double clocking.
- If it is not possible (or desirable) to route the bus in a daisy-chain configuration, the SI_Clk signal should be buffered and routed in a star topology from the buffers. Each buffered clock should be terminated at its source.
- The SI tri-states the SI_Clk and SI_DO signals prior to deasserting the SI_nCS0 signal. This makes it possible to implement CPOL/CPHA as 0/0 or 1/1, if the attached SI devices require it, using termination resistors. If the

attached devices support both types of CPOL/CPHA, SI_Clk and SI_DO must still have pull resistors to one of the I/O supply rails to prevent spurious clocks being seen when the signals are tri-stated.

- If the serial CPU interface is not used, all input signals can be left floating.

4.3 NOR Flash

NOR Flash is needed if booting from serial FLASH is enabled for the internal CPU. See *ENT-AN1263-4.5 - Application Note - Flash Configuration Design Guide - VPPD-04628* for Flash configurations.

- The VSC7423/8/9 is a 2.5V I/O device. VOH from this device might not meet requirement by the 3.3V NOR Flash at worst cases. A lower voltage supply (for example 2.8V) for the NOR Flash is recommended. Or using a buffer with voltage translation on the SPI interface between switch and the NOR Flash.

Note: During on-board Flash programming, hold the switch in Reset or change **VCORE_CFG[1:0]** away from '00'.

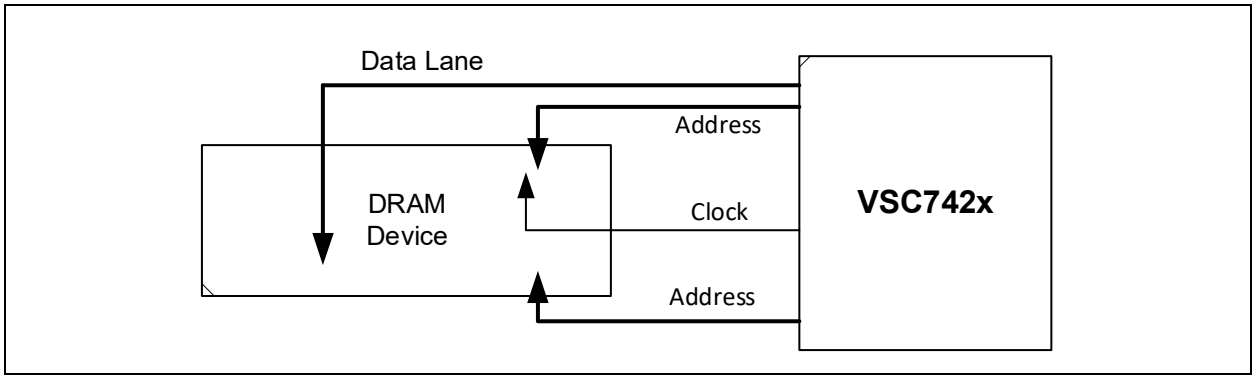
4.4 DDR2 SDRAM Interface

The DDR2 SDRAM interface is designed to interface directly with a single 8-bit DDR SDRAM device. The maximum supported density is 128 Mbyte (1 Gbps).

- All signals on this interface must be connected one-to-one with the corresponding signals on the DDR SDRAM device. If the memory size of the DDR SDRAM is smaller than maximum, then the upper part of the address and bank address signals can be left unconnected. All eight data bits must be used.

The placement of the VSC7423-02, VSC7428-02, and VSC7429-02 interface signals is optimized for point-to-point routing directly to a single DDR SDRAM device. See Figure 4-1.

FIGURE 4-1: DDR2 SDRAM POINT-TO-POINT ROUTING



- As reflections are absorbed by the driver, keep the physical distance of all the SDRAM interface signals below 1 ns to omit any external discrete termination on the address, command, control and clock lines. It is highly recommended to do simulation of the DDR interface.
- When routing the DDR2 interface, pay attention to the skew. The primary concern is the skew within the byte lane between the differential strobe and the single-ended signals. Skew recommendations for the DDR2 interface are listed in Table 4-1.

TABLE 4-1: RECOMMENDED SKEW BUDGET

Description	Signal	Maximum Skew
Skew within byte lane 0	DDR_DQS/DDR_DQSn	50 ps
Skew within address, command, and control bus	DDR_CK/DDR_CKn DDR_nRAS DDR_CKe DDR_ODT DDR_nCAS DDR_nWE DDR_BA[2:0] DDR_A[13:0]	100 ps

TABLE 4-1: RECOMMENDED SKEW BUDGET (CONTINUED)

Description	Signal	Maximum Skew
Skew within control bus clock and byte lane clock	DDR_CK/DDR_CKn DDR_DQS/DDR_DQSn	1250 ps
Control bus differential clock intrapair skew	DDR_CK/DDR_CKn	5 ps

- Use a shared voltage reference between the VSC7423-02, VSC7428-02, and VSC7429-02 device's DDR_Vref supply and the DDR device's reference voltage.
- Generate the DDR_Vref from the **VDD_IODDR** supply using a resistor divider with value of 1 kΩ and an accuracy of 1% or better.
- Use a decoupling capacitance of at least 0.1 µF on the supply in a manner similar to **VDD_IODDR** and **VSS** to ensure tracking of supply variations. However, the time constant of the resistor divider and decoupling capacitance should not exceed the nReset assertion time after power on.

Recommended routing:

- DDR_CK/DDR_CKn must be routed as a differential pair with a 100Ω differential characteristic impedance.
- DDR_DQS/DDR_DQSn must be routed as a differential pair with a 100Ω differential characteristic impedance.
- To minimize crosstalk, the characteristic impedance of the single-ended signals should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces.
- The crosstalk should be below -20 dB.

4.5 SGMII and QSGMII Interfaces

The SGMII interface (1 Gbps) consists of a **Tx** and **Rx** differential pair operating at 1250 Mbps using 10b8b encoding. The QSGMII interface operates at 5 Gbps due to its 10b8b encoding.

- **Tx** output signals in a pair should have matched electrical lengths.
- **Rx** input signals in a pair should have matched electrical lengths.
- SerDes **Tx** and **Rx** pairs must be routed as 100Ω differential traces with ground plane as reference. (All input buffers have built-in 100Ω terminations.)
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities. In other words, avoid the use of vias wherever possible.
- AC-coupling of **Tx** and **Rx** may be needed, depending on the PHY. If AC-coupled, the inputs are self-biased.
- To reduce the crosstalk between pairs or other PCB lines, it is recommended that the spacing on each side of the pair be larger than four times the track width.

4.6 SerDes and Enhanced SerDes Interfaces

The Enhanced SerDes interface can be used for fiber connections, backplanes, or direct coupler cable connections, such as the DAC cable. The Enhanced SerDes interface can operate in several modes. The physical signal bit rate is between 1.25 Gbps to 6.25 Gbps using 10b8b encoding with the default PCS layer in use.

- **100Base-FX support**: Besides supporting 1.25 Gbps, the 1G SerDes and Enhanced SerDes interfaces also support 100Base-FX (5b4b encoding). This is done by sampling the SerDes Rx at (normal) 1G speed and then digitally reconstructing the 5-bit symbols in a rate adaptation layer. Likewise, on TX side the 100M 5-bit encoded symbols are simply upscaled to the 1G SerDes speed, whereas the bit transitions are the same as with the 100M signal.
- The inputs are self-biased and have internal AC-coupling. In some modes, the interface requires external AC-coupling because of the input DC voltage limitation. If external AC-coupling capacitors are required, it is recommended to use small form factor components, such as 0603. The small form factor minimizes impedance mismatches by the AC-coupling capacitors because the size of the form factor approximately matches the trace width commonly used for these signals.
- If SFP MSA-defined signals such as TxFault, TxDisable, RxLos, ModuleDetect, and RateSelect are supported through the Serial GPIO interface then ensure that all signals have pull-ups. Likewise, an individual (selectable) I^2C clock should be routed to each module slot or cage.
- The Enhanced SerDes interface can be directly connected to either 1 Gbps or 2.5 Gbps SFP modules. For these applications, external AC-coupling capacitors are not required because the SFP module already includes capacitors.

Table 4-2 lists the AC-coupling requirements for common Enhanced SerDes connections.

TABLE 4-2: ENHANCED SERDES INTERFACE COUPLING REQUIREMENTS

Enhanced SerDes Connection	Mode	External AC-Coupling Requirement
SFP modules	SFP	Not required
SGMII PHY	SGMII	Required
Enhanced SerDes device	Enhanced SerDes	Required

- The Enhanced SerDes interface signals must be routed as a differential pair, with a 100Ω differential characteristic impedance. The differential intra-pair skew must be below 5 ps in the PCB trace.
- To minimize crosstalk between transmitter and receiver, equal drive strength is recommended in both devices in a link.
- To minimize crosstalk between differential pairs, the characteristic differential impedance of the signals must be determined only by the distance to the reference plane and the intra-pair coupling and not the distance to the neighboring traces. To separate the transmitter and receiver signals to minimize crosstalk, it is recommended to route the transmitter and receiver signals on as many different PCB layers as feasible.

4.7 Parallel Interface

This section applies when the parallel interface is enabled.

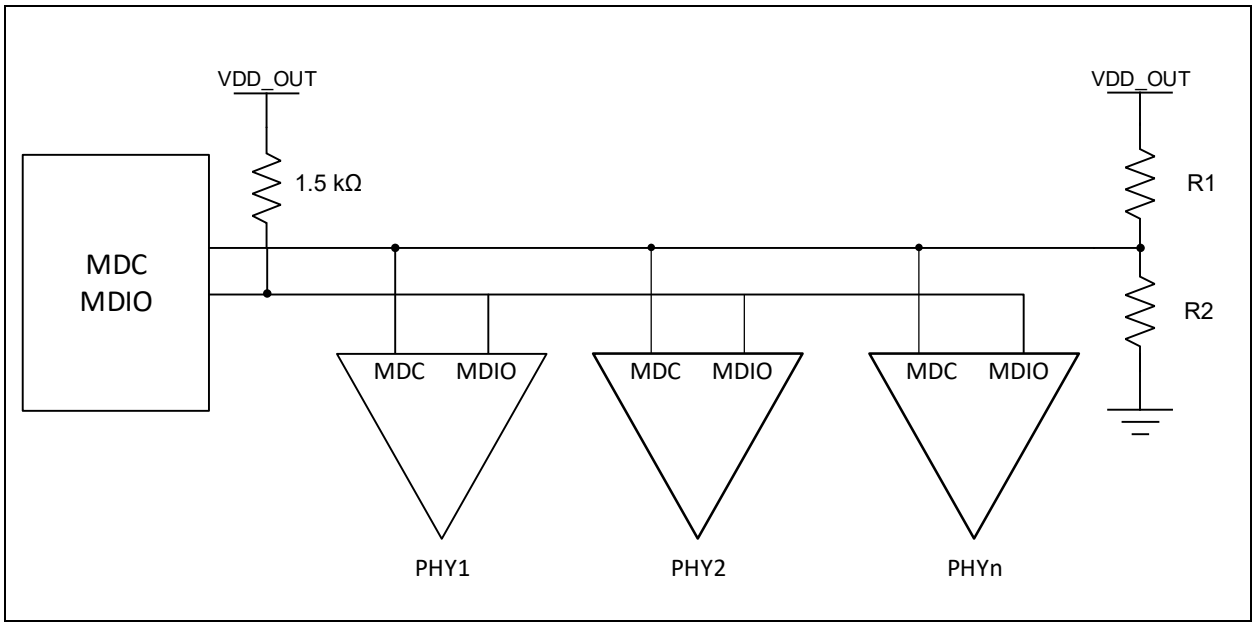
- The parallel interface (PI) consists of PI_Addr[3:0], PI_Data[7:0], PI_nCS, PI_nDone, PI_nOE, and PI_nWR. Leave these signals floating if the parallel interface is not used.
- When using the parallel interface, the timing parameter $t_{D(SLNH)}$ indicates when an issued command is sampled by the VSC7423-02, VSC7428-02, and VSC7429-02. For more information about the $t_{D(SLNH)}$ timing parameter, see *Table 861 PI Slave Mode Timing Specifications* in the data sheet.
- To ensure that the PI_nDone signal is driven inactive properly, add a 4.7 kΩ pull-up resistor to this signal, when used.

4.8 Media-Independent Interface Management (MIIM)

Also known as the Serial Management Interface (SMI), there are two MIIM controllers – one for internal PHYs and one for external PHYs. The external MIIM controller controls external PHYs via two pins, MDC (MIIM clock) and MDIO (MIIM data input/output).

- External PHYs are attached to the switch using SerDes ports. These PHYs are controlled via a single MIIM control bus. The MIIM controller uses PHY addresses to select one of the external PHYs, so the PHY addresses must be configured differently for all the external PHYs on the external MIIM bus.
- Due to MDIO is an open-drain output, MDIO should be pulled high with the resistor around 1.5 kΩ. When connecting MDC/MDIO to multiple PHYs, the layout scheme in Figure 4-2 with end termination is recommended.

FIGURE 4-2: CONNECTING THE EXTERNAL MDC/MDIO TO MULTIPLE PHYS



4.9 2-Wire Serial Interface

The 2-wire serial interface is capable of suppressing small amplitude glitches less than 5 ns in duration, which is less than the 50 ns duration often quoted for similar interfaces. Because the 2-wire serial implementation uses Schmitt-triggered inputs, the VSC7423-02, VSC7428-02, and VSC7429-02 devices have a greater tolerance to low amplitude noise.

- For glitch-free operation, select the proper pull-up resistor value to ensure that the transition time through the input switching region is less than 5 ns given the line's total capacitive load. For capacitive loads up to 40 pF, a pull-up resistor of 510Ω or less ensures glitch-free operation for noise levels up to 700 mV peak-to-peak.

5.0 MISCELLANEOUS SIGNALS

5.1 GPIO Pins

The devices include a GPIO interface with 32 individually configurable pins. Through the GPIOs, various interfaces are supported by the devices:

- 2-wire serial interface (two GPIO pins)
- 8-bit parallel interface (sixteen GPIO pins)
- UART (two GPIO pins)
- External interrupts (two interrupt pins)
- Serial GPIO (SGPIO) and LED interface (four GPIO pins)
- Fan controller with speed input and pulse-width-modulated output (two GPIO pins)
- Direct drive LEDs (two pins per internal PHY)
- IEEE 1588 pin with a programmable synchronized 1588 clock

For GPIO pin *N*, *N* = 1,2,3,…31:

GPIO_ALT[0][*N*] = 0, GPIO_ALT[1][*N*] = 0 → Normal GPIO mode

GPIO_ALT[0][*N*] = 1, GPIO_ALT[1][*N*] = 0 → Alternate mode 1

GPIO_ALT[0][*N*] = 0, GPIO_ALT[1][*N*] = 1 → Alternate mode 2

GPIO_ALT[0][*N*] = 1, GPIO_ALT[1][*N*] = 1 → Reserved

See the data sheet for the GPIO pin mapping for each variant in the VSC7423/8/9 family.

5.2 Serial GPIO Controller

The VSC7424-02, VSC7428-02, and VSC7429-02 devices feature a serial GPIO controller (SIO). By using a serial interface, the SIO controller significantly extends the number of available GPIOs with a minimum number of additional pins on the device. The main purpose of the SIO controller is to connect control signals from SFP modules. However, it can also act as an LED controller.

The SIO controller supports up to 128 serial GPIOs (SGPIOs) organized into 32 ports, with four SGPIOs per port. For more information, see *ENT-AN1015-1.0 - Application Note – Using the SparX-III Serial GPIO/LED Controller.*

5.3 System Resets

5.3.1 NRESET

This pin provides a global device Reset when low. On power-up, it is driven high when the clock and all power rails have stabilized. Refer to the data sheet for minimum required delays between clock and power rails and nReset going high.

Note that the internal 5 GHz PLL ramps up at power-up and is not controlled by any Reset signal. This allows all internal clocking to be running once HW Reset is released.

5.3.2 JTAG_NTRST

The JTAG_nTRST signal is asynchronous to the clock and does not have setup or hold time requirements. It must be held low until all power supply voltages have stabilized and reached recommended values. For normal device operations, i.e., when the JTAG interface is not in use, JTAG_nTRST should be pulled low.

Note:	All JTAG signals are **not** 5V tolerant.

5.4 Interrupt Pins

Two interrupt pins serve as inputs or outputs to the internal VCore-III CPU system or to an external processor. Signal polarity is programmable. These pins are EXT_IRQ[1:0] as GPIO_[8:9] using Overlaid Function One.

5.5 Coma Mode

The **COMA_MODE** pin provides an optional feature that may be used to control when PHY become active. It is an output for the Switch and an input to the PHYs. It is used to synchronize the operation of multiple PHYs (internal and external) on the same PCB.

- The typical usage is to keep the PHYs from becoming active before they have been fully initialized. Alternatively, the **COMA_MODE** pin may be connected low (ground) by a pull-down resistor and the PHYs will be fully active once out of Reset. When this pin is asserted high, all PHYs are held in a powered down state. When deasserted low, all PHYs are powered up and resume normal operation. This can be used to synchronize the operation of multiple PHYs on the same board to provide visual synchronization for LEDs by separate PHYs.

5.6 Reserved Pins

TABLE 5-1: VSC7423 PINS

Reserved Pins	Description
Reserved_1, Reserved_[7:8]	These reserved pins should be tied to V_{DD_IO}
Reserved_[4:6]	These reserved pins should be tied to V_{SS}
Reserved_[10:15], Reserved_[19:24] Reserved_[50:81], Reserved_[136:139] Reserved_[201:209], Reserved_[211:221] Reserved_[223], Reserved_[225] Reserved_[232:237], Reserved_[240:248]	These reserved pins should be left floating (no connect)

TABLE 5-2: VSC7428 PINS

Reserved Pins	Description
Reserved_1, Reserved_[5:6]	These reserved pins should be tied to V_{DD_IO}
Reserved_4, Reserved_[7:8]	These reserved pins should be tied to V_{SS}
Reserved_[10:15], Reserved_[19:24] Reserved_[50:81], Reserved_[136:139] Reserved_[201:209], Reserved_[211:221] Reserved_[223], Reserved_[225] Reserved_[232:237], Reserved_[240:248]	These reserved pins should be left floating (no connect)

TABLE 5-3: VSC7429 PINS

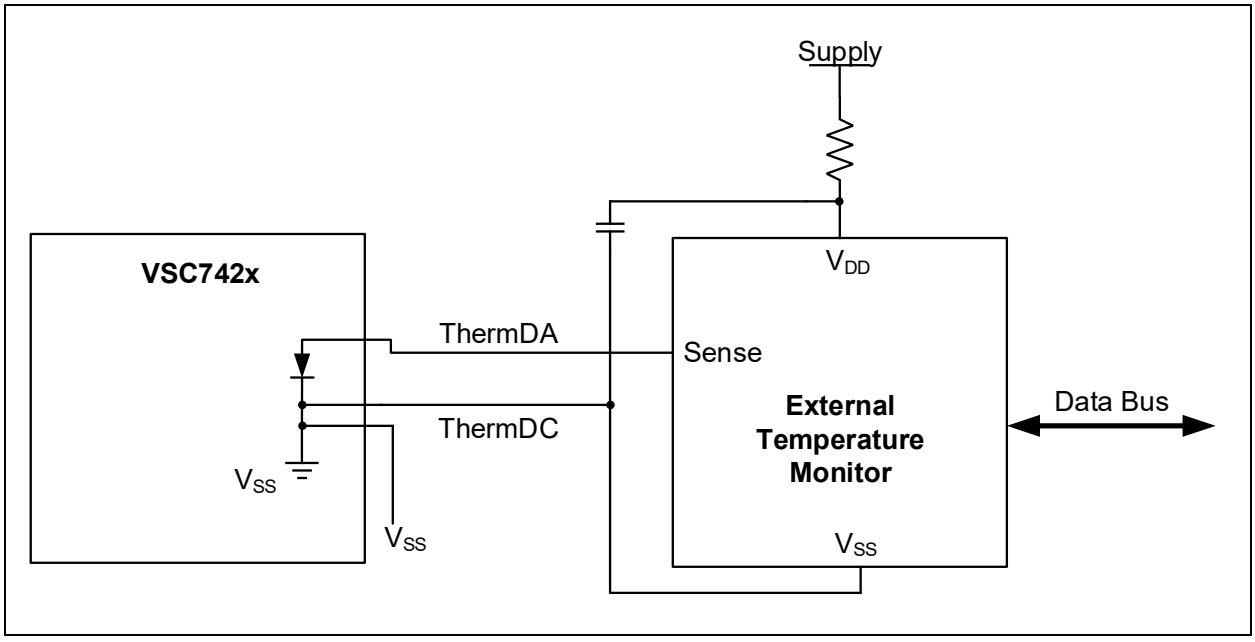
Reserved Pins	Description
Reserved_1, Reserved_6	These reserved pins should be tied to V_{DD_IO}
Reserved_4, Reserved_5, Reserved_[7:8]	These reserved pins should be tied to V_{SS}
Reserved_[10:15], Reserved_[19:24] Reserved_[201:209], Reserved_[211:221] Reserved_[223], Reserved_[225] Reserved_[232:237], Reserved_[240:248]	These reserved pins should be left floating (no connect)

5.7 Thermal Diode External Connection

The internal on-die thermal diode can be used with an external temperature monitor to easily and accurately measure the junction temperature of the VSC7423-02, VSC7428-02, and VSC7429-02 devices.

- The on-die thermal diode has an internal connection of the diode cathode to **VSS**, the external temperature sensor must support the thermal diode cathode connected to **VSS**.
- Thermal diode is extremely sensitive to noise. To minimize the temperature measurement errors, follow these guidelines:
  - Route the ThermDC and ThermDA signals as a differential pair with a differential impedance less than 100Ω.
  - Place the external temperature monitor as close as possible to the VSC7423-02, VSC7428-02,and VSC7429-02 devices.
  - Add a 47Ω resistor in series with the external temperature monitor supply to filter noise.
  - Place a de-coupling capacitor between the external temperature monitor supply pin and the ThermDC signal. Place the capacitor close to the external temperature sensor as shown in Figure 5-1.

FIGURE 5-1: EXTERNAL TEMPERATURE MONITOR CONNECTION



- Connect the external temperature monitor VSS pin directly to the ThermDC pin, which has the connection to **VSS**, as illustrated in Figure 5-1. Do not connect the external temperature monitor **VSS** pin to the global **VSS** plane.

5.8 Analog Bias Signals

Refer to the following information for the analog bias signals:

- **Analog Bias Calibration –** Connect SerDes_Rext1 and SerDes_Rext0 with a 620Ω ±1% resistor.
- **Reference Filters:** Ref_filt_[2:0] – Connect a 1.0 µF external capacitor between each pin and ground.
- **Reference External Resistors:** Ref_rext_[2:0] – Connect a 2.0 kΩ (1%) resistor between each pin and ground.
- Each [2:0] Reference capacitor and resistor should be joined before ground.

6.0 PORT CONFIGURATION

There are up to 26 internal ports for each device with an additional port assigned to the internal MIPS CPU. Both VSC7423 and VSC7428 have a single port configuration. The VSC7429 has three different port configurations, depending on the Switch mode (0,1, or 2).

Port assignments are fixed for each variant and mode in the family. See *Section 6.1 Port Mapping* in the data sheet to see the port mapping for your device.

7.0 INTERNAL COPPER PHY PORTS

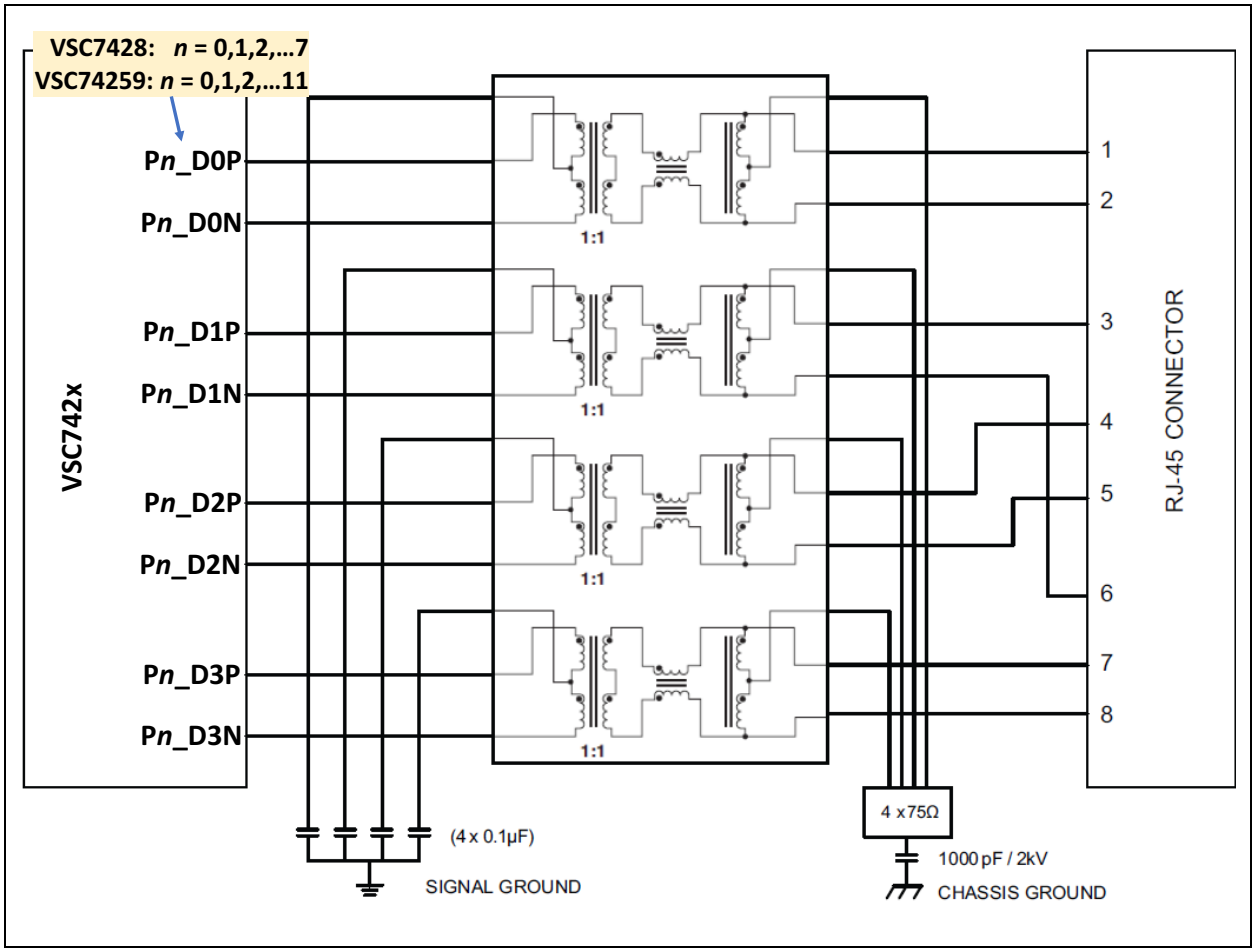
Five internal copper Gigabit (GbE) PHYs are available on the VSC7423. Eight internal copper Gigabit (GbE) PHYs are available on the VSC7428. Twelve internal copper Gigabit (GbE) PHYs are available on VSC7429. More external PHYs can be supported on the QSGMII interface or SGMII interfaces.

7.1 Copper PHY MDI Interface

Figure 7-1 shows the recommended connection from the internal copper PHY to the transformer. The internal copper PHY uses voltage-mode line driver technology, so no center tap voltage is required at the transformer. Each of the four center taps is recommended to be connected to GND through a separate 0.1 µF capacitor because the Common-mode voltage on each pair might be different.

Note:	The PHY has integrated termination resistors, so no external terminations are needed. It is recommended to use a minimum of 8-core magnetics with a Common-Mode-Choke (CMC) at the RJ45/cable side.

FIGURE 7-1: 12-CORE TRANSFORMER CONNECTIONS FOR INTERNAL COPPER PHY PORTS



The MDI interface is organized into four differential pairs (D0, D1, D2, and D3) for each PHY port. Pairs D2 and D3 are only used in Gigabit speed. When routing these pairs on a PCB, the characteristics must match one of the following:

- Route each single-ended trace with a characteristic impedance of 50Ω referenced to ground.
- Route each positive and negative trace on each port as differential pairs with 100Ω characteristic differential impedance.

8.0 HARDWARE CHECKLIST SUMMARY

TABLE 8-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet and retain the reference design's use of GPIO as much as possible to minimize software efforts.		
	Section 2.3, "Strapping Pins"	**VCORE_CFG[2:0]** configured to match design's Boot mode and endian.		
		VCORE_ICE_NEN should be low except during JTAG boundary scans.		
		A 25 MHz single-ended reference clock is not recommended when using QSGMII.		
		Single-ended reference clock design should follow *Section 14.2.1* in data sheet. Verify clock jitter will meet data sheet requirements.		
Section 3.0, "Power/ Ground"	Section 3.1, "Power Supplies"	The 2V5 IO supply must be within -1%/+4% to meet the minimum high level input signal on 3V3 sourced devices, such as JTAG and SPI.		
		When doing a SerDes backplane 1.2V is recommended. For SGMII and QSGMII between Switch and PHY located on the same board 1.0V is sufficient.		
	Section 3.2, "Power Supply Decoupling"	Each power rail should have bulk and high-frequency decoupling capacitors. High-frequency caps should be a close to the power pin as possible.		
		Analog supplies should be isolated from digital supplies through ferrite beads.		
	Section 3.3, "Ground"	Design in at least on unbroken ground plan. Other recommendations are followed.		
	Section 3.4, "Power Supply Sequencing"	Check the power sequencing if correct.		
Section 4.0, "Interfaces"	Section 4.1, "General Recommendations"	Recommendations to improve signal quality and minimize transmission distances are followed.		
	Section 4.2, "Serial CPU Interface"	If CPU interface is not used, pins can be left floating (no connect). Recommendations are followed.		
	Section 4.3, "NOR Flash"	Recommendations regarding buffering 3.3V NOR Flash to 2.5 V I/O are followed.		
	Section 4.4, "DDR2 SDRAM Interface"	Recommendations, including recommended skew budget, are followed.		

TABLE 8-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 4.0, "Interfaces"	Section 4.5, "SGMII and QSGMII Interfaces"	**Tx** and **Rx** differential pairs should have matched electrical cable lengths.		
		Pairs should be routed as 100Ω differential traces with ground plane as reference.		
		Check if PHY needs AC-coupling.		
		Spacing recommendations to reduce crosstalk are followed.		
	Section 4.6, "SerDes and Enhanced SerDes Interfaces"	Recommendations are followed.		
	Section 4.7, "Parallel Interface"	Recommendations are followed.		
	Section 4.8, "Media-Independent Interface Management (MIIM)"	Recommendations on MIIM bus interface with multiple external PHYs are followed.		
	Section 4.9, "2-Wire Serial Interface"	Recommendations are followed.		
Section 5.0, "Miscellaneous Signals"	Section 5.1, "GPIO Pins"	Use GPIO_ALT[1:0][31:1] to configure pin functions. Pins defaulting to GPIO should have GPIO_ALT[1:0][N] = 00b. In general, check for 2V5 level. All GPIO pins have internal pullup. Pins are 3.3V tolerant. All PHY LEDS are active-low and must have a resistor value of 100Ω to 300Ω in series. If LED unused it should left as NC.		
	Section 5.2, "Serial GPIO Controller"	Recommendations in the *ENT-AN1015-1.0 Application Note-Using the SparX-III Serial GPIO/LED Controller* are followed.		
	Section 5.3.1, "nReset"	Verify if **nReset** is held low until the clock and all power rails have stabilized. Follow timing specifications in the data sheet.		
	Section 5.3.2, "JTAG_nTRST"	No JTAG signals are 5 V tolerant. For normal operation, **JTAG_nTRST** should be pulled low.		
	Section 5.4, "Interrupt Pins"	Connect interrupt pins or GPIO pins configured as interrupt pins to supervisor. Depending on the polarity, remember pull resistors on interrupt signal.		
	Section 5.5, "Coma Mode"	Make sure that the use of pin is compatible with overall system design.		
	Section 5.6, "Reserved Pins"	Verify that pins are correctly terminated, either to **VDD_IO, VSS**, or are left floating.		
	Section 5.7, "Thermal Diode External Connection"	Recommendations are followed.		
	Section 5.8, "Analog Bias Signals"	Recommendations are followed.		
Section 6.0, "Port Configuration"		Port assignments vary by device. See Section 4.1, "General Recommendations" in the data sheet.		

TABLE 8-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Internal Copper PHY Ports"	Section 7.1, "Copper PHY MDI Interface"	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable.		
		Verify 10/100 BT mode of operation is supported on D0/D1.		
		Verify Auto-crossover only between A/B and C/D.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005272A (02-19-24)	Initial release	

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