AN 17.1

Power and Layout Considerations for EMC2105

1 Overview

This application note describes design and layout techniques that can be used to increase the performance and dissipate the power generated by the EMC2105. The EMC2105 device contains a fan driver which will cause internal power dissipation and heat generation. In addition, the high noise environment in which the EMC2105 is designed to operate may contribute unnecessary error to the temperature measurements.

2 Audience

This application note assumes that the reader is familiar with hardware design and the functionality of the EMC2105. The goal of the application note is to provide information on thermal management and noise immunity when using the EMC2105.

3 References

The following documents should be referenced when using this application note:

- SMSC EMC2105 Datasheet
- SMSC Application Note 10.14, “Using Temperature Sensing Diodes with EMC Devices - Remote Sensors” (AN10.14)
- SMSC Application Note 16.4, “Using Anti-Parallel Diode (APD) with SMSC Temperature Sensing Devices” (AN16.4)
- SMSC Application Note 18.15, “PCB Design Guidelines for QFN and DQFN Packages” (AN18.15)
- SMSC EMC2105 Reference Design
- AMKOR Application Note: “Application Notes for Surface Mount Assembly of Amkor’s *Micro*LeadFrame (MLF) Packages” (www.amkor.com)

4 Maintaining Accuracy of External Diode Connections

The EMC2105 includes an internal temperature sensor along with the ability to measure up to four external sensors. Temperature measurement is performed by measuring the change in forward bias voltage of a diode when different currents are forced through the junction. The circuit board itself can impact the ability to accurately measure these small changes in voltage. Therefore, to maintain the accuracy of the external temperature channels, apply the guidelines from the “Maintaining Accuracy” section of SMSC AN10.14. These include layout, device power supply decoupling, capacitor, cabling, manufacturing, and thermal recommendations for remote diodes.

4.1 Anti-Parallel Diode Support

The EMC2105 has Anti-Parallel Diode (APD) capability on several remote diode channels. This feature, illustrated in Figure 4.1 below, allows two 2N3904 type diodes to be measured on one pair of DP/DN pair. Routing and capacitor guidelines for APD applications are available in SMSC AN16.4.

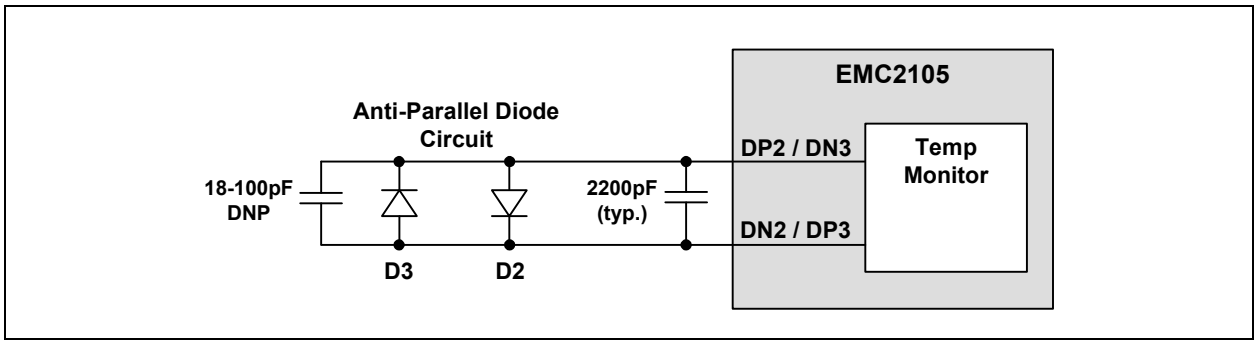


Figure 4.1 Anti-Parallel Diode Configuration

5 Power Considerations

The EMC2105 device contains a high side fan driver rated at 600mA maximum drive current. If the Fan Driver is fully loaded and driving at the maximum power dissipation, the EMC2105 can dissipate as much as 0.75W of on-chip power from the 5V supply.

The value of $Theta_{JA}$ for this package is approximately 60°C/W when soldered to a PCB without utilizing vias to conduct heat away from the die. The thermal resistance can be reduced to a much lower level with a sufficient quantity and diameter of vias connected to the ground plane.

When the guidelines in this section are followed, the EMC2105 is rated to operate up to an ambient temperature of 85°C and drive a fan rated up to 5V@600mA in all voltage/current settings.

5.1 Maximum Die Temperature

The maximum rated die temperature for the EMC2105's fabrication process is 125°C; however, SMSC recommends designing the thermal solution to maintain a die temperature below 110°C. This will provide thermal margin for different PCB configurations, via solder-fill variations and solder voids between the exposed pad and the thermal landing.

Note: The internal temperature sensor will report the average die temperature. This sensor will not report an accurate ambient temperature when the fan driver is dissipating power. The internal sensor may be measured to validate the thermal design. See Section 5.3, "Validating the Thermal Design".

5.2 Thermal Pad Design

The EMC2105's QFN package has an "exposed die paddle" which must be soldered to a thermal landing on the PCB. The thermal landing must be connected to the PCB ground plane with four 20mil vias, which results in a $Theta_{JA}$ value of approximately 40°C/W. The AMKOR application note provides details on manufacturability issues such as achieving solder-fill in the vias and minimizing voids due to gassing. SMSC AN18.15 also provides guidelines for using QFN packages.

Note: SMSC strongly recommends using 20mil vias to minimize die temperature. The larger vias are especially effective for applications with high power dissipation.

To help conserve routing resources, blind vias may be used to connect the QFN exposed die paddle to the ground plane. This makes it possible to route other signals under the QFN package on the

bottom layers of the PCB. If the vias are drilled completely through the PCB, the bottom side pad diameter may be the minimum allowed by the PCB manufacturing process.

5.3 Validating the Thermal Design

A simple test can be performed to validate the thermal solution. With no other active heat sources on the PCB, apply a load to the fan driver that results in 1W of power dissipation in the EMC2105. Apply power to this configuration for 1 hour to allow the temperatures to stabilize and then measure the ambient air temperature near the EMC2105 and the internal temperature sensor to determine the value of $Theta_{JA}$. The difference between the two temperatures is the thermal solution's $Theta_{JA}$ value.

Power dissipation of 1W can be achieved by applying the following conditions to the Fan Driver. Set the fan driver voltage to 3.0V (write value 0x99 to register 0x40) and connect a 6 ohm power resistor from the fan driver to ground.

Note: A power dissipation level of 1W is in excess of the normal operating conditions for this IC; however, it will not cause permanent damage to the EMC2105 as long the die temperature does not exceed the maximum rated die temperature of 125°C.

6 5V Linear Fan Driver

The EMC2105's high side fan driver circuit can provide up to 600mA of current from a 5V supply. The power dissipation of this circuit is dependent upon the current draw from the load as well as the output voltage where it is programmed. For linear drive systems, the on-chip power dissipation takes on a parabolic curve as shown in Figure 6.1.

This illustration assumes a constant load impedance. This is a simple mathematical example only and does not represent measured performance, nor does it include fan driver R_{ON}. Most linear fan drive systems have a non-linear load impedance that is proportional to the fan speed. In addition, there is a point in the curve where there is not enough energy to maintain the fan magnetic field or electronics and the fan will stop spinning, reducing the current load to zero. Consult the fan manufacturer for the voltage/current for the specific fan to be driven.

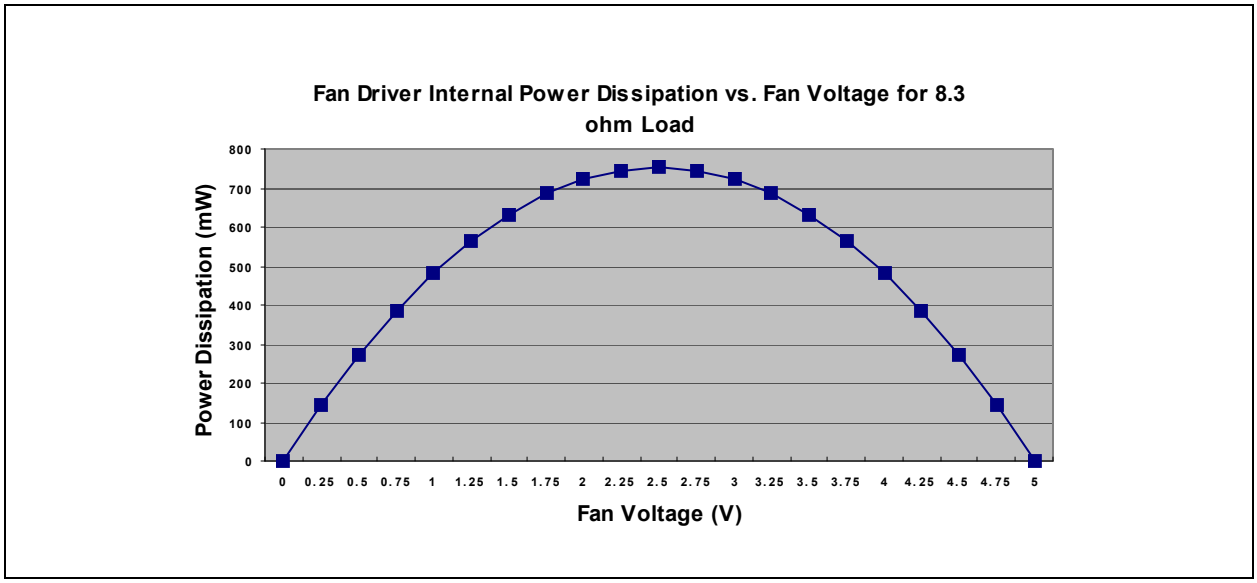


Figure 6.1 EMC2105 Fan Driver Power Example with Linear Load

6.1 Fan Driver Layout Considerations

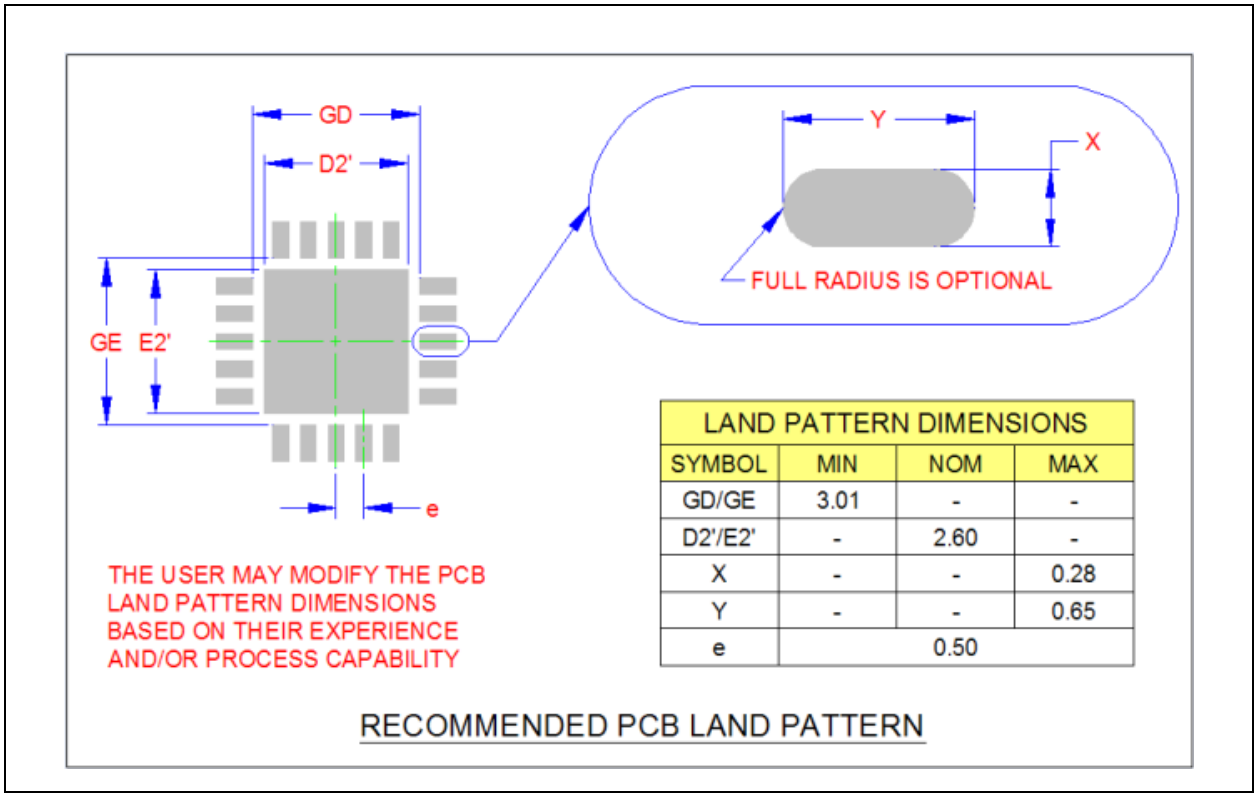
The VDD_5V and FAN_OUT pins may carry currents up to 600mA, so the cross-sectional area of the associated traces must be large enough to avoid voltage drop or excessive trace heating.

The high side fan driver should obey the following layout guidelines:

1. The 2 VDD_5V signals must be connected together.
2. The 2 FAN_OUT signals must be connected together.
3. The FAN_OUT signals should be loaded with a capacitor to ground. The value of this capacitor can vary from 10uF to 100uF. This capacitor should be placed as close to the load as possible.
4. The VDD_5V supply should be bypassed with at least a 10uF capacitor to ground and a 0.1uF capacitor to ground. These capacitors should be placed as close to the device as possible.
5. The FAN pin cannot sink more than 100uA of current; therefore, it should not be loaded with capacitors, resistors or inductors connected to VDD_5V or any supply higher than the programmed output voltage.

7 Other Layout Considerations

7.1 EMC2105 Recommended PCB Footprint



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	3.01	-	-
D2'/E2'	-	2.60	-
X	-	-	0.28
Y	-	-	0.65
e		0.50	

Figure 7.1 EMC2105 Recommended PCB Footprint Design for 20SQFN-4x4 Body

7.2 Solder Paste Stencil

A better solder joint can be achieved by applying solder paste with a stencil approximately 75% the size of the solder flag. Various shapes and sizes are used for the opening in the stencil, and an array of smaller openings is often cut into the solder paste template for QFN packages, as shown in Figure 7.2. For more details, refer to AMKOR - *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages*.

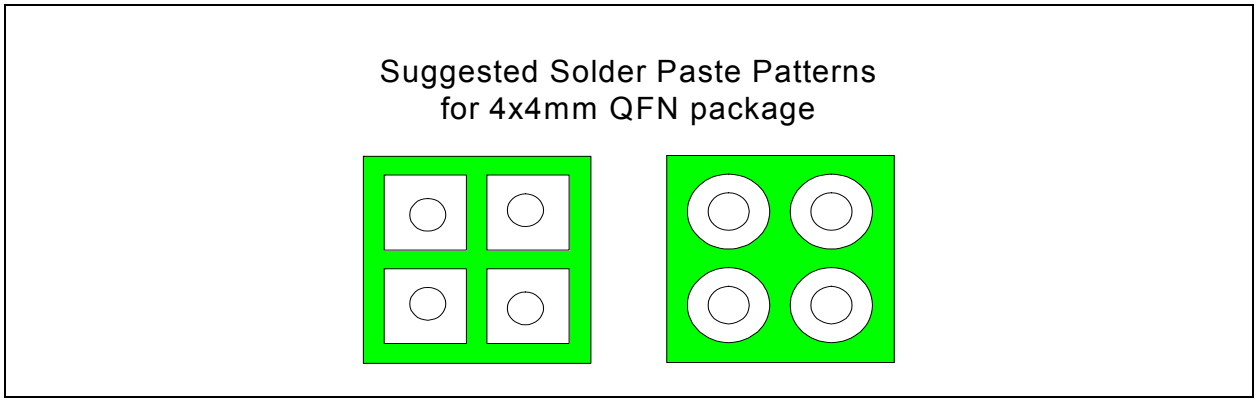


Figure 7.2 Suggested Solder Paste Stencil Patterns for Thermal Landing

Note: The green areas in the solder paste stencil patterns in Figure 7.2 indicate open PCB areas, while the white areas indicate solder paste.

7.3 General Purpose I/O Pins

The GPIO pins should obey the following layout guidelines:

1. The General Purpose I/O pins default as Inputs and should be terminated to some known state if they are not used. If this is not practical, then the BIOS should configure the not-connected pins as push-pull outputs.

7.4 General Notes

The remaining pins should obey the following layout guidelines:

1. The following pins are open drain and require a pull-up resistor:

- SMDATA
- SMCLK
- $\overline{\text{SYS\_SHDN}}$
- $\overline{\text{ALERT}}$

2. The following pin is a programmable I/O pin and will require pull-ups when used as an open drain output:

- CLK_IN/GPIO1

8 Application Note Revision History

Table 8.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 0.5 (02-23-11)	Document	This revision supersedes previous revisions.
	Section 3, "References"	Added references to the device reference designs, AN10.14, and AN18.15.
	Section 4, "Maintaining Accuracy of External Diode Connections"	Added ref to AN10.14 and removed the Layout section as updated information is covered in that updated AN.
Rev. 0.4 (10-04-07)	Initial Release	

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123