Color Space Conversion User Guide

Introduction (Ask a Question)

A color space is a mathematical representation of a set of colors. The most popular color models are listed as follow.

- RGB—Used in computer graphics
- YIQ, YUV, and YCbCr—Used in video compression

The red, green, and blue (RGB) color spaces are widely used in computer graphics. These are three primary additive colors and are represented by a three-dimensional, Cartesian coordinate system. These three colors are used to create any desired color. Therefore, the choice of the RGB color space simplifies the architecture and design of the system. Also, the system that is designed using the RGB color space takes advantage of a large number of existing software routines.

However, RGB is not very efficient in terms of bandwidth as all the three components have to be present in equal bandwidth to produce any color. So an RGB based frame buffer must have the same pixel depth and display resolution for each RGB component. Processing an image in RGB color space is usually not the most efficient method. For example, to modify the intensity or color of a given pixel, the three RGB values must be read from the frame buffer, the intensity or color calculated, desired modifications performed, new RGB values calculated, and written back into the frame buffer.

The same can be achieved if the image color properties are stored directly in intensity and color format.

Due to this reason, many video standards use luma and two color difference signals. One of the common color spaces in this format is the YCbCr color space format.

The YCbCr color space was developed as part of ITU-R VT.601 during the development of a worldwide digital component video standard. The luma component Y is defined to have a nominal 8-bit range of 16-235 range of values. The color information is represented as Cb and Cr with a nominal 8-bit range of 16-240 range of values. There are several YCbCr sampling formats such as 4:4:4, 4:2:2, 4:1:1, and 4:2:0.

Table 1. YCbCr Sample Formats

YCbCr Sample Format	Description
4:4:4	Each sample has a Y, a Cb, and a Cr value represented typically using 8-bits or 10-bits per component. Therefore, each sample in a 4:4:4 sampling format requires either 24-bits or 30-bits.
4:2:2	In the 4:2:2 sampling format, for every two horizontal Y samples, there is one Cb and Cr value. Each component sample is typically represented as 8-bits or 10-bits. Therefore, each sample in a 4:2:2 sampling format requires either 16-bits or 20-bits.
4:1:1	In the 4:1:1 sampling format, for every four horizontal Y samples, there is one Cb and Cr value. Each component sample is typically represented as 8-bits. Therefore, each sample in a 4:1:1 sampling format requires 12-bits.
4:2:0	In the 4:2:0 sampling format, the 2:1 reduction is done on both horizontal and vertical values. It is commonly used in video compression.

The advantages and disadvantages of various color space formats lead to requirements for color space conversions. The objective is to convert the video inputs into the desired color space before performing any video processing on it. The RGB to YCbCr and vice-versa conversion is one such example.

Summary (Ask a Question)

The following table provides a summary of the color space conversion IP characteristics.

Table 2. Summary

Core Version	This document applies to color space conversion IP.
Supported Device Families	PolarFire® SoC PolarFire RTG4™ IGLOO® 2 SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Licensing	Color space conversion IP clear RTL is license locked, and the encrypted RTL is available for free. Complete RTL code is provided for the core, allowing the core to be instantiated with the SmartDesign tool. Simulation, synthesis, and layout can be performed within Libero System-on-Chip (SoC). The RTL code for the core is encrypted.

Key Features (Ask a Question)

The key features of color space conversion IP are listed as follows:

- Supports RGBtoYCbCr444 and RGBtoYCbCr422 upsampling color space conversion also supports YCbCr444toRGB and YCbCr422toRGB downsampling color space conversion
- Supports 8, 10, 12, 14, and 16 data width
- Supports native and AXI4 stream video interface

Resource Utilizations (Ask a Question)

The color space conversion block is implemented on an M2S150T SmartFusion® 2 System-on-Chip (SoC) FPGA in the FC1152 package) and PolarFire FPGA (MPF300TS_ES - 1FCG1152E package).

The following table shows the Resource Utilization of RGB to YCbCr.

Table 3. Resource Utilization of RGBtoYCbCr in One Pixel Mode

Resource	YCbCr444	YCbCr422	AXI444	AXI422
Fabric DFF	54	72	80	90
Fabric 4LUTs	97	106	98	107
Math (18 ×18)	9	9	9	9
µSRAM	0	0	0	0
LSRAM	0	0	0	0

Table 4. Resource Utilization of RGBtoYCbCr in Four Pixel Mode

Resource	YCbCr444	YCbCr422	AXI444	AXI422
Fabric DFF	207	204	305	270
Fabric 4LUTs	388	258	389	259
Math (18 ×18)	36	24	36	24
µSRAM	0	0	0	0
LSRAM	0	0	0	0

The following table shows the Resource Utilization of YCbCr to RGB.

Table 5. Resource Utilization of YCbCrtoRGB in One Pixel Mode

Resource	YCbCr444	YCbCr422	AXI444	AXI422
Fabric DFF	88	90	114	116
Fabric 4LUTs	161	163	162	164
Math (18 ×18)	5	5	5	5
µSRAM	0	0	0	0
LSRAM	0	0	0	0

Table 6. Resource Utilization of YCbCrtoRGB in Four Pixel Mode

Resource	YCbCr444	YCbCr422	AXI444	AXI422
Fabric DFF	343	294	441	392
Fabric 4LUTs	644	592	645	593
Math (18 ×18)	20	12	20	12
µSRAM	0	0	0	0
LSRAM	0	0	0	0

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1. Hardware Implementation (Ask a Question)

This section describes the implementation of the color space conversion block.

1.1 Design Description (Ask a Question)

The color space conversion IP block contains two modules — RGB to YCbCr and YCbCr to RGB. The RGB to YCbCr color space converter IP module implements the equations to convert 24-bit input RGB color samples to 24-bit YCbCr output samples. The YCbCr to RGB color space converter IP module converts vice-versa of the RGB to YCbCr. Both the converters use a 4:4:4 sampling format.

Both the modules take data to enable inputs and pipeline them accordingly to match the conversion video data outputs.

To convert the floating-point constants into integer multiplication, the floating-point constants are scaled by multiplying these constants with 2^8 = 256. After the computation of the following equations, the output is divided by the scaling factor 2^{16} = 65536.

After scaling, the RGB to YCbCr equations are:

Y= 16 + 65.738*R/256 + 129.057*G/256 + 25.064*B/256

Cb = 128-37.945*R/256 - 74.494*G/256 + 112.439*B/256

Cr = 128+112.439*R - 94.154*G/256 - 18.285*B/256

After scaling, the YCbCr to RGB equations are:

R = 298.082*Y/256 + 408.583 * Cr/256 - 222.921

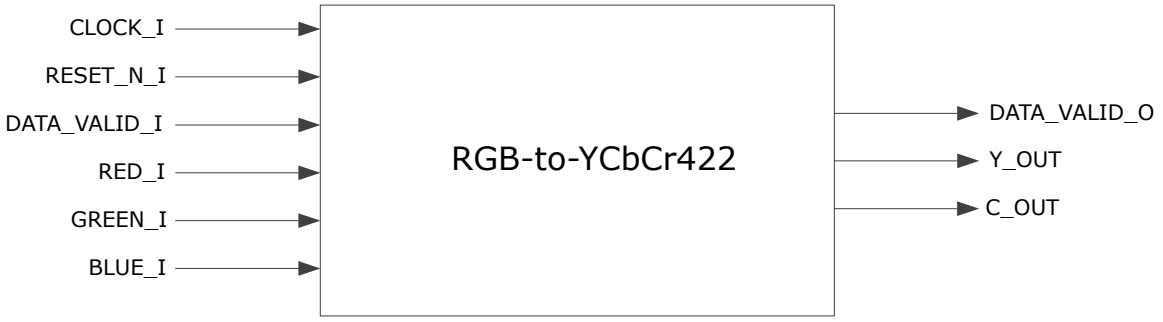
G = 298.082*Y/256 -100.291*Cb/256 - 208.120*Cr/256 + 135.576

B = 298.082*Y/256 + 516.412*Cb/256 - 276.836

The following figures show the system-level block diagrams of the RGB to YCbCr block.

Figure 1-1. System-Level Block Diagram of RGB to YCbCr444

Figure 1-2. System-Level Block Diagram of RGB to YCbCr422



The following figures show the system-level block diagrams of the YCbCr to RGB blocks.

Figure 1-3. System-Level Block Diagram of YCbCr444 to RGB

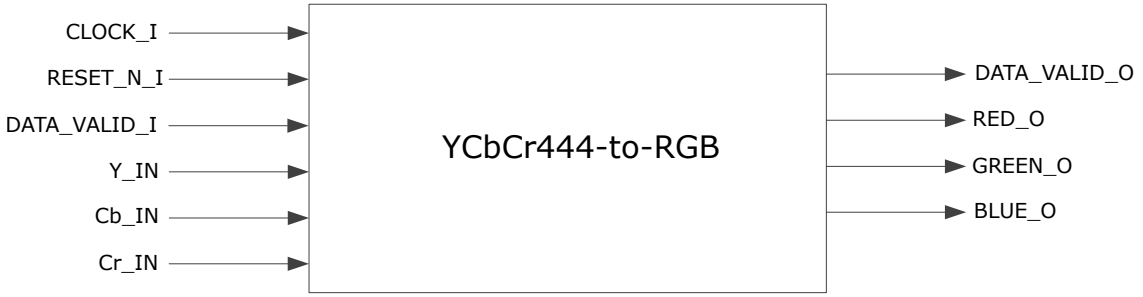
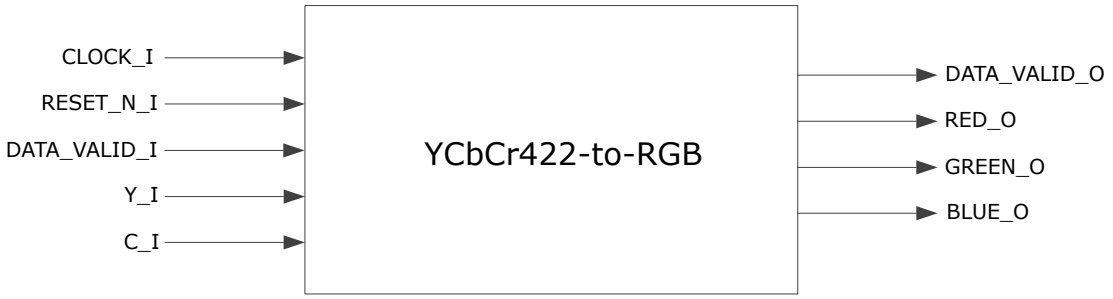


Figure 1-4. System-Level Block Diagram of YCbCr422toRGB



1.2 Inputs and Outputs (Ask a Question)

The following tables show the input and output ports of the RGB to YCbCr.

Table 1-1. Input and Output Ports of the RGB to YCbCr444 Block

Signal Name	Direction	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock

.....continued			
Signal Name	**Direction**	**Width**	**Description**
RED_I	Input	(Number of pixels * data width)	Red pixel data input
GREEN_I	Input	(Number of pixels * data width)	Green pixel data input
BLUE_I	Input	(Number of pixels * data width)	Blue pixel data input
DATA_VALID_I	Input	1-bit	Input data valid signal
Y_OUT_O	Output	(Number of pixels * data width)	Y pixel data output
Cb_OUT_O	Output	(Number of pixels * data width)	Cb pixel data output
Cr_OUT_O	Output	(Number of pixels * data width)	Cr pixel data output
DATA_VALID_O	Output	1-bit	Output data valid signal

Table 1-2. Input and Output Ports of the RGB to YCbCr422 Block

Signal Name	Direction	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
RED_I	Input	(Number of pixels * data width)	Red pixel data input
GREEN_I	Input	(Number of pixels * data width)	Green pixel data input
BLUE_I	Input	(Number of pixels * data width)	Blue pixel data input
DATA_VALID_I	Input	1-bit	Input data valid signal
Y_OUT	Output	(Number of pixels * data width)	Y pixel data output
C_OUT	Output	(Number of pixels * data width)	C pixel data output
DATA_VALID_O	Output	1-bit	Output data valid signal

The following tables shows the input and output ports of the YCbCr to RGB blocks.

Table 1-3. Input and Output Ports of the YCbCr444 to RGB Block

Signal Name	Direction	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
Y_IN	Input	(Number of pixels * data width)	Y pixel data input
Cb_IN	Input	(Number of pixels * data width)	Cb pixel data input
Cr_IN	Input	(Number of pixels * data width)	Cr pixel data input
DATA_VALID_I	Input	1-bit	Input data valid signal
RED_O	Output	(Number of pixels * data width)	Red pixel data output
GREEN_O	Output	(Number of pixels * data width)	Green pixel data output
BLUE_O	Output	(Number of pixels * data width)	Blue pixel data output
DATA_VALID_O	Output	1-bit	Output data valid signal

Table 1-4. Input and Output Ports of the YCbCr422 to RGB Block

Signal Name	Direction	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
Y_I	Input	(Number of pixels * data width)	Y pixel data input
C_I	Input	(Number of pixels * data width)	C pixel data input
DATA_VALID_I	Input	1-bit	Input data valid signal
RED_O	Output	(Number of pixels * data width)	Red pixel data output
GREEN_O	Output	(Number of pixels * data width)	Green pixel data output
BLUE_O	Output	(Number of pixels * data width)	Blue pixel data output
DATA_VALID_O	Output	1-bit	Output data valid signal

Table 1-5. Input and Output Ports for RGB to YCbCr444 AXI4 Stream Video Interface

Port Name	Type	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
TREADY_O	Output	1-bit	Output target ready
TDATA_I	Input	(3 * Number of pixels * data width)	Input Video Data
TVALID_I	Input	1-bit	Input Video Valid
TUSER_I	Input	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TDATA_O	Output	(Number of pixels * YCbCr Conversion Format * data width)	Output Video Data
TVALID_O	Output	1-bit	Output Video Valid
TUSER_O	Output	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TLAST_O	Output	1-bit	Output Video End of Frame
TSTRB_O	Output	(Number of pixels * data width)/8	Output Video Data strobe
TKEEP_O	Output	(Number of pixels * data width)/8	Output Video Data Keep

Table 1-6. Input and Output Ports for YCbCr444 to RGB AXI4 Stream Video Interface

Port Name	Type	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
TREADY_O	Output	1-bit	Output target ready
TDATA_I	Input	(Number of pixels * YCbCr Conversion Format * data width)	Input Video Data
TVALID_I	Input	1-bit	Input Video Valid
TUSER_I	Input	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TDATA_O	Output	(3 * Number of pixels * data width)	Output Video Data
TVALID_O	Output	1-bit	Output Video Valid
TUSER_O	Output	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TLAST_O	Output	1-bit	Output Video End of Frame
TSTRB_O	Output	(Number of pixels * data width)/8	Output Video Data strobe
TKEEP_O	Output	(Number of pixels * data width)/8	Output Video Data Keep

Table 1-7. Input and Output Ports for RGB to YCbCr422 AXI4 Stream Video Interface

Port Name	Type	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
TREADY_O	Output	1-bit	Output target ready
TDATA_I	Input	(3 * Number of pixels * data width)	Input Video Data

.....continued			
Port Name	**Type**	**Width**	**Description**
TVALID_I	Input	1-bit	Input Video Valid
TUSER_I	Input	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TDATA_O	Output	(Number of pixels * YCbCr Conversion Format * data width)	Output Video Data
TVALID_O	Output	1-bit	Output Video Valid
TUSER_O	Output	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TLAST_O	Output	1-bit	Output Video End of Frame
TSTRB_O	Output	(Number of pixels * data width)/8	Output Video Data strobe
TKEEP_O	Output	(Number of pixels * data width)/8	Output Video Data Keep

Table 1-8. Input and Output Ports for YCbCr422 to RGB AXI4 Stream Video Interface

Port Name	Type	Width	Description
RESET_N_I	Input	1-bit	Active low asynchronous reset signal to design
CLOCK_I	Input	1-bit	System clock
TREADY_O	Output	1-bit	Output target ready
TDATA_I	Input	(Number of pixels * YCbCr Conversion Format * data width)	Input Video Data
TVALID_I	Input	1-bit	Input Video Valid
TUSER_I	Input	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TDATA_O	Output	(3 * Number of pixels * data width)	Output Video Data
TVALID_O	Output	1 bit	Output Video Valid
TUSER_O	Output	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TLAST_O	Output	1-bit	Output Video End of Frame
TSTRB_O	Output	(Number of pixels * data width)/8	Output Video Data strobe
TKEEP_O	Output	(Number of pixels * data width)/8	Output Video Data Keep

1.3 Configuration Parameters (Ask a Question)

The following table shows the configuration parameters used in the hardware implementation of RGB to YCbCr and YCbCr to RGB blocks. These are generic parameters and can be varied as per the application requirements.

Table 1-9. Configuration Parameters

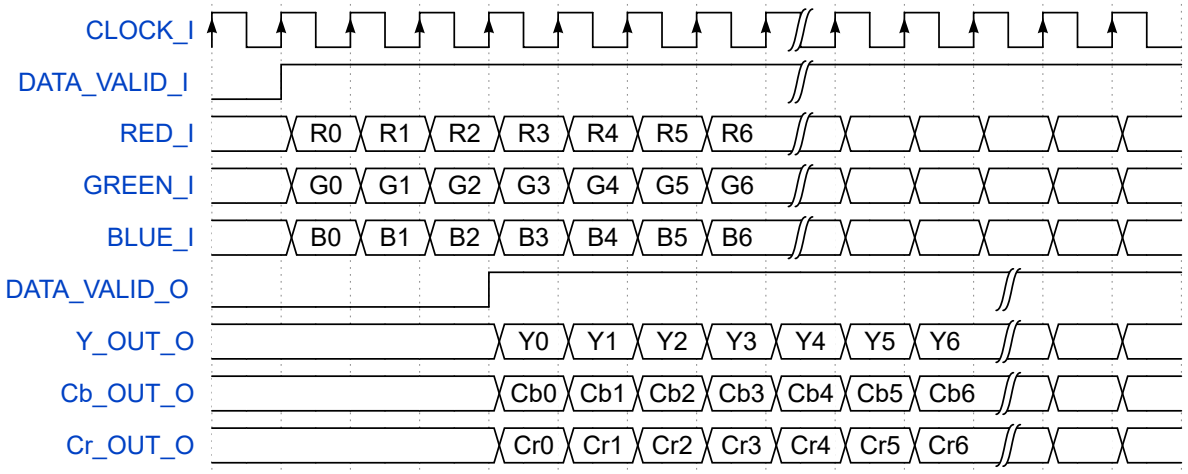
Name	Description
Data width	Width of each pixel (supports 8, 10, 12, 14, and 16)
Number of Pixels	Number of pixels per clock is 1 or 4
YCbCr Conversion Format	YCbCr444 and YCbCr422

.....continued	
Name	**Description**
Video Interface	Native and AXI4 Stream

2. Timing Diagrams (Ask a Question)

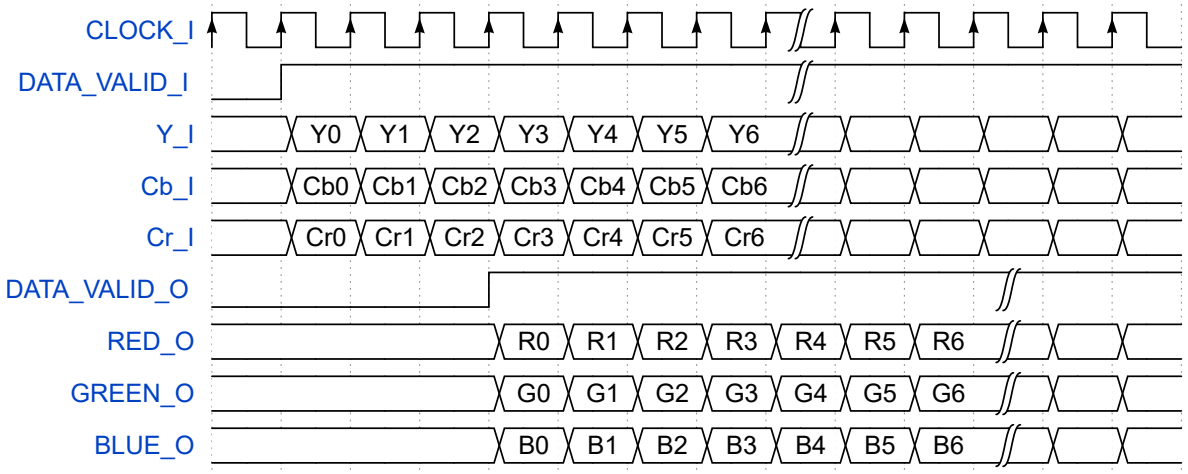
The following figure shows the timing diagrams of RGB to YCbCr444.

Figure 2-1. Timing Diagram of RGB to YCbCr444



The following figure shows the timing diagrams of YCbCr444 to RGB blocks.

Figure 2-2. Timing Diagram of YCbCr444 to RGB



Important: All other input signals get delayed by the clock cycles, as shown in the preceding figure.

3. Testbench (Ask a Question)

A testbench is provided to check the functionality of the color space converter core.

The testbench uses the following default parameters. The parameters of the testbench must match the configuration settings of the IP.

Parameter **G_DATA_BIT_WIDTH** = 8

Parameter **G_YCbCr_FORMAT** = 3; // 3 for YCbCr format 444 and 2 for YCbCr format 422

Parameter **G_PIXELS** = 1

Parameter **G_FORMAT** = 0; // 0 for Native mode and 1 for AXI4 Streaming

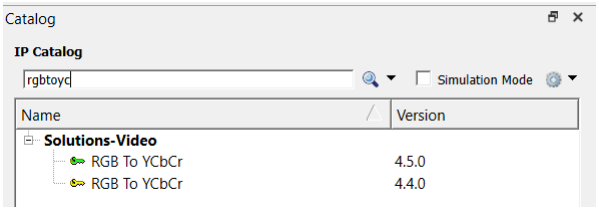
3.1 Simulation Rows (Ask a Question)

To simulate the core using the testbench, perform the following steps:

1. Open the Libero SoC application, click on **Libero SoC catalog** tab, and then search for **RGBtoYCbCr**, The documentation associated with the IP are listed under documentation section. See the following figure.

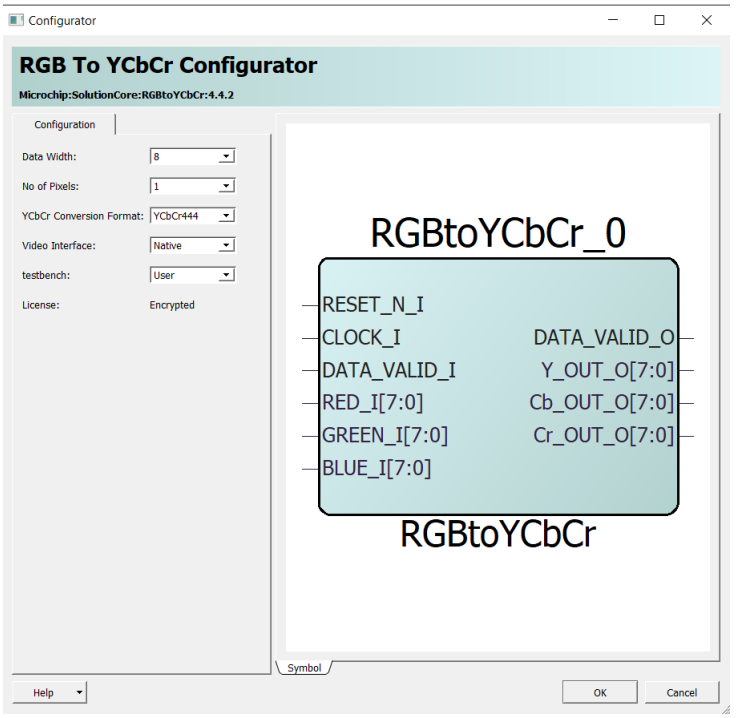
Important: If you do not see the catalog tab, navigate to **View** > **windows menu** and click **catalog** to make it visible.

Figure 3-1. RGBtoYCbCr IP Core in Libero SoC Catalog



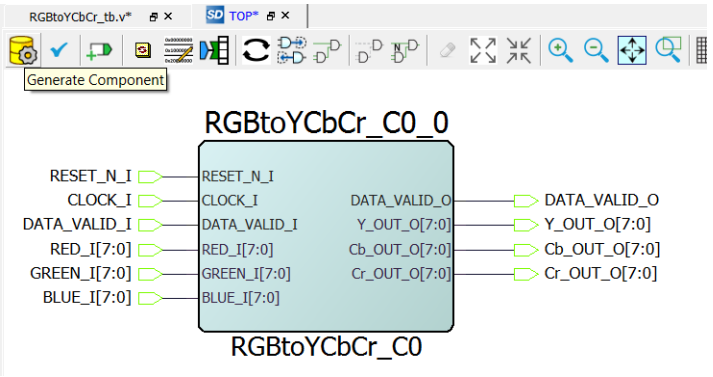
2. Double click on **RGBtoYCbCr**. Configure the core IP as per requirement. Click **OK**

Figure 3-2. RGBtoYCbCr Configurator



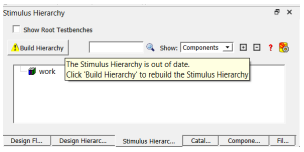
3. Promote all the signals to top-level and generate the component. See the following figure.

Figure 3-3. Generate Component



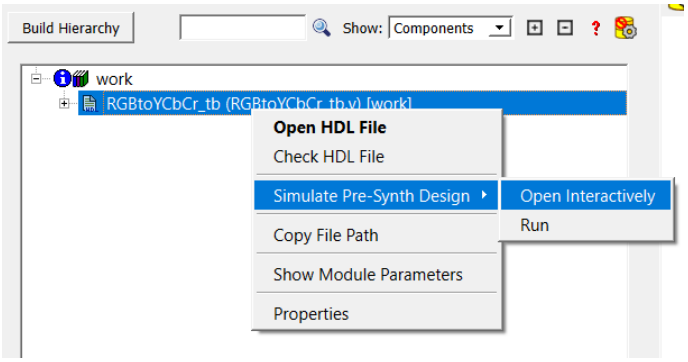
4. Go to **Stimulus Hierarchy** tab, click **Build Hierarchy**.

Figure 3-4. Simulating Pre-synth Design



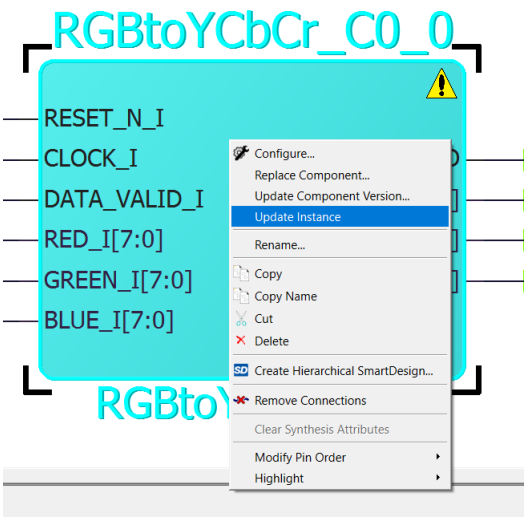
5. Right-click on `RGBtoYCbCr_tb` and then click on **Simulate Pre-synth Design** > **Open Interactively**. See the following figure.

Figure 3-5. Stimulus Hierarchy



6. To change the Configuration of the core IP, double click on IP and change the configuration parameters as per requirement and in the testbench. Update the Instance by right-click on IP and select **Update Instance**, generate the design.

Figure 3-6. Update Instance



If the simulation is interrupted because of the runtime limit in the DO file, use the `run -all` command to complete the simulation. After the simulation is completed, the testbench output image file appears in the simulation folder (**View** > **Files** > **Simulation**).

Testbench Results with Parameters

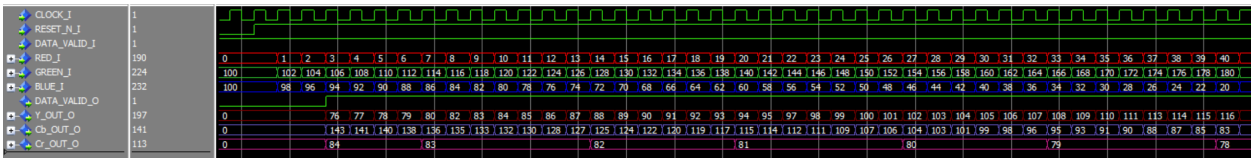
The following figures show the testbench results for RGBtoYCbCr and YCbCrtoRGB conversion.

One Pixel Mode

Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 3; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 1
- Parameter G_FORMAT = 0; // 0 for Native mode and 1 for AXI4 Streaming

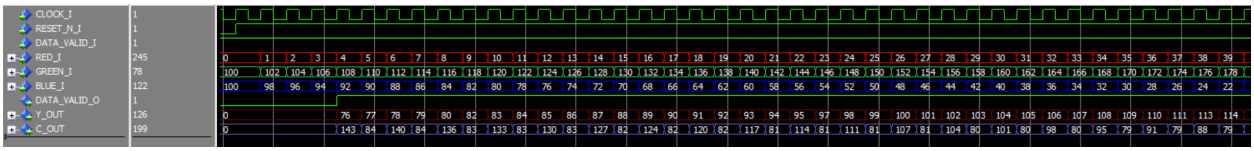
Figure 3-7. Simulation Waveform for RGB to YCbCr444



Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 2; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 1
- Parameter G_FORMAT = 0; // 0 for Native mode and 1 for AXI4 Streaming

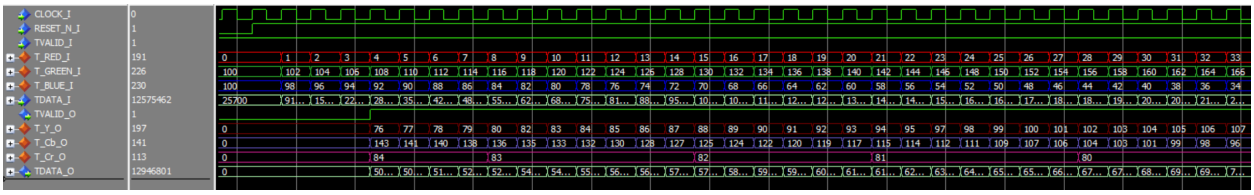
Figure 3-8. Simulation Waveform for RGB to YCbCr422



Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 3; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 1
- Parameter G_FORMAT = 1; // 0 for Native mode and 1 for AXI4 Streaming

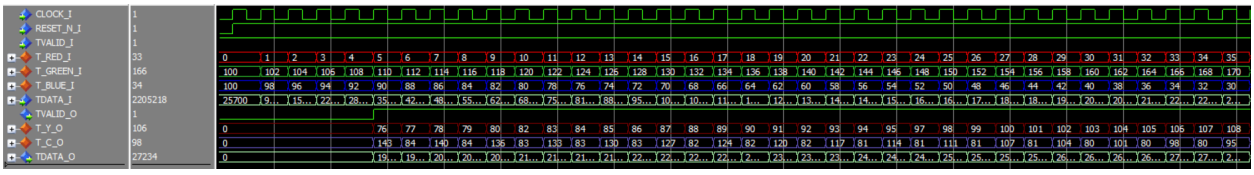
Figure 3-9. Simulation Waveform for RGB to YCbCr444 using AXI Stream Interface



Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 2; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 1
- Parameter G_FORMAT = 1; // 0 for Native mode and 1 for AXI4 Streaming

Figure 3-10. Simulation Waveform for RGB to YCbCr422 using AXI Stream Interface



Important: The parameters for YCbCrtoRGB is similar to RGBtoYCbCr in different modes.

Figure 3-11. Simulation Waveform for YCbCr444 to RGB

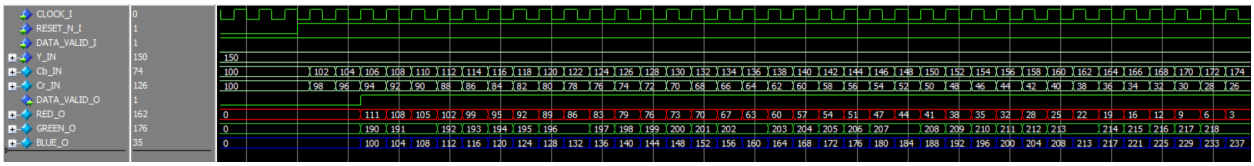


Figure 3-12. Simulation Waveform for YCbCr422 to RGB

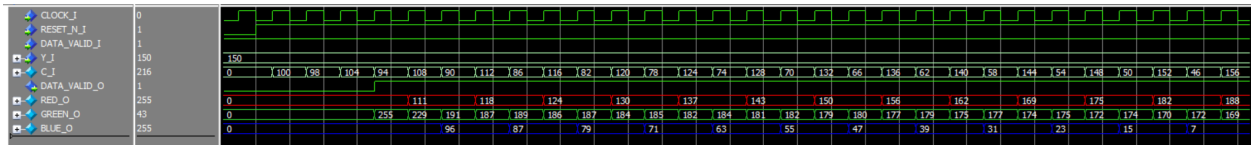


Figure 3-13. Simulation Waveform for YCbCr444 to RGB using AXI Stream Interface

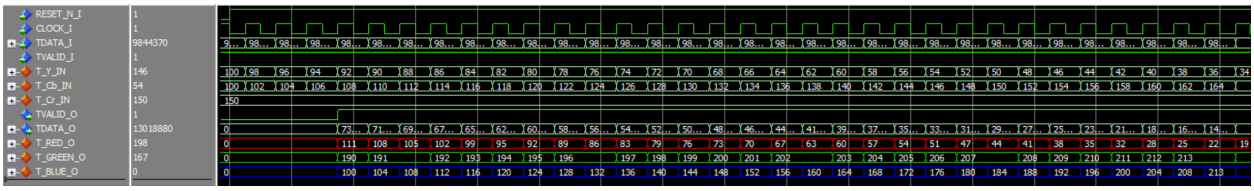
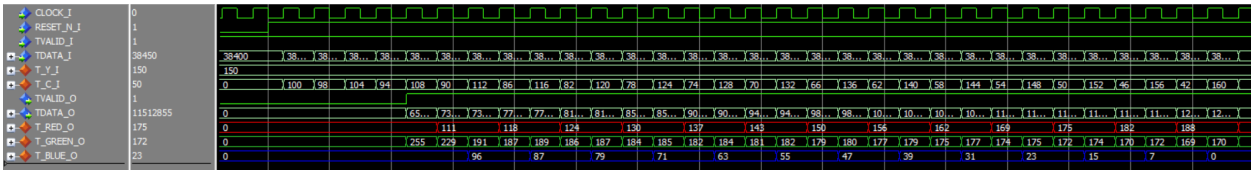


Figure 3-14. Simulation Waveform for YCbCr422 to RGB using AXI Stream Interface

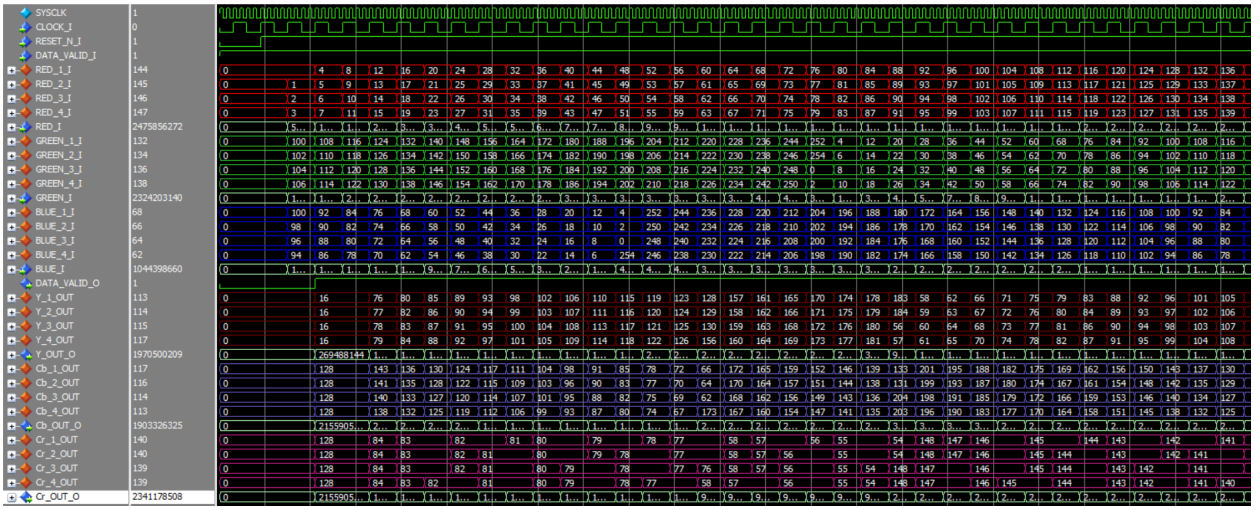


Four Pixel Mode

Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 3; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 4
- Parameter G_FORMAT = 0; // 0 for Native mode and 1 for AXI4 Streaming

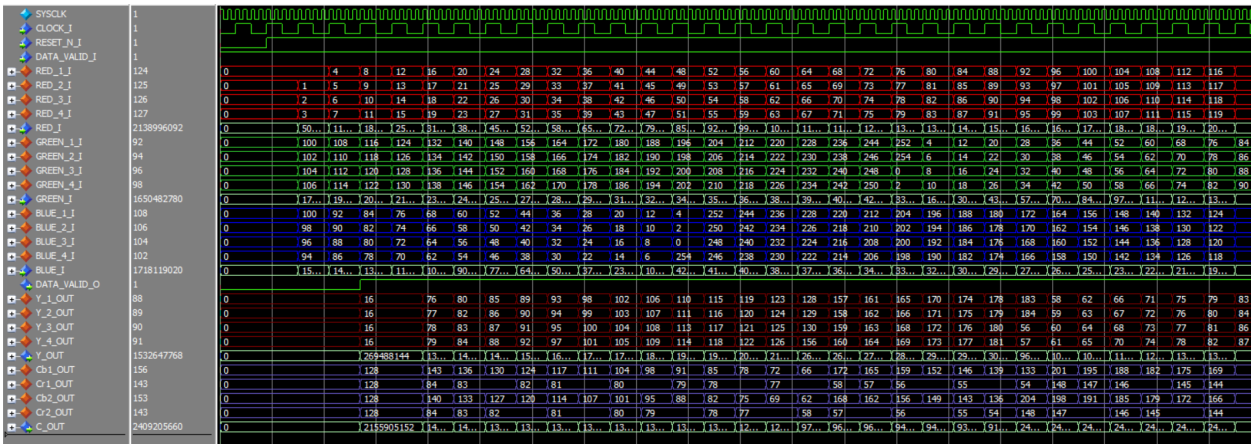
Figure 3-15. Simulation Waveform for RGB YCbCr444



Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 2; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 4
- Parameter G_FORMAT = 0; // 0 for Native mode and 1 for AXI4 Streaming

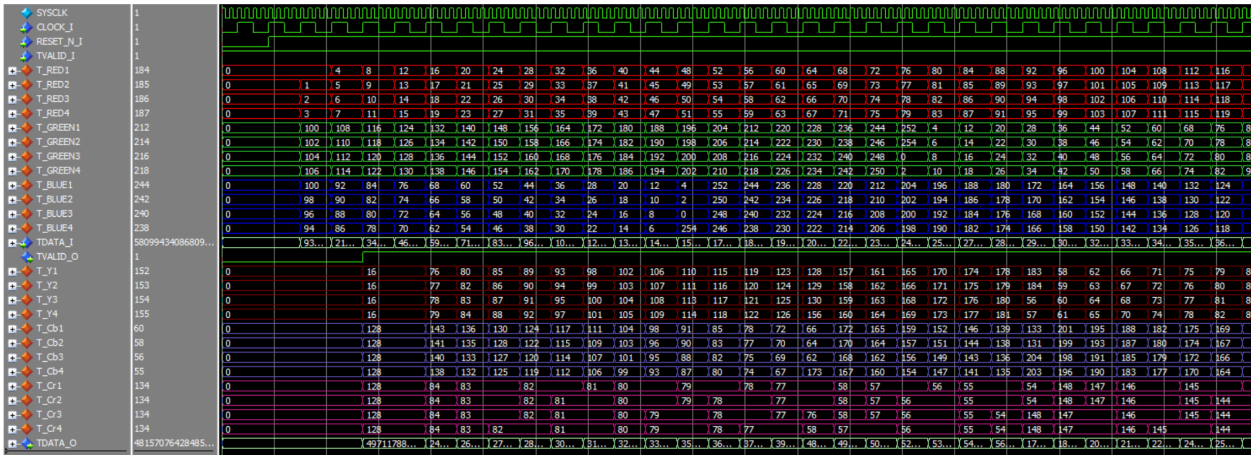
Figure 3-16. Simulation Waveform for RGB YCbCr422



Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 3; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 4
- Parameter G_FORMAT = 1; // 0 for Native mode and 1 for AXI4 Streaming

Figure 3-17. Simulation Waveform for RGB to YCbCr444 using AXI Stream Interface



Parameters need to be changed in testbench as follows:

- Parameter G_DATA_BIT_WIDTH = 8
- Parameter G_YCbCr_FORMAT = 2; // 3 for YCbCr format 444 and 2 for YCbCr format 422
- Parameter G_PIXELS = 4
- Parameter G_FORMAT = 1; // 0 for Native mode and 1 for AXI4 Streaming

Figure 3-18. Simulation Waveform for RGB to YCbCr422 using AXI Stream Interface

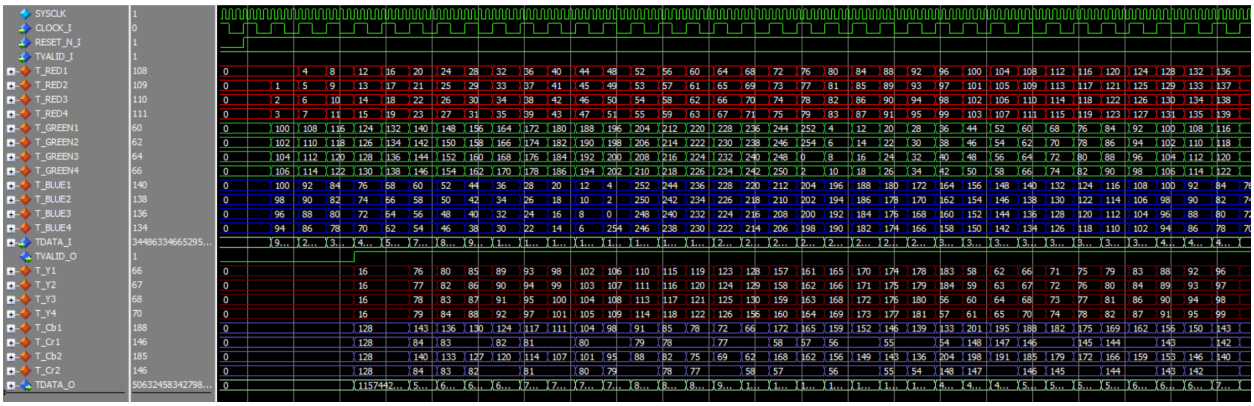


Figure 3-19. Simulation Waveform for YCbCr444 to RGB

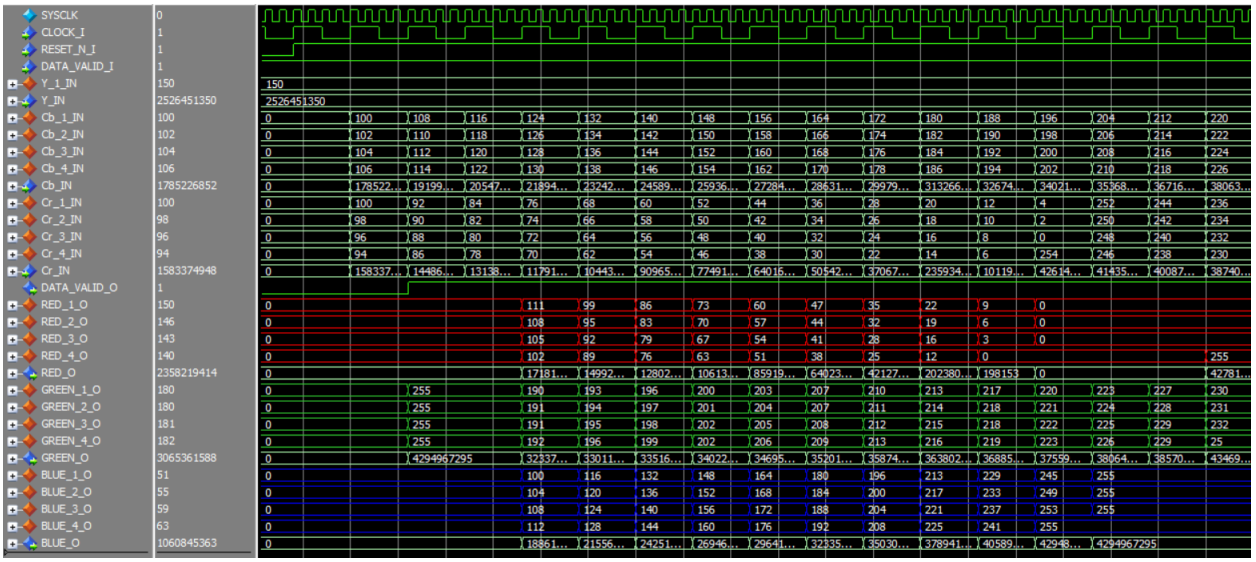


Figure 3-20. Simulation Waveform for YCbCr422 to RGB

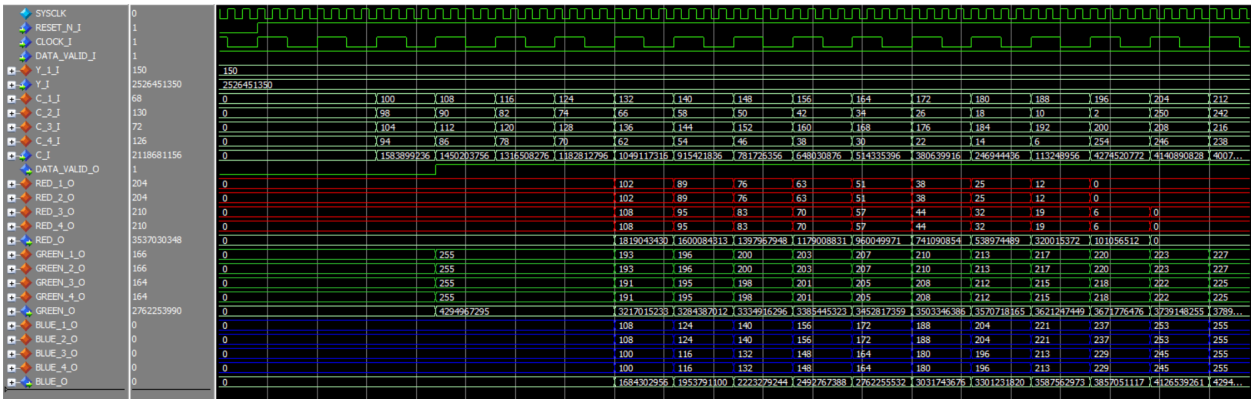


Figure 3-21. Simulation Waveform for YCbCr444 to RGB with AXI Stream Interface

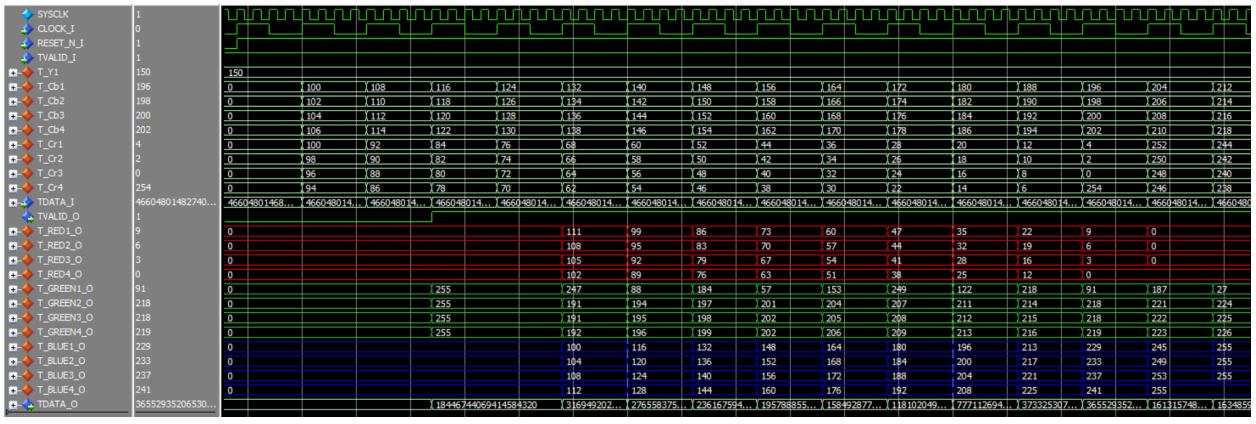
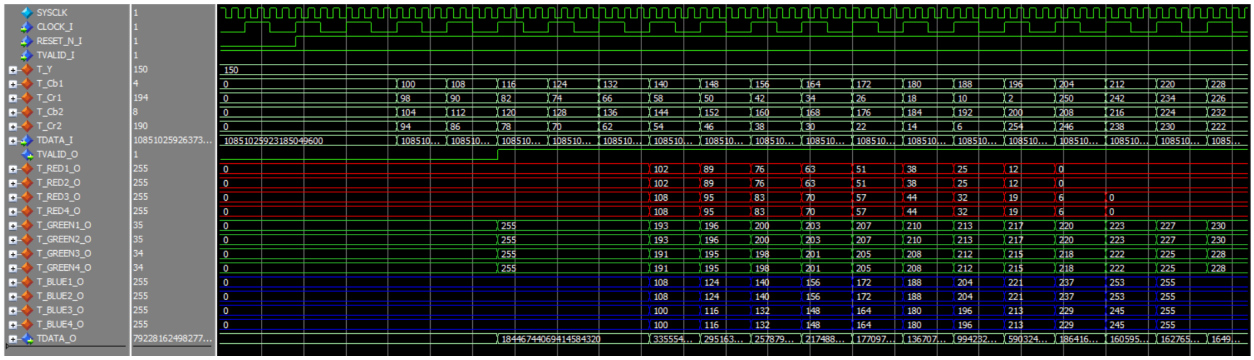


Figure 3-22. Simulation Waveform for YCbCr422 to RGB with AXI Stream Interface



4. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 4-1. Revision History

Revision	Date	Description
A	07/2023	The following is the list of changes in revision A of the document: • Migrated the document to the Microchip template. • Updated for 4 pixel mode throughout the document.
5.0	—	The following is a summary of the changes in this revision. • Updated Figure 1-1 and Figure 1-3. • Updated Table 1-9 and Table 4. • Added figures to show system-level block diagram. See Figure 1-2 and Figure 1-4. • Added figure to show testbench results. • Added table for input and output ports of the RGB to YCbCr422 block. See Table 1-2. • Resource Utilization tables were added. See Table 3 and Table 5.
4.0	—	The following is a summary of the changes in this revision. • IOs and equations were updated. • Updated Figure 1-1 and Figure 1-3. • Input and Output Port were updated. See Table 1-1 and Table 1-3. • Added figure to show Testbench results. • Resource Utilization values were updated. See Resource Utilizations.
3.0	—	Updated the Resource Utilization section and the Resource Utilization Report. See Resource Utilizations.
2.0	—	The following is a summary of the changes in this revision. • The Testbench section was added to the document as per SAR 76100. For more information, see 3. Testbench. • Resource Utilization values were updated as per SAR 76100. For more information, see Resource Utilizations.
1.0	—	The first publication of this document.

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