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DOCUMENT DESCRIPTION
Component Placement Checklist for the LAN9220, 56-pin QFN Package

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Component Placement Checklist for LAN9220

Information Particular for the 56-pin QFN Package

LAN9220 QFN Phy Interface:

1. If the Auto MDIX functionality is enabled, place the $49.9\ \Omega$ TX termination pull-up (TPO+, pin 45) as close to the LAN9220 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
2. If the Auto MDIX functionality is enabled, place the $49.9\ \Omega$ TX termination pull-up (TPO-, pin 44) as close to the LAN9220 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
3. Place the $49.9\ \Omega$ RX termination pull-up (TPI+, pin 48) as close to the LAN9220 as possible.
4. Place the $49.9\ \Omega$ RX termination pull-up (TPI-, pin 47) as close to the LAN9220 as possible.

LAN9220 QFN Magnetics:

1. Place the $10.0\ \Omega$ TX/RX Channel Center Tap feed resistor as close to the magnetics as possible.
2. Place the $0.022\ \mu\text{F}$ TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.
3. Place the $75\ \Omega$ cable side center tap termination resistors and the $1000\ \text{pF}$, 2KV capacitor (C_{magterm}) cap as close to the magnetics as possible.

RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN9220 QFN as close together as possible.
2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN9220 QFN.
3. Select and place the magnetics as to set up the best routing scheme from the LAN9220 QFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.
4. Place the Unused Wire Pair termination resistors and the 1000 μ F, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.
5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

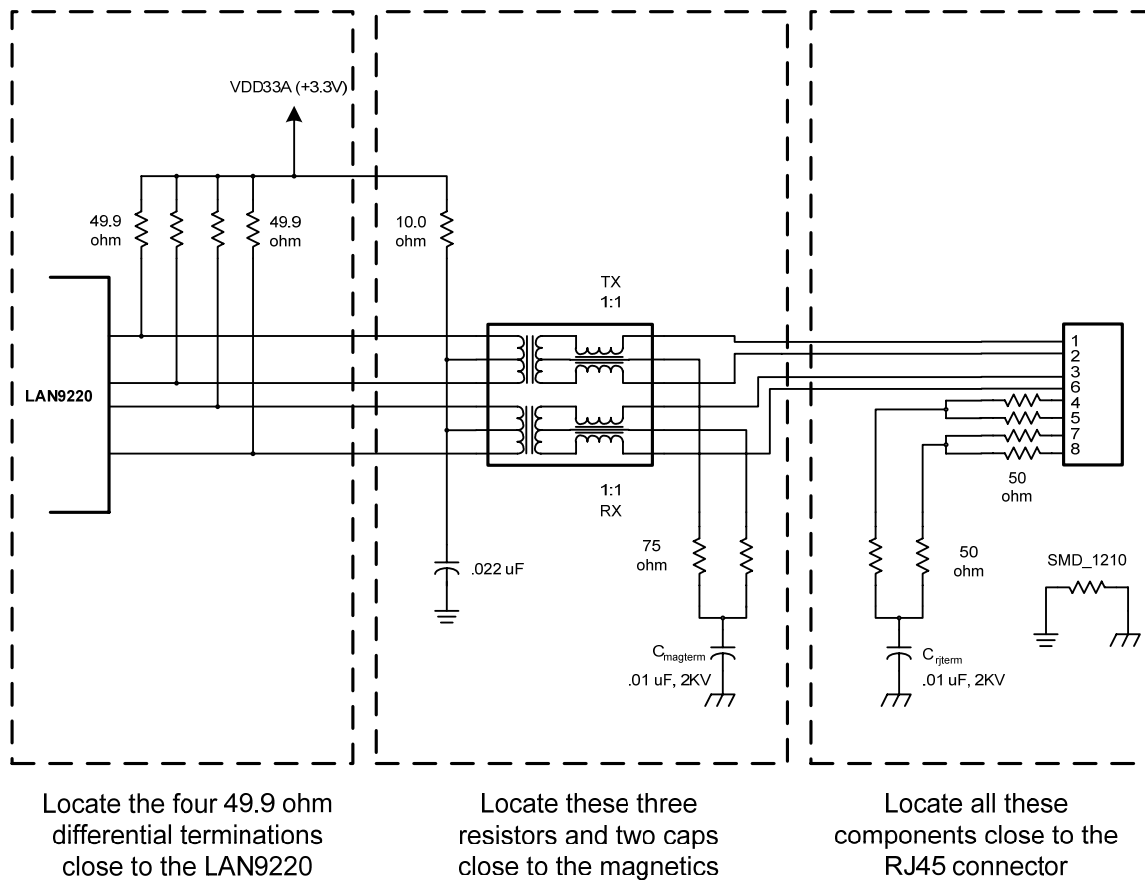


Figure No.1 Indicating Component Placement

The figure above shows the pull-up terminations for the TX+ & TX- signals placed close to the LAN9220 for an Auto MDIX enabled application. For an Auto MDIX disabled application, these same two resistors should be located as close as possible to the magnetics.

+3.3V Power Supply Connections:

1. Place the (1) VDD33REG decoupling capacitor for the LAN9220 QFN as close to the VDD33REG power pin as possible. Using an SMD_0603 package will make this task easier.
2. Place the (3) VDD33A decoupling capacitors for the LAN9220 QFN as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

+1.8V to +3.3V Variable I/O Power Supply Connections:

1. Place the (4) VDDVARIO decoupling capacitors for the LAN9220 QFN as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

VDD18CORE:

1. VDD18CORE (pin 2) requires a 0.01 μ F bypass capacitor and a low ESR 10 μ F bulk capacitor placed as close as possible to pin 2.
2. The other VDD18CORE (pin 37) only requires a 0.01 μ F bypass capacitor placed as close as possible to pin 37.

VDD18A:

1. VDD18A (pin 53) only requires a 0.01 μ F bypass capacitor placed as close as possible to pin 53.

Ground Connections:

1. There are no component placement issues associated with the LAN9220 QFN ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible. The exposed die paddle (pin 57) ground on the bottom of the LAN9220 will be connected immediately to this solid digital ground plane.

Crystal Connections:

1. Place the 25 MHz crystal, the 1.0 M Ω parallel resistor, the zero ohm series EMI resistor and the associated 15 – 33 μ F capacitors as close together as possible and as close to the LAN9220 QFN (XTAL1, pin 55 & XTAL2, pin 54) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)
2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all the crystal components are referenced to the same reference plane.

EEPROM Interface:

1. There are no component placement issues associated with the EEPROM Interface.

EXRES Resistor:

1. Place the EXRES resistor as close to pin 50 of the LAN9220 QFN as possible.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups/Pull-downs required by the LAN9220 QFN.

CPU Interface:

1. The design engineer must review placement issues associated with the Host Bus CPU Interface. Specific processor design guidelines should be reviewed in determining the placement of the LAN9220 device with respect to the processor. Address, data and control signal trace lengths must be considered when placing these two devices. Critical timing issues may arise if recommended trace lengths are exceeded.

Internal Pull-up / Pull-down Augmentation:

1. There are no component placement issues associated with the extra external pull-ups or pull-downs required by the LAN9220 when operating at lower than +3.0V on the VDDVARIO.

Miscellaneous:

1. Bulk capacitors for each power plane can reside anywhere on the plane they serve.
2. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.