AVR32EB14/20/28/32 Silicon Errata and Data Sheet Clarifications

AVR32EB14/20/28/32 SEDSC

www.microchip.com Product Pages: AVR32EB14, AVR32EB20, AVR32EB28, AVR32EB32

The AVR32EB14/20/28/32 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002615), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR32EB14/20/28/32 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002615) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A0
Device	Write Operation Lost if Consecutive Writes to Specific Address Spaces	X
	Limitation on Flash Boot Size and Flash Code Size Fuses	X
ADC	Missing Codes When Using Internal Reference and CPU is Running	X
	Missing Codes When Using Internal Reference and CPU is Running	X
CRCSCAN	Running CRC Scan on Part of The Flash is Non-Functional	X
NVMCTRL	Flash-Self Programming Failing When Flash Read During Programming	X
TCF	Prescaler Non-Functional in NCO Modes	X
	Reading Count Value Might Return Wrong Value	X
USART	Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.

X Erratum is applicable.

2.2 Device

2.2.1 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. A0
X

2.2.2 Limitation on Flash Boot Size and Flash Code Size Fuses

If CRC is enabled through fuse (CRCSRC in FUSE.SYSCFG0) or started from software using CRCSCAN, the Flash Boot Size (FUSE.BOOTSIZE) and Flash Code Size (FUSE.CODESIZE) must be configured to be a multiple of 512 bytes (LSb of FUSE.BOOTSIZE and FUSE.CODESIZE must be '0').

Work Around

None.

Affected Silicon Revisions

Rev. A0
X

2.3 ADC - Analog-to-Digital Converter

2.3.1 Missing Codes When Using Internal Reference and CPU is Running

The ADC has missing codes when selecting internal reference (REFSEL in ADCn.CTRLC) and performing conversions when the CPU runs.

Work Around

Perform ADC conversions using external reference or keep the device in Idle or Standby sleep mode.

Affected Silicon Revisions

Rev. A0
X

2.3.2 Missing Codes When Using Internal Reference and CPU is Running

The ADC has missing codes when selecting internal reference (REFSEL in ADCn.CTRLC) and performing conversions when the CPU runs.

Work Around

Perform ADC conversions using external reference or keep the device in Idle or Standby sleep mode.

Affected Silicon Revisions

Rev. A0
X

2.4 CRCSCAN - Cyclic Redundancy Check Memory Scan

2.4.1 Running CRC Scan on Part of The Flash is Non-Functional

- Running CRC scan on the boot section does not work if FUSE.BOOTSIZE is different from `0x00`
- Running CRC scan on the boot and application section does not work if FUSE.CODESIZE is different from `0x00`
- Running CRC scan on the entire Flash works

Work Around

None

Affected Silicon Revisions

Rev. A0
X

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Flash-Self Programming Failing When Flash Read During Programming

If data are read from the Flash NRWW section while the Flash RWW section is being written to or erased (Flash Page Write or Flash Page Erase), the erase or write may fail. Instruction fetch from the Flash NRWW section does not affect erase or write operation to the Flash RWW section.

Work Around

Alternative 1: RWW functionality not needed

- Do not use flash self-programming when executing from the NRWW section

Alternative 2: RWW functionality needed

- Enable BOD in continuous mode (in FUSE.BODCFG, set bitfield LVL to BODLEVEL1 or higher and bitfield ACTIVE to `0x3`)
- Do not use the *Flash Page Erase and Page Write* operation (writing the CMD bitfield in NVMCTRL.CTRLA to `0x05`). Execute Flash Page Erase and Flash Page Write as two separate operations instead.

Affected Silicon Revisions

Rev. A0
X

2.6 TCF - 24-bit Timer/Counter Type F

2.6.1 Prescaler Non-Functional in NCO Modes

When the TCF is configured to either NCOPF or NCOFDC mode (CNTMODE in TCFn.CTRLB is `0x1` or `0x2`), the prescaler in (PRESC in TCFn.CTRLA) is non-functional.

Work Around

None

Affected Silicon Revisions

Rev. A0
X

2.6.2 Reading Count Value Might Return Wrong Value

The TCF counter value (TCFn.CNT) is continuously updated from asynchronous domain, which can result in reading an incorrect counter value. The higher bytes (TCFn.CNT1 and TCFn.CNT2) may change after reading the lower bytes (TCFn.CNT0 and TCFn.CNT1).

Work Around

None.

Affected Silicon Revisions

Rev. A0
X

2.7 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.7.1 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A0
X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002615).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
A	11/2024	Initial document release

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