SY89872U

2.5V, 2 GHz Any Differential In-to-LVDS Programmable Clock Divider/Fanout Buffer with Internal Termination

Features

- Guaranteed AC Performance Over Temperature and Voltage:
  - > 2 GHz f_{MAX}
  - < 750 ps t_{pd} (Matched Delay between Banks)
  - < 15 ps Within-device Skew
  - < 200 ps t_r/t_f
- Low Jitter Design:
  - 265 fs RMS Phase Jitter
- Unique input termination and VT pin for DC-coupled and AC-coupled inputs: any differential inputs (LVPECL, LVDS, CML, HTSL)
- Precision Differential LVDS outputs
- Matched Delay: All Outputs Have Matched Delay, Independent of Divider Setting
- TTL/CMOS Inputs for Select and Reset/Disable
- Two Output Banks (Matched Delay)
  - Bank A: Buffered Copy of Input Clock (Undivided)
  - Bank B: Divided Output (÷2, ÷4, ÷8, ÷16), Two Copies
- 2.5V Power Supply
- Wide Operating Temperature Range: –40°C to +85°C
- Available in 3 mm × 3 mm 16-lead VQFN Package

Applications

- OC-3 to OC-192 SONET/SDH Applications
- Transponders
- Oscillators
- SONET/SDH Line Cards

General Description

This 2.5V low-skew, low-jitter, precision LVDS output clock divider accepts any high-speed differential dock input (either AC-coupled or DC-coupled) CML, LVPECL, HSTL, or LVDS and divides down the frequency by using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock.

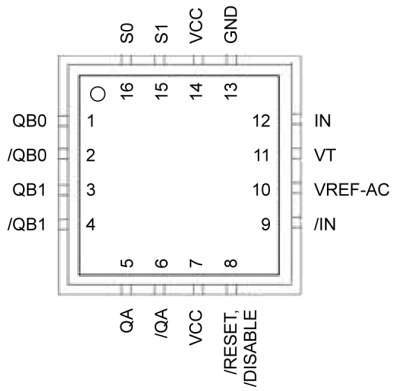
The SY89872U includes two output banks. Bank A Is an exact copy of the input dock (pass through) with matched propagation delay to Bank B, the divided output bank. Available divider ratios are 2, 4, 8, and 16. In a typical 622 MHz clock system, this would provide availability of 311 MHz, 155 MHz, 77 MHz, or 38 MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

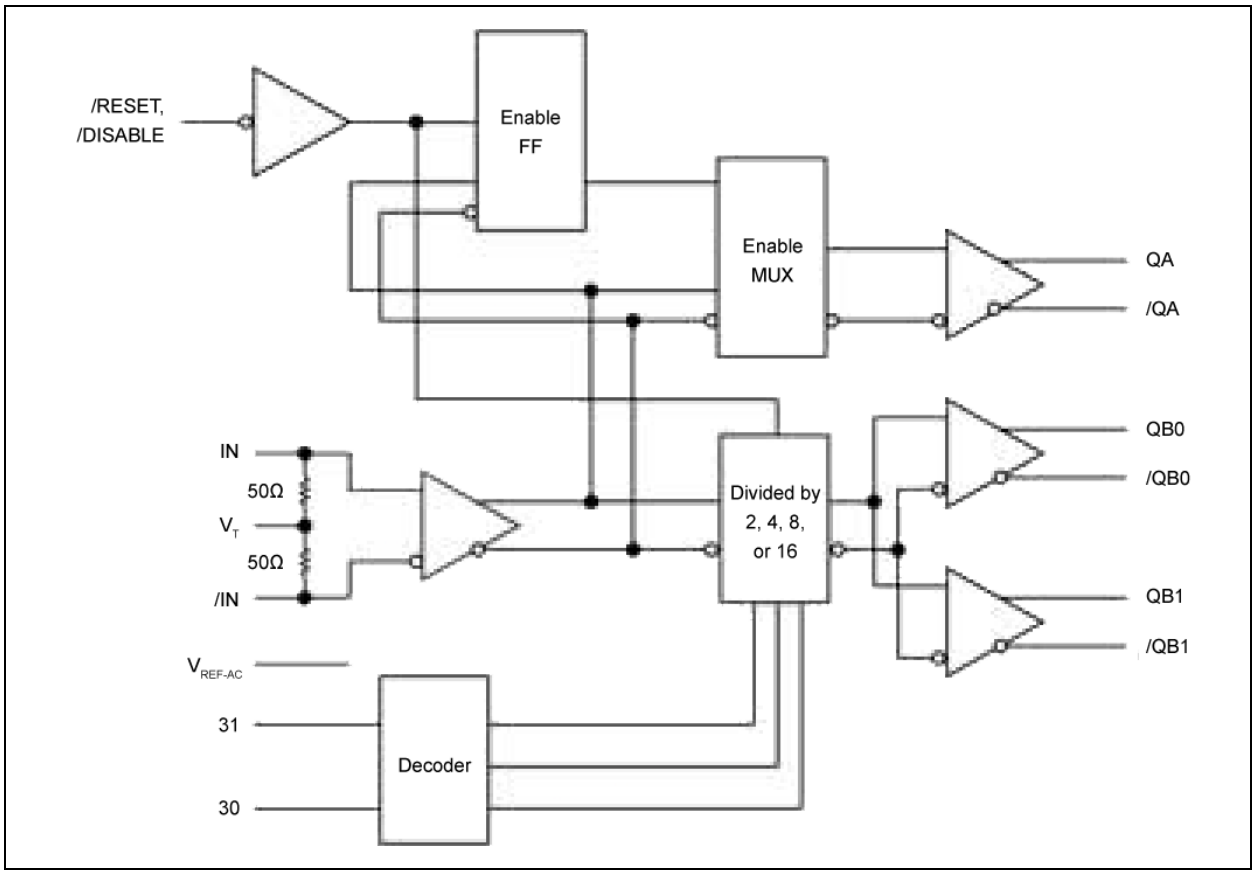
The SY89872U is part of Microchip's high-speed Precision Edge® timing and distribution family. For 3.3V applications, consider the SY89873L. For applications that require an LVPECL output, consider the SY89872U. The /RESET input asynchronously resets the divider outputs (Bank B). In the pass-through function (Bank A) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN). Refer Section 7.0, Timing Diagram:

Package Type

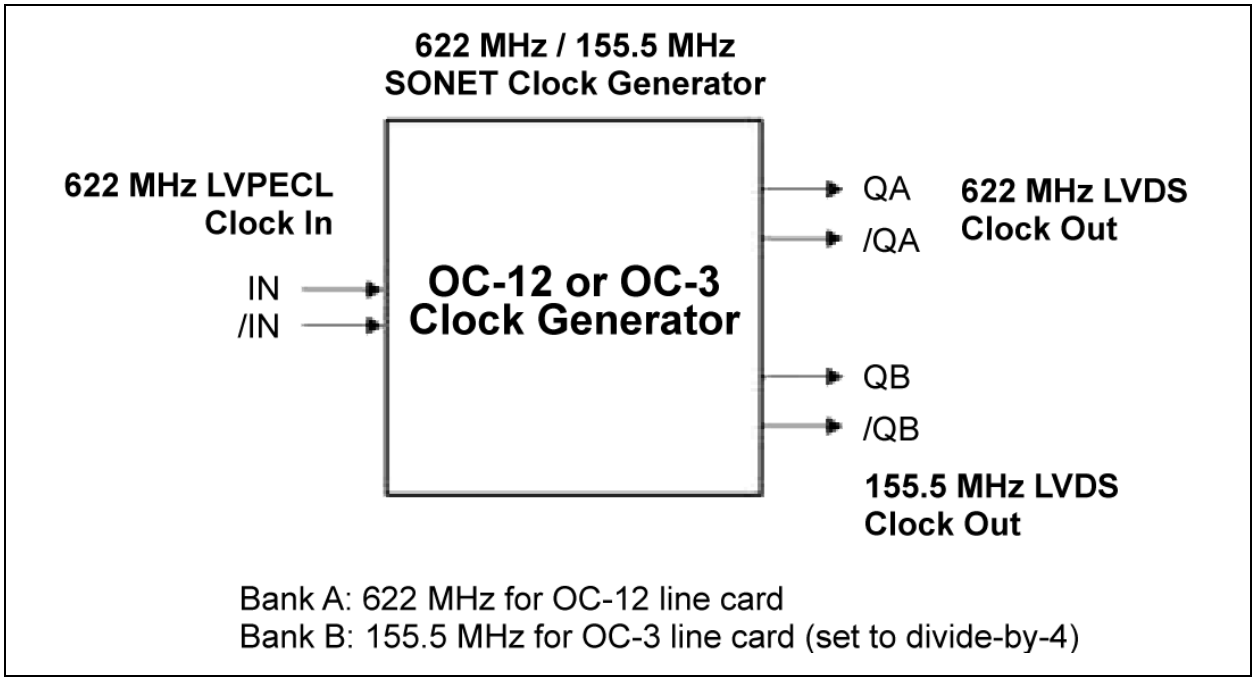
SY89872U
16-Lead VQFN



Functional Block Diagram



Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVDS Output Current (I_{OUT}) ..... ±10 mA
Input Current IN, /IN (I_{IN}) ..... ±50 mA
V_{REF-AC} Input Sink/Source Current ($I_{VREF-AC}$), Note 1 ..... ±2 mA

Operating Ratings††

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

All values applicable for when T_A = –40°C to +85°C unless otherwise noted. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Voltage	V_{CC}	2.375	2.5	2.625	V	—
Power Supply Current	I_{CC}	—	75	110	mA	No load, max. V_{CC}
Differential Input Resistance (IN to /IN)	R_{IN}	90	100	110	Ω	—
Input HIGH Voltage (IN, /IN)	V_{IH}	0.1	—	V_{CC} + 0.3	V	Note 3
Input LOW Voltage (IN, /IN)	V_{IL}	–0.3	—	V_{IH} – 0.1	V	Note 3
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	V_{CC}	V	Note 3 and Note 4
Differential Input Voltage Swing |IN – /IN|	V_{DIFF_IN}	0.2	—	—	V	Note 3, Note 4, and Note 5
Input Current IN, /IN	$\|I_{IN}\|$	—	—	45	mA	Note 3
Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	Note 6

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Specification for packaged product only.

3: Due to the internal termination (see Section 8.0, Input Buffer Structure) the input current depends on the applied voltages at IN, /IN, and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

4: See Section 7.0, Timing Diagram for V_{IN} definition. V_{IN} (max.) is specified when V_T is floating.

5: See Figure 6-1 and Figure 6-2 for V_{DIFF} definition.

6: Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to V_T pin.

TABLE 1-2: LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% and T_A = –40°C to +85°C, unless otherwise noted. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Voltage Swing	V_{OUT}	250	350	450	mV	Note 3
Output High Voltage	V_{OH}	—	—	1.475	V	Note 4
Output Low Voltage	V_{OL}	0.925	—	—	V	Note 4
Output Common Mode Voltage	V_{OCM}	1.125	—	1.375	V	Note 5
Change in Common Mode Voltage	ΔV_{OCM}	–50	—	50	mV	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Specification for packaged product only.

3: See Figure 6-1.

4: Measured as per Figure 5-1, 100Ω across Q and /Q outputs.

5: Measured as per Figure 5-2.

TABLE 1-3: LVTTL/CMOS INPUTS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% and T_A = –40°C to +85°C, unless otherwise noted. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input HIGH Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input LOW Voltage	V_{IL}	0	—	0.8	V	—
Input HIGH Current	I_{IH}	–125	—	20	µA	—
Input LOW Current	I_{IL}	—	—	–300	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Specification for packaged product only.

TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% and T_A = –40°C to + 85°C, unless otherwise noted. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Toggle Frequency	f_{MAX}	2	—	—	GHz	Output swing: ≥200 mV
Maximum Input Frequency		3.2	—	—	GHz	Note 3
Differential Propagation Delay IN-to-Q	t_{pd}	500	625	750	ps	Input swing: <400 mV
		450	575	700	ps	Input Swing: ≥400 mV
Within-Device Skew (Differential) (QB0-to-QB1)	t_{SKEW}	—	7	15	ps	Note 4
Within-Device Skew (Differential) (Bank A-to-Bank B)		—	12	30	ps	Note 4
Part-to-Part Skew (Differential)		—	—	250	ps	Note 4
Reset Recovery Time	t_{rr}	600	—	—	ps	Note 5
RMS Phase Jitter	t_{JITTER}	—	265	—	fs	Output = 622 MHz, Integration Range: 12 kHz–20 MHz
Rise/Fall Times (20% to 80%)	t_r, t_f	70	130	200	ps	—

Note 1: Measured with 400 mV input signal, 50% duty cycle, 100Ω termination between Q and /Q, unless otherwise stated.

2: Specification for packaged product only.

3: Bank A (pass-through) maximum frequency is limited by the output stage. Bank B (input-to-output +2, +4, +8, +16) can accept an input frequency >3 GHz, while Bank A will be slew rate limited.

4: Skew is measured between outputs under identical transitions.

5: See Section 7.0, Timing Diagram.

TABLE 1-5: TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
VQFN, Still Air	θ_{JA}	—	+60	—	°C/W	—
VQFN, 500 lfpm		—	+54	—	°C/W	—
VQFN, Junction-to-Board (Note 1)	Ψ_{JB}	—	+32	—	°C/W	—

Note 1: Junction-to-board resistance assumes exposed pad Is soldered (or equivalent) to the device's most negative potential on the PCB.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2, 3, 4	QB0, /QB0 QB1, /QB1	Differential LVDS Compatible Outputs: Divide by 2, 4, 8, 16. Unused outputs must be terminated with 100Ω across the pin (Q, /Q),
5, 6	QA, /QA	Differential L VOS Compatible Undivided Output Clock.
7, 14	VCC	Positive Power Supply: Bypass with 0.1 µF/0.01 µF low ESR capacitors.
8	/RESET, /DISABLE	Output Reset and Output Enable/Disable: Internal 25 kΩ pull-up. Input threshold is $V_{CC}/2$. Logic LOW will reset the divider select, and align Bank A and Bank B edges, In addition, when LOW, Bank A and Bank B will be disabled.
12, 9	IN, /IN	Differential Reference Input Clock Internal 50Ω termination resistors to V_T input. See Section 9.0, Input Interface Applications.
10	VREF-AC	Reference Voltage: Equal to V_{CC} – 1.4V (approx.). and used for AC-coupled applications. Maximum sink/source current is 0.5 mA. See Section 9.0, Input Interface Applications,
11	VT	Termination Center-Tap: For DC-Coupled CML and LVDS inputs, leave this pin floating, See Section 9.0, Input Interface Applications,
13	GND	Ground.
15, 16	S1, S0	Select Pins: LVTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). S0 = LSB. Input threshold is $V_{CC}/2$.

TABLE 2-2: TRUTH TABLE

/RESET /DISABLE	S1	S0	Bank A Output	Bank B Outputs
1	0	0	Input Clock	Input Clock + 2
1	0	1	Input Clock	Input Clock + 4
1	1	0	Input Clock	Input Clock + 8
1	1	1	Input Clock	Input Clock + 16
0	X	X	QA = Low, /QA = High (Note 1)	QB0 = Low, /QB0 = High (Note 2) QB1 = Low, /QB1 = High (Note 2)

Note 1: On the next negative transition of the input signal.

2: Asynchronous reset/disable function. See Section 7.0, Timing Diagram.

3.0 TYPICAL CHARACTERISTICS

V_{CC} = 2.5V; V_{IN} = 400 mV, T_A = 25°C, unless otherwise noted.

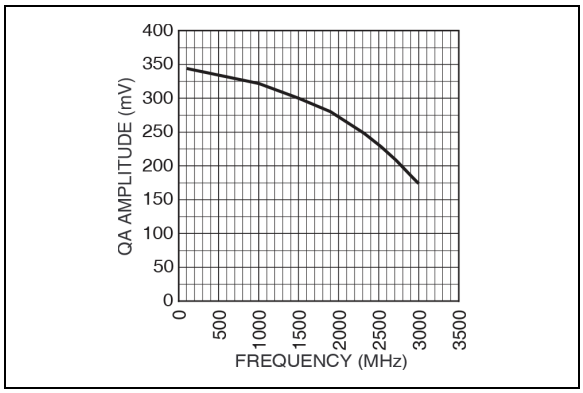


FIGURE 3-1: QA OUTPUT AMPLITUDE VS. FREQUENCY.

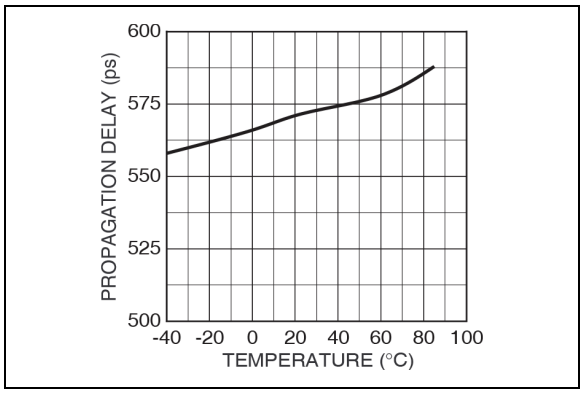


FIGURE 3-3: IN TO Q PROPAGATION DELAY VS. TEMPERATURE.

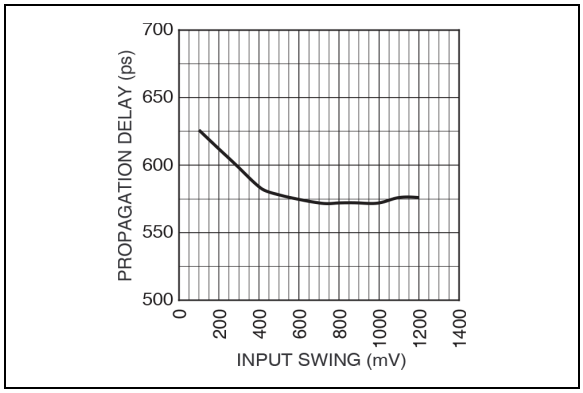


FIGURE 3-2: IN TO Q PROPAGATION DELAY VS. INPUT SWING.

4.0 TYPICAL OUTPUT WAVEFORMS

V_{CC} = 2.5V; V_{IN} = 400 mV, T_A = 25°C, unless otherwise noted.

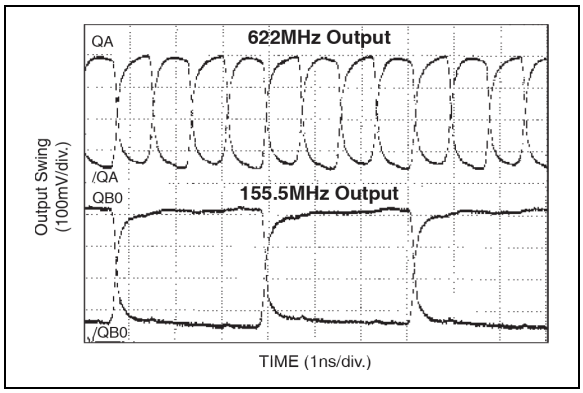


FIGURE 4-1: QA @ 622 MHZ AND QB @ 155.5 MHZ (DIVIDE-BY-4).

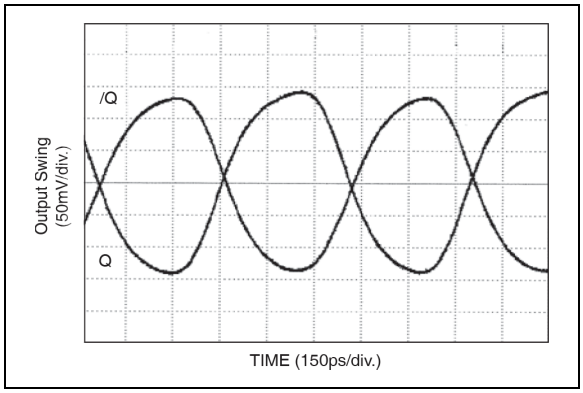


FIGURE 4-2: 1.25 GHZ OUTPUT.

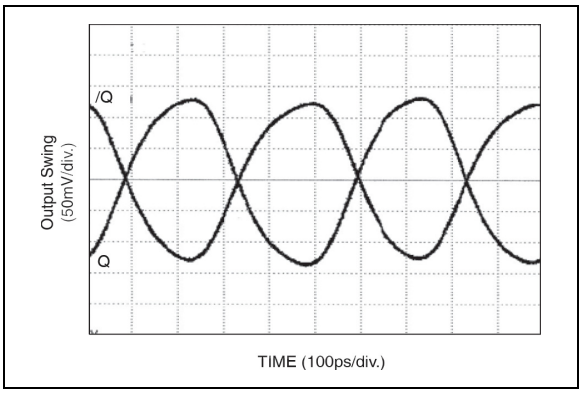


FIGURE 4-3: 2 GHZ OUTPUT.

5.0 LVDS OUTPUT

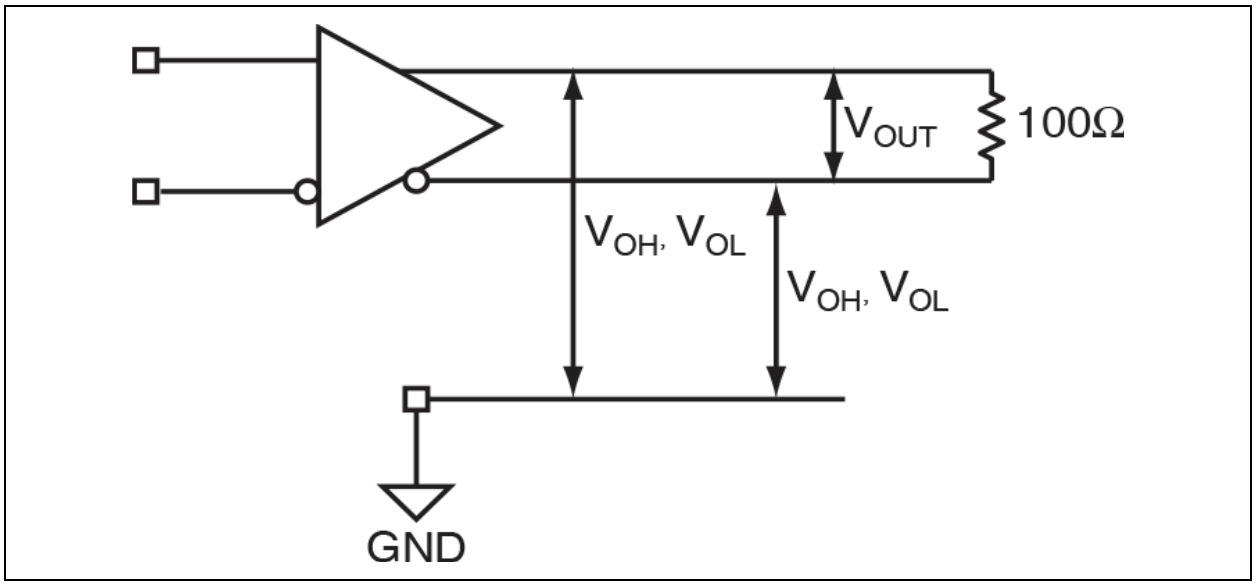


FIGURE 5-1: LVDS DIFFERENTIAL MEASUREMENT.

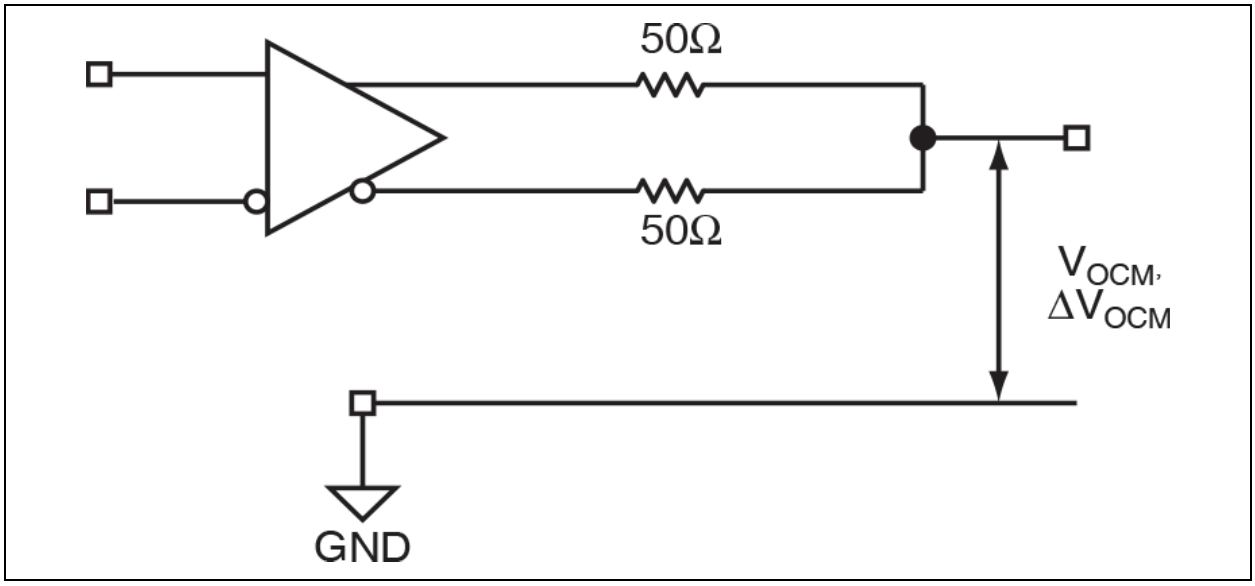


FIGURE 5-2: LVDS COMMON MODE MEASUREMENT.

6.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

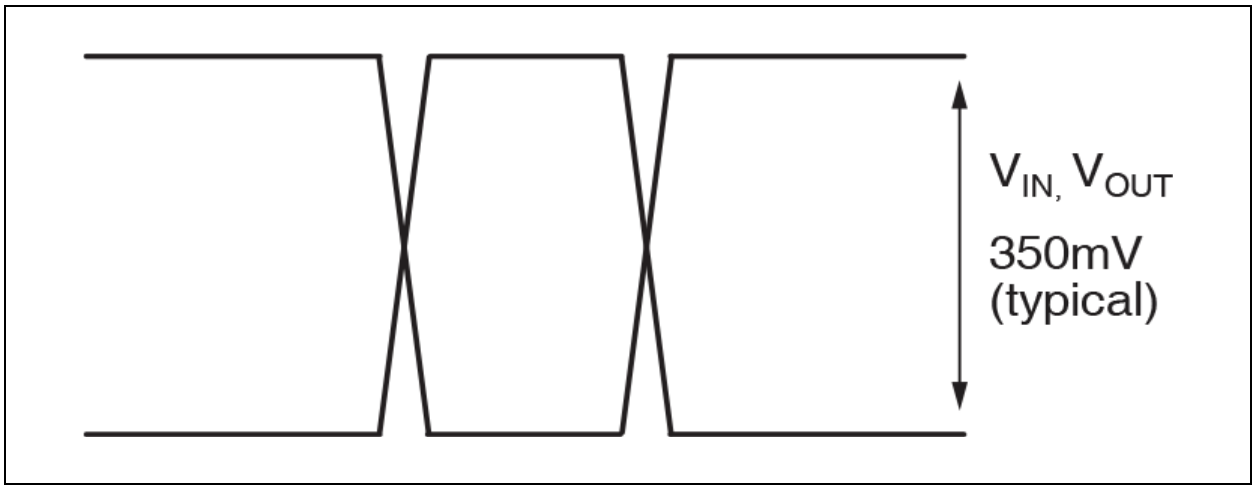


FIGURE 6-1: SINGLE-ENDED VOLTAGE SWING.

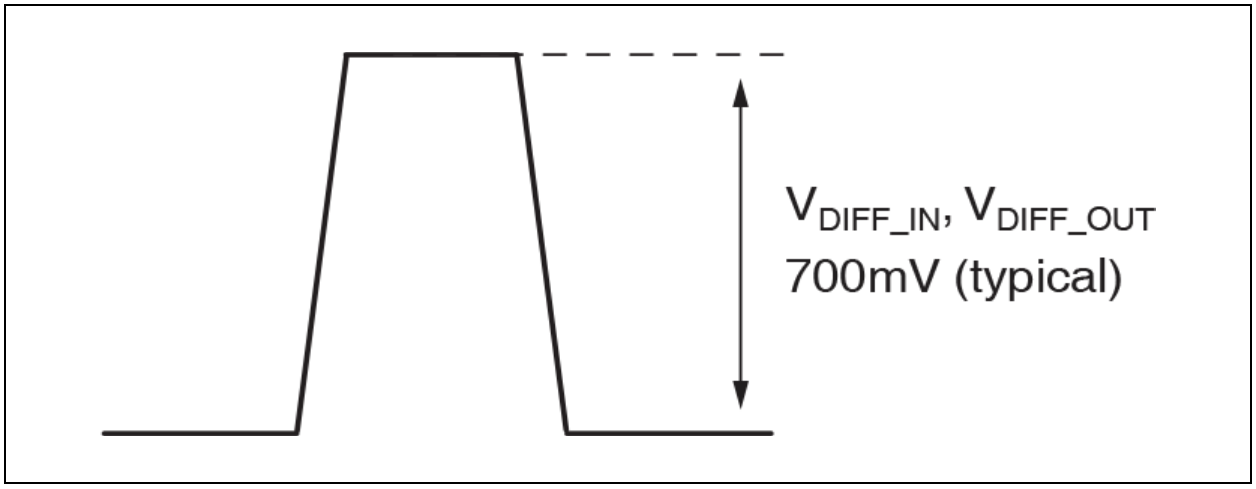


FIGURE 6-2: DIFFERENTIAL VOLTAGE SWING.

7.0 TIMING DIAGRAM

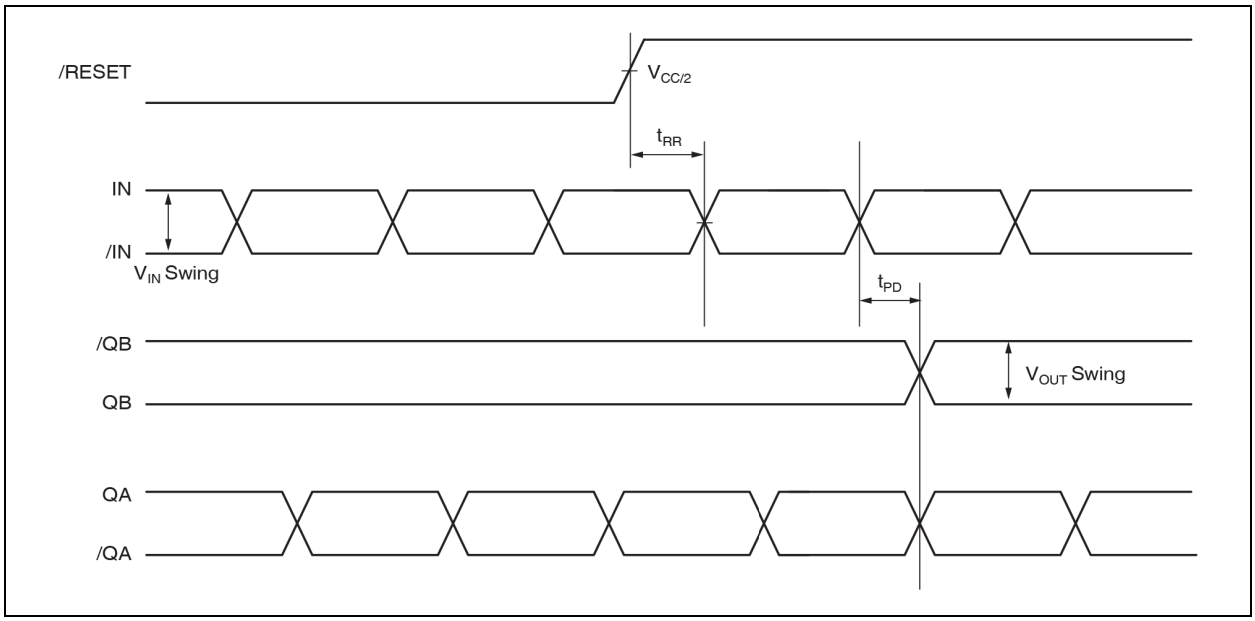


FIGURE 7-1: TIMING DIAGRAM.

8.0 INPUT BUFFER STRUCTURE

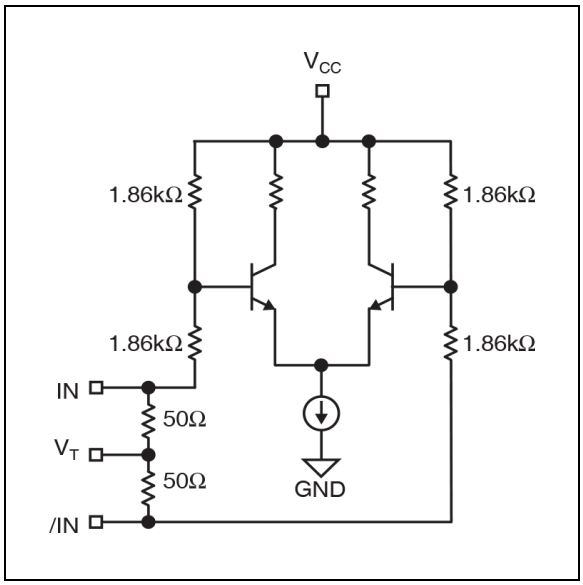


FIGURE 8-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.

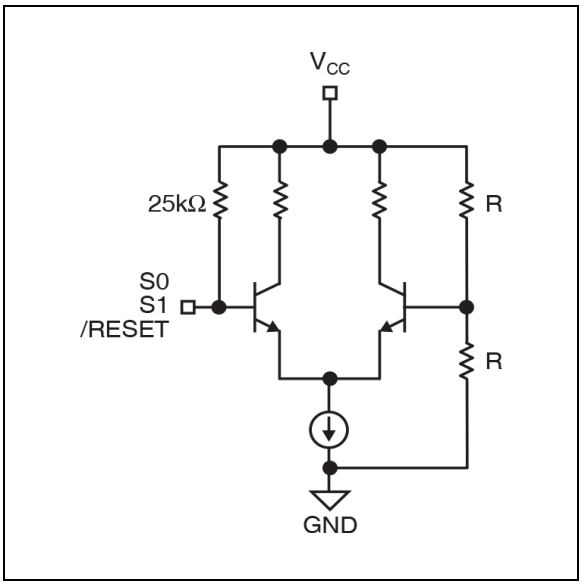


FIGURE 8-2: SIMPLIFIED TTL/CMOS INPUT BUFFER.

9.0 INPUT INTERFACE APPLICATIONS

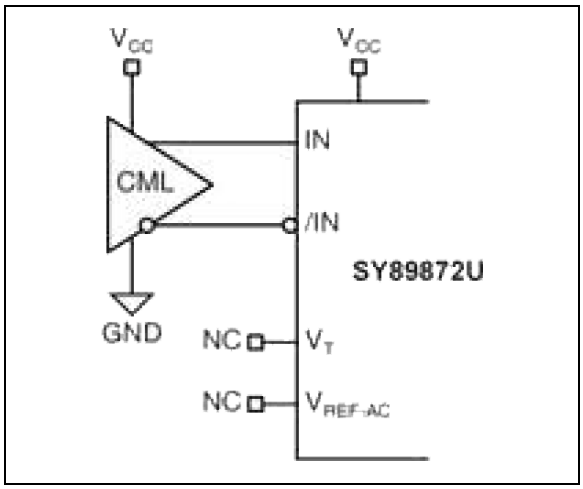


FIGURE 9-1: DC-COUPLED CML INPUT INTERFACE.

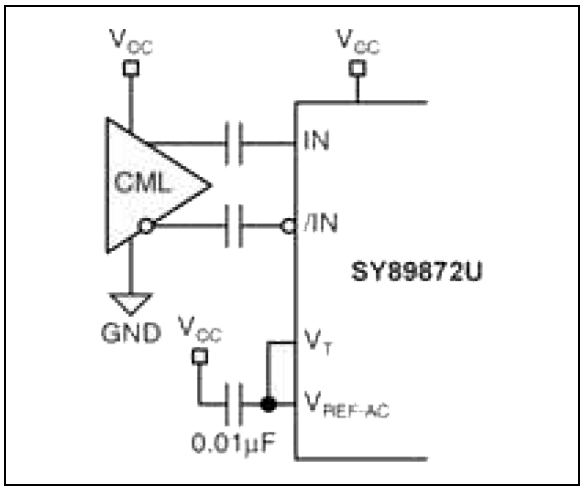


FIGURE 9-2: AC-COUPLED CML INPUT INTERFACE.

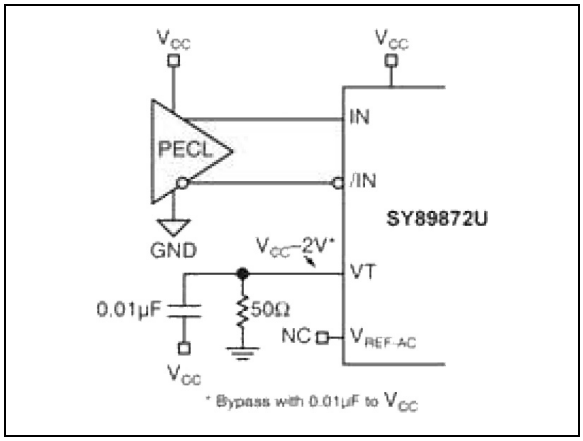


FIGURE 9-3: DC-COUPLED PECL INPUT INTERFACE.

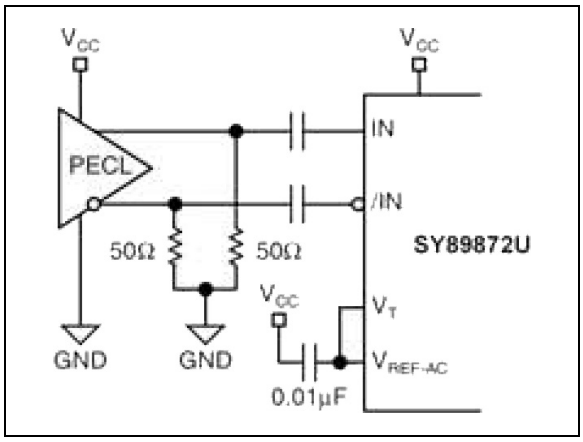


FIGURE 9-4: AC-COUPLED PECL INPUT INTERFACE.

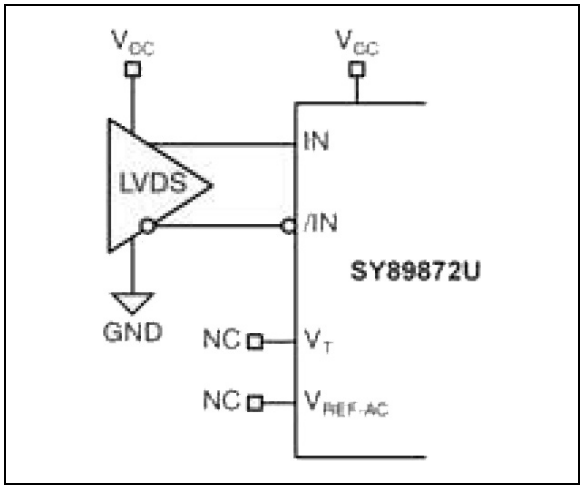


FIGURE 9-5: DC-COUPLED LVDS INPUT INTERFACE.

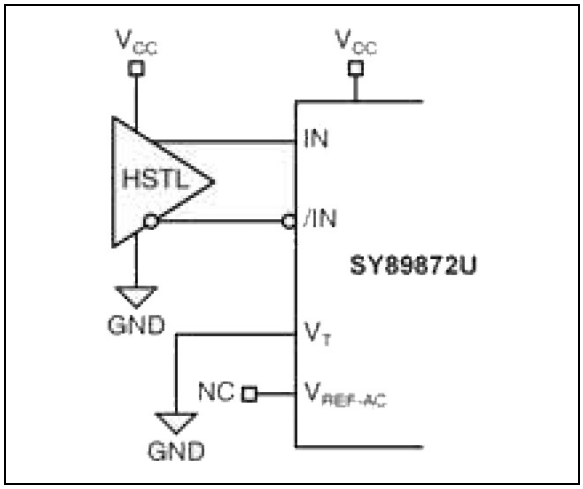
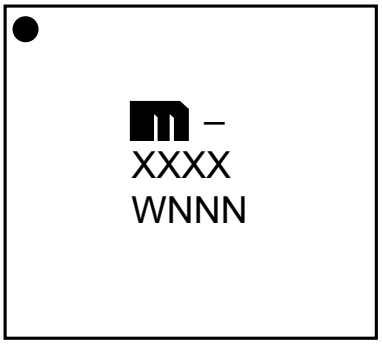


FIGURE 9-6: HSTL INPUT INTERFACE.

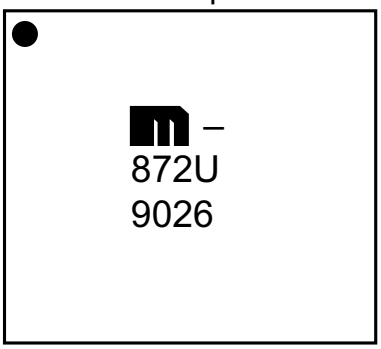
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

16-Lead VQFN*



Example*



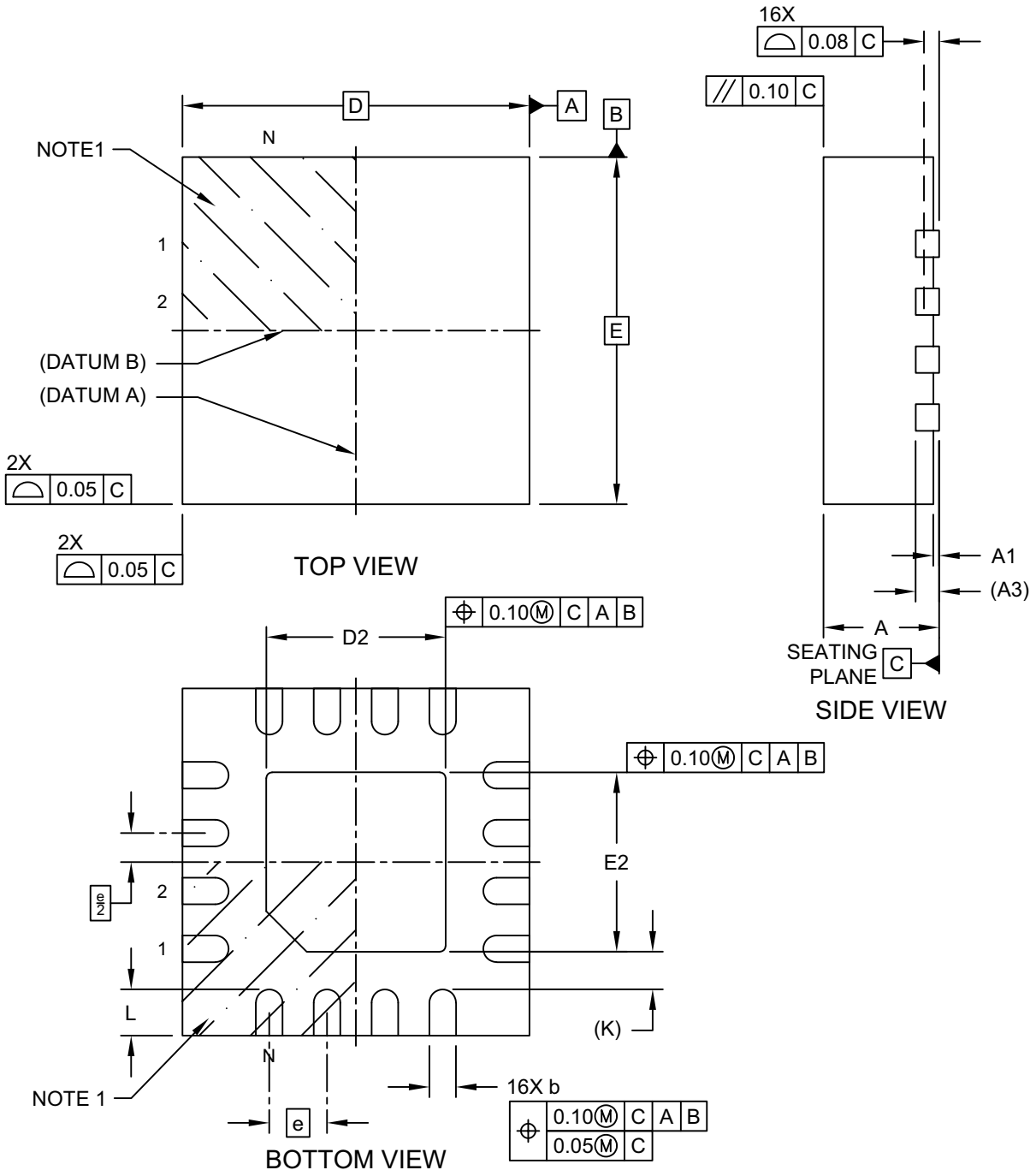
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

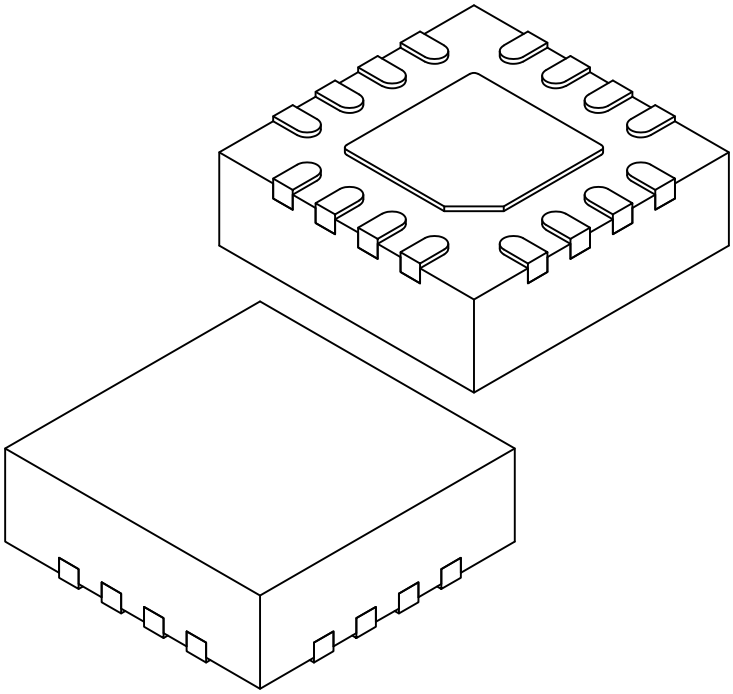
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

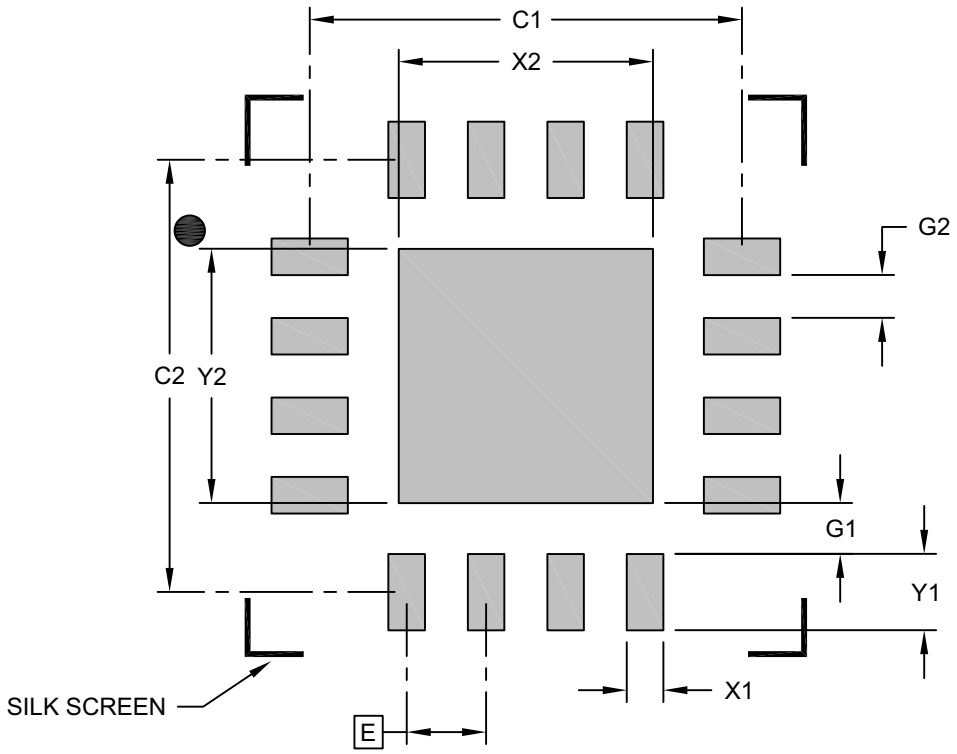
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Converted Micrel data sheet for SY89872U to Microchip format as DS20006871A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY89872	=	2.5V, 2 GHz Any Differential In-to-LVDS Programmable Clock Divider/Fanout Buffer with Internal Termination
Voltage Option:	U	=	2.5V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) **SY89872UMG**

2.5V, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY89872UMG-TR**

2.5V, 16-Lead VQFN, –40°C to 85°C, 1,000/Reel

NOTES:

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