dsPIC30F1010/202X to dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Migration Guide

INTRODUCTION

This document provides an overview of considerations for migrating from dsPIC30F1010/202X devices to dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. If you are undertaking this migration, it is recommended that you download data sheets and errata documents for these devices from www.microchip.com.

The code developed for the dsPIC30F1010/202X devices can be ported to the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices after making the appropriate changes outlined in this document.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices are based on a new architecture and feature many improvements and new capabilities over the dsPIC30F1010/202X devices, such as:

- Reduced power consumption
- Flash increased from 12 Kbytes (dsPIC30F2020/2023) to 16 Kbytes (dsPIC33FJ16GSX02/X04)
- Operating frequency increased from 30 MIPS to 40 MIPS
- RAM increased from 512 bytes (dsPIC30F2020/2023) to 2 Kbytes (dsPIC33FJ16GSX02/X04)
- More flexible PLL and clocking scheme
- Reference Clock Output feature added
- Peripheral Pin Select feature added
- Upgraded PWM module with 1.04 ns resolution for phase, dead time and period
- True independent PWM mode – separate Period, Duty Cycle, and Phase for PWMxH and PWMxL outputs
- Secondary PWM trigger and dual trigger modes added
- PWM capture feature added
- PWM swap feature added
- PWM clock divider added
- Center-aligned PWM mode added
- Independent Fault mode added (affects PWMxH and PWMxL outputs independently)
- Additional PMD bits added to disable individual PWM channels for power-saving
- Upgraded ADC module to 4 Msps (dsPIC33FJ16GS50X)
- Asynchronous sampling feature added to ADC
- Upgraded Analog Comparator module with DAC update time of 650 ns
- DAC output provided
- JTAG support added
- BOR module added

Note 1: The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices have been designed to perform to the parameters provided in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318), and have been tested to electrical specifications designed to determine their conformance with these parameters. Due to manufacturing process differences, these devices may have different performance characteristics than their earlier versions. These differences may cause these devices to perform differently in your application than their earlier versions.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

OPERATING RANGE

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices operate at a supply voltage of 3.0V to 3.6V unlike dsPIC30F1010/202X devices, which operate at 4.5V to 5.5V. This affects the dsPIC® DSC supply voltage, input and output voltages of the I/O ports, and the ADC and comparator reference voltages. The circuitry surrounding the dsPIC DSC device, which includes modules like gate driver ICs, opto couplers, logic devices, memory interfaces and op amps, must be modified appropriately. This is discussed further in the input/output voltage tolerance, high-speed PWM and analog comparator sections. The operating frequency is up to 40 MIPS. The specified operating temperature range is -40°C to +125°C.

PIN CONFIGURATION

The dsPIC30F and dsPIC33F families are pin compatible with the exception of the I^2C pins (44-pin devices-only), the General Purpose I/O (GPIO) pins, and the VDDCORE pin. This is reflected in the pin diagrams of the 28-pin SPDIP and SOIC and the 44-pin QFN, QFN-S and TQFP devices.

All digital peripherals (SPI, UART, Input Capture and Output Capture) are remappable. In order to migrate from dsPIC30F devices to dsPIC33F devices, these peripherals should be remapped in software using the same pins as the dsPIC30F devices.

The VDDCORE pin must be connected to the circuit ground via a 1 µF to 10 µF capacitor as shown in Figure 1. This particular pin is a VDD pin on dsPIC30F1010/202X devices. Refer to the **"Pin Diagrams"** section in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318) for pin diagrams showing the VDDCORE pin.

FLASH PROGRAM MEMORY

Just like the dsPIC30F1010/202X devices, the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices also support Run Time Self-Programming (RTSP). Table 1 lists the RTSP differences between the two device families for the high-endurance Flash program memory.

INPUT/OUTPUT VOLTAGE TOLERANCE

Some I/O pins on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices are not 5V tolerant. For a detailed description of the 5V tolerant behavior of the I/O pins, refer to Table 9-1 in **Section 9.0 "I/O Ports"** of the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

The dsPIC33F devices work at a nominal operating voltage of 3.3V. Therefore, all output pins on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices generate outputs equal to 3.3V, unlike outputs equal to 5V on dsPIC30F1010/202X devices. In addition, there may be changes in the VIH, VIL, VOH, and VOL specifications. Refer to Table 23-9 and Table 23-10 in **Section 23. "Electrical Characteristics"** of the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318) for I/O pin input/output specifications.

Table 9-1 in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318) shows the current sink/source capability of the I/O pins. When migrating from a dsPIC30F device to a dsPIC33F device, care must be taken to make all supporting circuitry compatible with the source/sink capability of the dsPIC33F device. The open-drain feature allows the generation of outputs higher than VDD = 3.3V (for example, 5V) on any desired digital-only pin by using external pull-up resistors.

For more information on the specifics of open-drain configuration refer to **Section 9.0 "I/O Ports"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

FIGURE 1: VDDCORE CIRCUIT

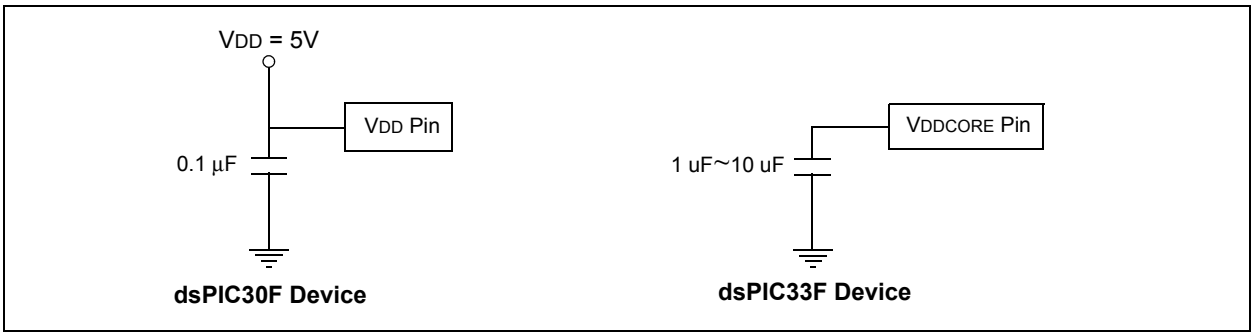

TABLE 1: RTSP CHANGES FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 DEVICES

Parameter	dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04	dsPIC30F1010/202X
Smallest Program Memory Erase Size	One page – 512 instructions or 1536 bytes	One row – 32 instructions or 96 bytes
Smallest Program Memory Program Size	One row – 64 instructions or 192 bytes	One row – 32 instructions or 96 bytes

INTERRUPT CONTROLLER

Some changes have been made to the Interrupt Request Flag Register (IFSx), Interrupt Enable Register (IECx) and Interrupt Priority Control Register (IPCx) on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. The locations of the interrupt flag status bits, interrupt enable control bits, and interrupt priority level set bits have been moved across the IFSx, IECx and IPCx registers. For more information on the specifics of these bit locations, refer to **Section 6.0 "Interrupt Controller"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

PERIPHERAL PIN SELECT

Peripheral Pin Select (PPS) is a new feature added to the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. It enables peripheral set selection and placement on a wide range of I/O pins unlike the dedicated pin configuration on the dsPIC30F1010/202X devices.

The Peripheral Pin Select configuration feature operates over a fixed subset of I/O pins. Users have to independently map the input and/or output of the remappable peripherals to any of the available remappable pins.

For more information on the complete list of peripherals that can be selected using the Peripheral Pin Select feature refer to **Section 9.0 "I/O Ports"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

OSCILLATOR CONFIGURATION

The Oscillator architecture has changed. Various speeds of operation can be achieved on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices by using the on-chip PLL and setting the appropriate values for the Clock Divisor (CLKDIV) register and the PLL Feedback Divisor (PLLFBD) register. The Oscillator Tuning Register 2 (OSCTUN2) and the Linear Feedback Shift (LFSR) registers present on dsPIC30F1010/202X devices have been removed in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. An additional bit, which indicates the Peripheral Pin Select Lock (IOLOCK), has been added to the Oscillator Control (OSCCON) register.

Refer to **Section 7.0 "Oscillator Configuration"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318) for a detailed explanation and examples on setting up the Oscillator Control registers for desired oscillator functioning.

Changes made to the Oscillator Control registers are summarized in Table 2.

Auxiliary Clock

A new Auxiliary Clock module has been added on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices in conjunction with the System Clock module and the PLL configuration to drive peripherals such as the High-Speed PWM and ADC, which need to operate at a frequency unrelated to the system clock. The primary oscillator or internal FRC oscillator sources can be used with or without the auxiliary PLL to obtain the auxiliary clock. The Auxiliary Clock Divisor Control (ACLKCON) register can be used to configure the auxiliary clock.

For more information and examples regarding configuration of the auxiliary clock, refer to **Section 7.0 "Oscillator Configuration"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

TABLE 2: SFR CHANGES FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 OSCILLATOR MODULE

SFR	Differences from dsPIC30F1010/202X	Data Sheet Reference
OSCCON	Two changes have been made to the Oscillator Control (OSCCON) register. 1. The Pseudo Random Clock Dither (PRCDEN) bit has been removed. 2. The FRC Tune Sequencer Enable (TSEQEN) bit has been removed.	**Section 7.0 "Oscillator Configuration"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318)
OSCTUN	The FRC Oscillator Tuning (TUN) bits in the FRC Oscillator Tuning Register have been extended to 5 bits providing more functionality. The Time Sequence Value (TSEQx) bits have been removed.	

HIGH-SPEED PWM

The PWM module on the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices has been upgraded with 1.04 ns resolution for phase, dead time and period. The Auxiliary clock provides the clock source for the PWM module. This is used with the appropriate PWM Input Clock Prescaler (PCLKDIV) bits in the PWM Clock Divider Select (PTCON2) register to generate the desired PWM clock. Refer to **43.5 "Module Description"** in **Section 43. "High-Speed PWM"** of the *"dsPIC33F Family Reference Manual"* for details.

Many changes have been made to the SFR registers associated with the PWM module. These changes are summarized in Table 3. Also, new registers have been added.

The PWM4L and PWM4H can be remapped using the Peripheral Pin Select (PPS) functionality.

Trigger Output Divider values less than 8 work on the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices unlike on the dsPIC30F1010/202X devices on which they did not. Trigger Output Divider value of 0 on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices behave as Trigger Output Divider value of 8 on dsPIC30F1010/202X devices. For the following combination of Trigger Output Divider bits and Trigger Postscaler Start Enable Select bits the trigger pulses behave differently on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices when compared to dsPIC30F1010/202X devices:

-TRGDIV = 0 & TRGSTRT = 0; -TRGDIV = 1 & TRGSTRT = 0

Refer to **Section 43. "High-Speed PWM"** of the *"dsPIC33F Family Reference Manual"* for more details.

For more information on the specifics of new registers and changes to the existing registers refer to **Section 14.0 "High-Speed PWM"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

TABLE 3: SFR CHANGES FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 HIGH-SPEED PWM MODULE

SFR	Differences from dsPIC30F1010/202X	Data Sheet Reference
PTCON	The Synchronous Source Selection (SYNCSRC) bits in the PWM Time Base Control register have been reduced to 2 bits.	**Section 14.0 "High-Speed PWM"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318)
PTPER	The PWM Master Time Base register has been extended to a full 16-bit time-base register.	
PHASEx	The PWM Phase Shift Value register has been extended to a full 16-bit phase-shift register.	
DTRx	The PWM Dead-Time register has been extended to a 14-bit dead-time register.	
ALTDTRx	The PWM Alternate Dead-Time register has been extended to a 14-bit alternate dead-time register.	
TRGCONx	The Trigger Output Divider (TRGDIV) bits in the PWM Trigger Control register have been extended to 3 bits to accommodate additional trigger events.	
FCLCONx	Four changes have been made to the PWM Fault Current-Limit Control register. 1. The Current-Limit Control Signal Source Select for PWM Generator # (CLSRC) bits have been extended to four bits providing more functionality. 2. The Current-Limit Polarity for PWM Generator # (CLPOL) bit has been shifted to the bit 9 location. 3. The Current-Limit Mode Enable for PWM Generator # (CLMODE) bit has been shifted to the bit 8 location. 4. The Fault Control Signal Source Select for PWM Generator # (FLTSRC) bits have been extended to four bits providing more functionality.	

HIGH-SPEED 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADC module on the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices has been upgraded to support a 4 Msps conversion rate supported by two Successive Approximation Registers (SARs). Devices with one SAR can achieve a 2 Msps conversion rate. Refer to the device variant table of the specific data sheet for details on which devices have one or two SARs.

The Auxiliary clock provides the clock source for the ADC module. The A/D Conversion Clock Divider Select (ADCS) bits in the A/D Control (ADCON) register, should be used to generate the desired ADC Clock (TAD). Refer to **44.3 "ADC Configuration"** of **Section 44. "High-Speed ADC"** (DS70321) in the *"dsPIC33F Family Reference Manual"* for details.

The voltage reference level of the input voltage is 3.3V for dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. The last ADC level, 1023, of the 10-bit ADC, corresponds to the input voltage of 3.3V. Appropriate changes to the analog circuitry need to be made by the user to accommodate the maximum input voltage reference level limit of 3.3V. Other changes in the ADC module are listed in Table 4.

TABLE 4: SFR CHANGES FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 HIGH-SPEED 10-BIT ADC MODULE

Differences from dsPIC30F1010/202X		Data Sheet Reference
The A/D Conversion Clock Divider Select (ADCS) bits in the A/D Control Register have been upgraded to use the clock divider for low- and high-frequency ADC input clocks, as shown below. This feature can be controlled by using the Enable Slow Clock Divider (SLOWCLK<12>) bit (the user must select the appropriate ADCS value to achieve the desired ADC clock rate).		**Section 18.0 "High-Speed 10-bit Analog-to-Digital Converter (ADC)"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318)
dsPIC30F1010/202X ADCS<2:0> 000 = FADC/4 001 = FADC/6 010 = FADC/8 011 = FADC/10 100 = FADC/12 101 = FADC/14 110 = FADC/16 111 = FADC/18	dsPIC33FJX06GSX0X ADCS<2:0> If SLOWCLK = 1 000 = FADC/1 001 = FADC/2 010 = FADC/3 011 = FADC/4 100 = FADC/5 101 = FADC/6 110 = FADC/7 111 = FADC/8 If SLOWCLK = 0 000 = FADC/3.5 001 = FADC/4 010 = FADC/4.5 011 = FADC/5 100 = FADC/5.5 101 = FADC/6 110 = FADC/6.5 111 = FADC/7	

TABLE 4: SFR CHANGES FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 HIGH-SPEED 10-BIT ADC MODULE (CONTINUED)

<table>
<tr><th colspan="2">Differences from dsPIC30F1010/202X</th><th>Data Sheet Reference</th></tr>
<tr><td colspan="2">• The Trigger Source Selection (TRGSRCx) bits in the A/D Convert Pair Control registers have been changed.
• The PWM trigger name has been updated to PWM Generator x Primary Trigger from PWM Generator x Trigger.
• The TRGSRC bits associated with Timer2 Period Match Trigger have been changed to 0b11111.
• The TRGSRC bits associated with PWM Generator x Fault ADC Trigger have been removed.
• The PWM Generator x Current-Limit ADC Trigger can also be used for PWM Generator x Fault ADC Trigger.
• Also, in order to use the external faults the I/O pins must be remapped to ‘Fault Input to PWM x’ function using the Peripheral Pin Select feature.</td><td rowspan="2">Section 18.0 “High-Speed 10-bit Analog-to-Digital Converter (ADC)” in the “dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet” (DS70318)</td></tr>
<tr><td>dsPIC30F1010/202X
TRGSRCx<4:0>

00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM Generator 1 trigger selected
00101 = PWM Generator 2 trigger selected
00110 = PWM Generator 3 trigger selected
00111 = PWM Generator 4 trigger selected
01100 = Timer1 Period match
01101 = Timer2 Period match
01110 = PWM Generator 1 Current-limit ADC trigger
01111 = PWM Generator 2 Current-limit ADC trigger
10000 = PWM Generator 3 Current-limit ADC trigger
10001 = PWM Generator 4 Current-limit ADC trigger
10110 = PWM Generator 1 Fault ADC trigger
10111 = PWM Generator 2 Fault ADC trigger
11000 = PWM Generator 3 Fault ADC trigger
11001 = PWM Generator 4 Fault ADC trigger</td><td>dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04
TRGSRCx<4:0>

00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM Generator 1 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
01000 = Reserved
. . .
01100 = Timer1 period match
01101 = Reserved
01110 = PWM Generator 1 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10010 = Reserved
. . .
10110 = Reserved
10111 = PWM Generator 1 Current-limit ADC trigger
11000 = PWM Generator 2 Current-limit ADC trigger
11001 = PWM Generator 3 Current-limit ADC trigger
11010 = PWM Generator 4 Current-limit ADC trigger
11011 = Reserved
. . .
11111 = Timer2 period match</td></tr>
</table>

HIGH-SPEED ANALOG COMPARATOR

The Analog Comparator reference voltage on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices has two internal voltage references: AVDD/2 and INTREF.

The high range voltage of AVDD/2 is 1.65V because the AVDD is 3.3V for dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. If the RANGE bit in the Comparator Control (CMPCONx) register is selected, AVDD/2, which is 1.65V, provides the high range comparator reference.

The EXTREF pin can be selected as the comparator reference voltage by setting the EXTREF bit to '1' in the CMPCONx register. The maximum voltage reference that can be used on the EXTREF pin is AVDD – 1.6V.

The Comparator Reference Voltage Select (CMREF) bits in the Comparator DAC Control (CMPDACx) register depends on an AVDD of 3.3V in the high range mode. For more information refer to **Section 19.0 "High-Speed Analog Comparator"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

If the analog comparator is used as an external PWM Fault or a Current-limit source, a virtual pin (ACMPx) must be mapped to the 'Analog Comparator Output x' function using the Peripheral Pin Select feature. Additionally, the same virtual pin needs to be remapped to 'Fault Input to PWMx' using the Peripheral Pin Select feature. For more information on virtual pins for the Peripheral Pin Select feature, refer to the **Section 9.0 "I/O ports"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

A DAC output pin is provided on the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices, which can be mapped to only one comparator DAC. This is done by setting the DACOE bit to '1' in the CMPCONx register. It must be ensured in software that no more than one DACOE bit is set to '1'.

SPECIAL FEATURES

Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The Configuration registers, which are updated with new bits for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices are as follows:

- Boot Segment Program Flash Code/Write Protection (FBS)
- General Segment Code/Write Protection (FGS)
- Oscillator Select (FOSCSEL)
- Oscillator Control (FOSC)
- Watchdog Timer Configuration (FWDT)
- Power-on Reset Configuration (FPOR)
- Debugger Configuration (FICD)

The user must configure the appropriate bits in the Configuration bits registers along with proper configuration of the oscillator configuration registers to achieve the desired functioning of the device clock.

The changes in the Oscillator Control (FOSC) register is provided in Table 5. For more information on the specifics of new registers and changes to the existing registers, refer to **Section 20. "Special Features"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318).

TABLE 5: CHANGES FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CONFIGURATION BIT REGISTERS

Address	Register	Differences from dsPIC30F1010/202X	Data Sheet Reference
0xF80008	FOSC	The Peripheral Pin Select Configuration (IOL1WAY) bit has been added in the place of the Frequency Range Select for FRC and PLL (FRANGE) bit in the Oscillator Control Register (FOSC). The IOL1WAY bit allows a single or multiple peripheral pin select reconfiguration.	**Section 20. "Special Features"** in the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318)
0xF8000C	FPOR	The Brown-out Reset Enable (BOREN) bit, which enables and disables the Brown-out Reset (BOR) feature, has been added to the Power-on Reset (FPOR) register.	

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Fax: 86-21-5407-5066

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Fax: 86-755-8203-1760

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India - Pune
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Korea - Seoul
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Malaysia - Kuala Lumpur
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Malaysia - Penang
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