
PolarFire EDAC and Scrubbing of Fabric RAMs

Introduction

The CoreEDAC IP generates Error Detection And Correction (EDAC) circuitry for both internal (on-chip) and external RAM blocks. The user data is fed to the EDAC encoder, which calculates the parity bits and appends these to the user data, forming a codeword. The codeword is stored into the RAM. During user read, the read codeword is decoded first, which detects and corrects errors (if any), discards parity bits, and outputs the corrected user data word. Scrubbing periodically checks every memory location using the ECC decoder. If a location contains a corrupted word, the decoder detects and corrects the word. The scrubbing circuitry then writes the corrected word back to the same location. To provide normal access to the RAM and prevent decreasing performance, scrubbing is only done during idle periods. The scrubbing circuitry sets a proper write address and write enable signals, writing the corrected codeword back to the RAM. Writeback occurs only upon detecting an error.

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1. EDAC and Scrubbing of Fabric RAMs

To program the application design note, use the following option:

Using the job file: To program the device using the job file provided along with the design files, see [5. Appendix 1: Programming the Device Using FlashPro Express](#).

1.1 Design Requirements

The following table lists the hardware and software requirements for this application note design.

Table 1-1. Design Requirements

Requirement	Version
Operating System	64-bit Windows® 10
Hardware	
PolarFire® Evaluation Kit (MPF300-EVAL-KIT) 12V/5A AC power adapter and cord USB 2.0A to mini-B cable for UART and programming	Rev D or later
Software	
Libero® SoC	Refer to the <code>readme.txt</code> file provided in the design files for the software versions used with this reference design.
FlashPro Express	



Important: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

1.2 Prerequisites

Before you start, perform the following steps:

1. Download the design files from:
www.microchip.com/en-us/application-notes/AN4895
2. Download and install Libero SoC from: [Libero SoC Documentation](#)

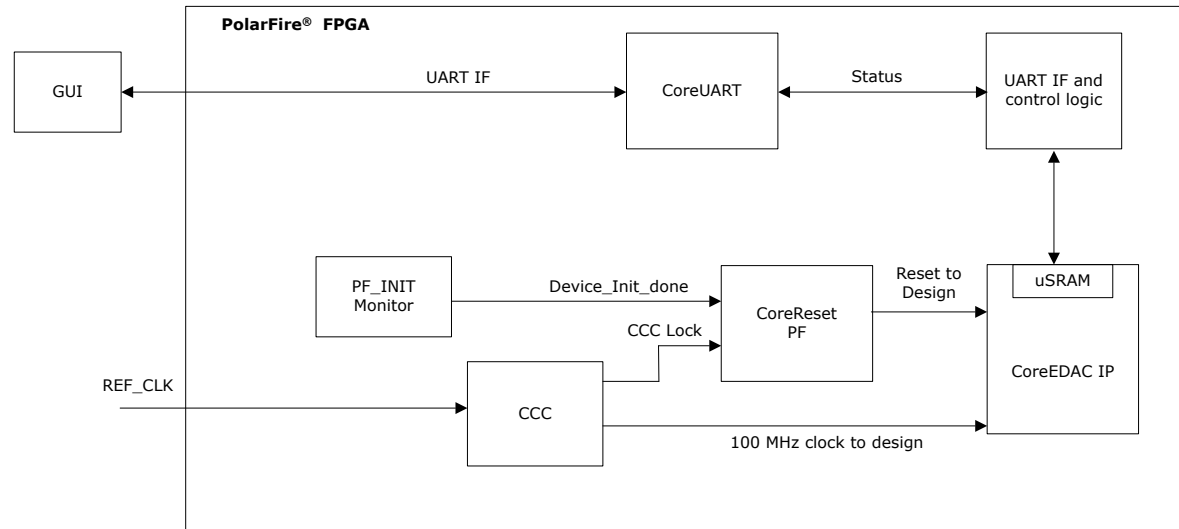
1.3 Application Note Design

EDAC detects a 1-bit error or 2-bit error when data is read from the memory. If EDAC detects the 1-bit error, the EDAC controller corrects the same error bit. If EDAC is enabled for all the 1-bit and 2-bit errors, corresponding error counters get incremented. To demonstrate this, an error is introduced manually and detection and correction is observed. The application note design shows how to use CoreEDAC IP with internal μ SRAMs for the following:

- Detect and correct single-bit errors
- Detect double-bit errors
- Perform auto memory scrubbing and on-demand memory scrubbing

The following figure shows the block diagram of the design.

Figure 1-1. Block Diagram



You can use the similar approach for on-chip LSRAMs. This application note design does not demonstrate the use of EDAC with external memories.

The following steps describes how to use CoreEDAC IP with on-chip LSRAMs:

1. Configure CoreEDAC IP to use internal μ SRAM blocks and set the memory depth to 1 kb. To induce an error into the memory, enable error inject test port. To correct the errors, enable scrubbing logic.
2. Use the user RTL logic to write and read 1 kb data to and from the memory. This logic also monitors the status flags set by the CoreEDAC controller to monitor the scrubbing requests and to detect single-bit and double-bit errors.
3. Universal Asynchronous Receiver and Transmitter (UART) is used to interface with GUI to provide commands to the design and display the error counters and status flags.
4. The application note design performs the following operations using the GUI.
 - **Memory Write:** Initializes 1 kb μ SRAM memory with incremental data
 - **Memory Read:** Reads 1 kb data from μ SRAM memory to verify the memory is initialized. Initially, the memory is not corrupted; hence the error counters must be zero.
 - **Inject Error:** Injects Single-bit or double-bit error in memory locations
 - **Memory Read:** Reads the data from corrupted μ SRAM memory
 - **Single-bit error:** The relevant counter is incremented and the corrected data is available
 - **Double-bit error:** The relevant counter is incremented and the erroneous data is available
 - **Memory Scrub:** Performs memory scrubbing and corrects single bit errors in the μ SRAM memory
 - **Single Memory Write:** You can access the entire 1 kb memory through this operation. You can provide the memory address and the data to be written during this operation.
 - **Single Memory Read:** You can access the entire 1 kb memory through this operation. You can provide the memory address and the data to be read during this operation.
 - **Loop Test:** You can use this option to perform the operations from step to step in one click

1.3.1 Design Description

This application note design involves implementation of the following tasks:

- Writing data to μ SRAM
- Reading data from μ SRAM
- Corrupting one or two bits
- Reading the data



Important: In the case of a 1-bit error, the EDAC controller corrects the error. In the case of a 2-bit error, the EDAC controller does not correct the error.

This application note design implements the following tests:

- [1.3.1.1. Loop Test](#)
- [1.3.1.2. Manual Test](#)



Important: These tests are applicable to both 1-bit and 2-bit errors.

1.3.1.1 Loop Test

The PolarFire FPGA executes the loop test when it receives the loop test command from the GUI. Initially, all the error counters and EDAC related registers are placed in the RESET state.

For each iteration, following steps are executed:

1. 1 Kb incremental data is written into the memory.
2. 1 Kb data is read from the memory.
3. 50 single bit errors are injected into the memory.
4. The memory is read and the error count is displayed.
5. Scrubbing is performed on the memory and the scrubbing correction count is displayed.
6. 1-bit or 2-bit error detection and correction is sent to the GUI.

1.3.1.2 Manual Test

This method allows manual testing for enabling or disabling EDAC and the write or read operation. Use this method to introduce 1-bit or 2-bit errors to any location within the μ SRAM. Enable the EDAC and write the data to the specified address using the GUI fields. Disable the EDAC and write 1-bit or 2-bit corrupted data to the same address location. Enable the EDAC and read the data from the same address location. The corresponding error counter is displayed on the GUI. The GUI Serial Console logs all the actions performed in PolarFire.

As shown in the following figure, the CoreEDAC IP is configured with the following options:

- Internal μ SRAM blocks are selected and the memory depth is set to 1 Kb
- Error injection is enabled for inducing errors into the memory
- Scrubbing logic is enabled for correcting errors
- Triple Redundancy is also enabled for the generation of three independent sets of the EDAC circuitry and the majority vote logic for protecting the EDAC from the soft errors
- Scrubber is enabled to detect the data errors and repair them

Figure 1-2. CoreEDAC IP Configuration

Configuring C0_COREEDAC_C0_0 (COREEDAC 2.11.107)

Configuration

RAM block: Internal

User Data

Width (bits): 8 Encoded width (bits): 13

Depth (words): 1024 Approx. Max RAM depth: 245760

Click on "Check Configuration" to check availability of Depth entered

Use Triple Redundancy Use single Read/Write clock Create error injection test port

Encoder / Decoder

Limit encoder latency to: 0 Clock cycles Actual Latency: 0 Clock cycles

Limit decoder latency to: 0 Clock cycles Actual Latency: 0 Clock cycles

Provide RAM read address with the data

Error Scrubber

Use scrubber to detect data errors Allow scrubber to repair detected errors

Min Refresh Period: 10240 Read Clocks Refresh Period: 1.02E+006 Read Clocks

Start Address: 0 Binary Divider Width: 10

End Address: 1023 Timeout: 1000

Protected RAM (generated)

RAM Type: Micro SRAM

Initialize RAM with 0 Use pipeline register for read data

Testbench: User

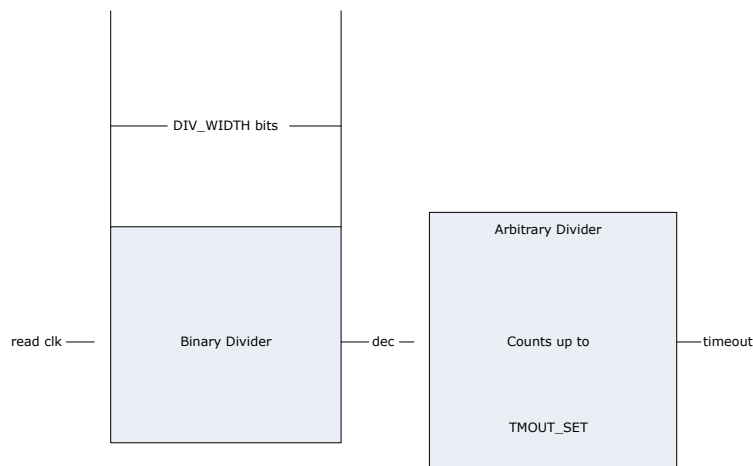
License: RTL

Check Configuration OK Cancel

1.3.1.3 Scrubbing Refresh Period

The refresh period defines how often the scrubbing session runs. The following figure shows the block diagram of the refresh period timer.

Figure 1-3. Refresh Period Timer



The timer is driven by the RCLK signal. The binary divider that has a configurable bitwidth of DIV_WIDTH , generates a relatively slow signal, dec . The frequency of the dec signal equals the frequency of the read clock divided by 2^{DIV_WIDTH} . The dec signal serves as an input to the configurable arbitrary divider. It divides dec frequency by arbitrary number $TMOUT_SET$. As a result, the circuitry generates a timeout output signal once per $TMOUT_SET \times 2^{DIV_WIDTH}$ RCLK periods.

The refresh period must be more than 10 times the scrubbing time that is, DIV_WDTH and TMOUT_SET parameters must satisfy the following condition:

$$\text{TMOUT_SET} * 2^{\text{DIV_WDTH}} > 10 * (\text{SCRUB_AMAX} - \text{SCRUB_AMIN})$$

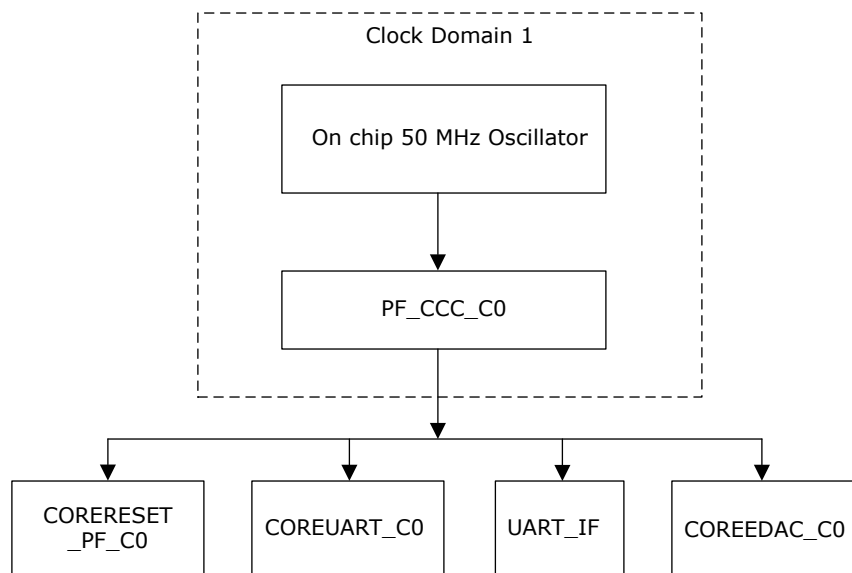
The timeout signal initiates another scrubbing session. As the user access takes priority over scrubbing, there might be an exception.

For more information about setting the refresh period timer, scrubbing, and scrubbing refresh period, see [CoreEDAC_HB](#). The Maximum User Word Sizes Fault-Tolerant RAM Accommodates table in this handbook explains DIV_WDTH, TMOUT_SET, SCRUB_AMAX, and SCRUB_AMIN parameters.

1.4 Clocking Structure

In this design, there is one clock domain. The on-board 50 MHz crystal oscillator is connected to the PF_CCC block which generates 100 MHz clock that provides clock source to CORERESET_PF, COREUART, UART_IF, and COREEDAC modules. The following figure shows the clocking structure of the design.

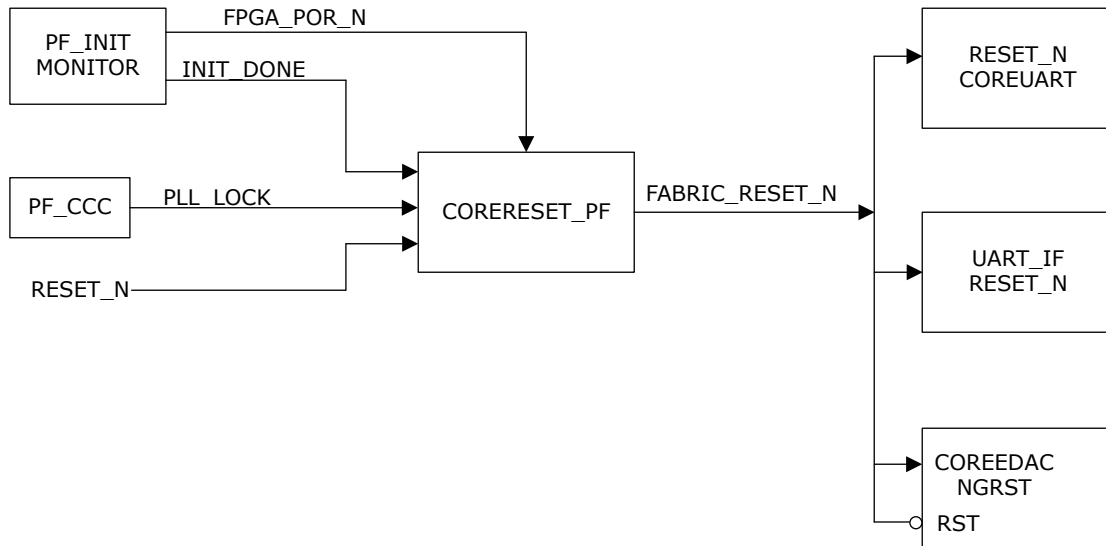
Figure 1-4. Clocking Structure



1.5 Reset Structure

In this design, the reset signal of COREUART, UART_IF, and COREEDAC blocks are issued using the CORERESET_PF module. The CORERESET_PF module releases active low reset when the PF_CCC lock and PF_INIT_MONITOR INIT_DONE are asserted. The following figure shows the reset structure of the design.

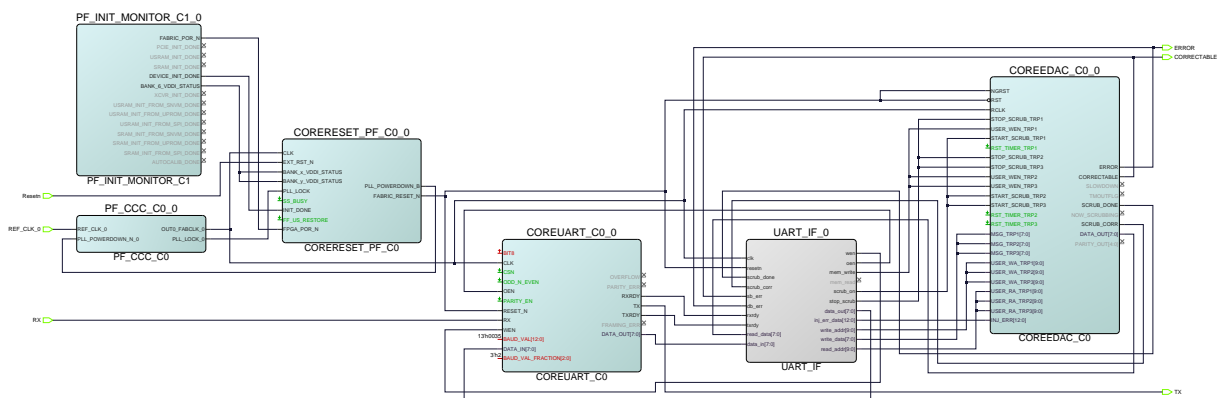
Figure 1-5. Reset Structure



1.6 Hardware Implementation

The following figure shows the implementation of PolarFire EDAC and scrubbing design in Libero SoC.

Figure 1-6. Hardware Implementation



2. Setting Up the Hardware

To set-up the hardware, perform the following steps:

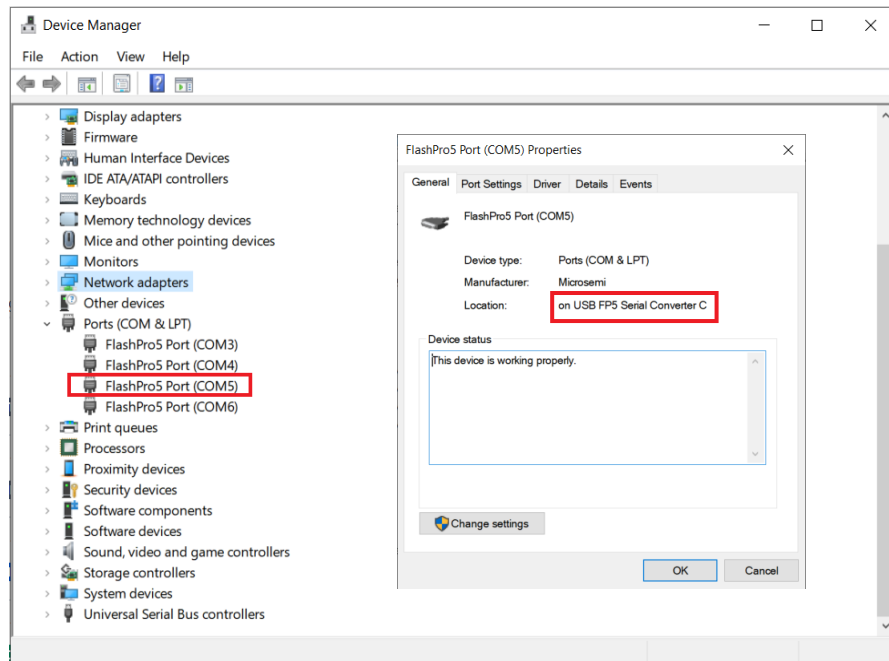
1. Ensure that the following Jumper Settings are set on the board. The following table lists the descriptions of the Jumper pins.

Table 2-1. Jumper Settings

Jumper	Description	Default
J18, J19, J20, J21, and J22	Short pin 2 and 3 for programming the PolarFire® FPGA through FTDI	Closed
J28	Short pin 1 and 2 for programming through the on-board FlashPro5	Open
J26	Short pin 1 and 2 for programming through the FTDI SPI	Closed
J4	Short pin 1 and 2 for manual power switching using SW3	Closed
J12	Short pin 3 and 4 for 2.5V	Closed

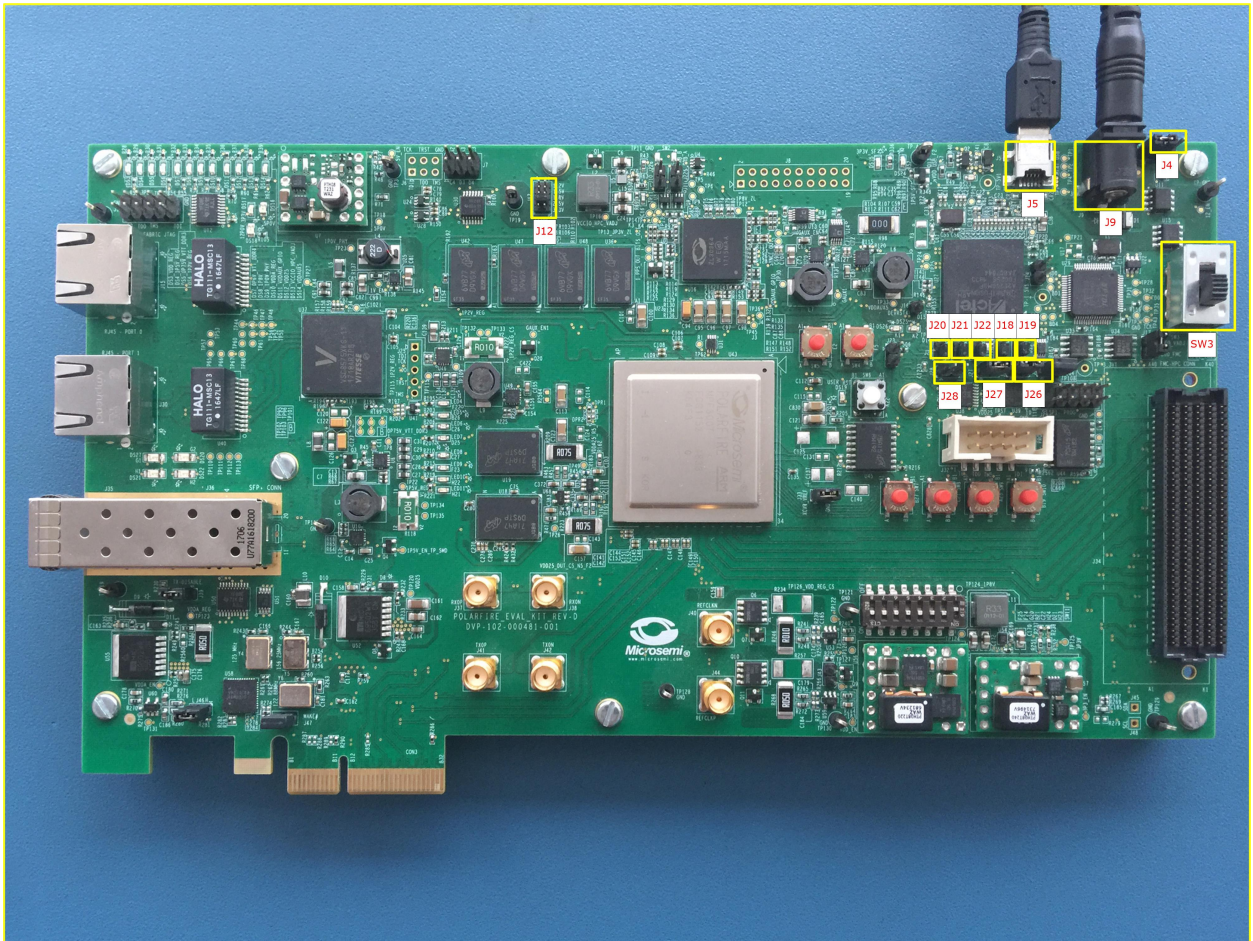
2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the Host PC to J5 (FTDI port) on the board.
4. Power on the board using the SW3 slide switch.
5. Ensure that the USB to UART bridge drivers are automatically detected. You can verify this in the device manger of the host PC.
6. As shown in following figure, the port properties of COM5 show that it is connected to USB Serial Converter C. Hence, COM5 is selected in this example. The COM port number is system specific.

Figure 2-1. Device Manager



The following figure shows the PolarFire board setup.

Figure 2-2. PolarFire Board Setup



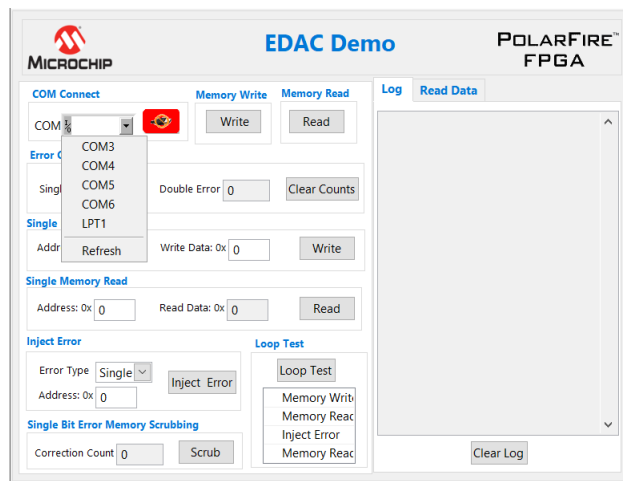
3. Running the Demo

The PolarFire EDAC application is a simple Graphic User Interface (GUI) that runs on the host PC to communicate with the PolarFire Device. Before running the demo, ensure to set up the hardware and program the device using FlashPro Express. For more information, see [2. Setting Up the Hardware](#) and [5. Appendix 1: Programming the Device Using FlashPro Express](#).

To run the EDAC demo, perform the following steps:

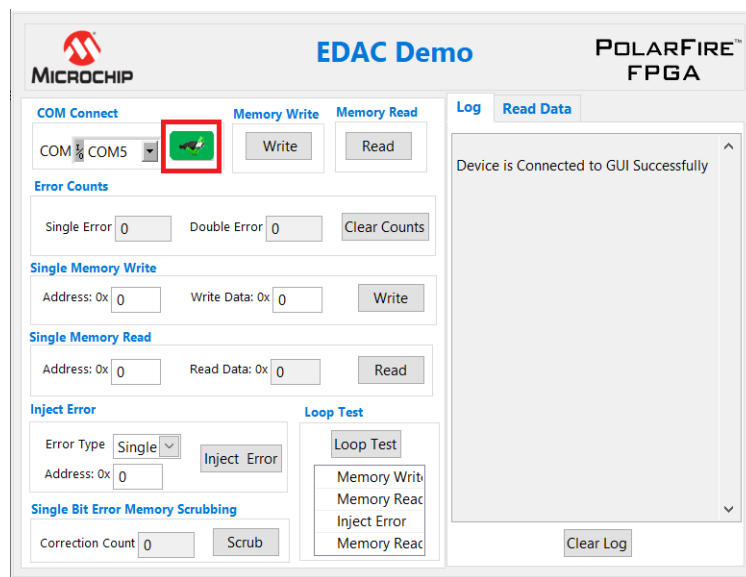
1. Run the setup.exe file available at the following design files location:
<\$Download_Directory>\mpf_an4895_v2022p3_df\EDAC_PF_GUI\setup.exe
2. Follow the installation wizard to install the GUI application.
3. After installing the GUI, invoke the EDAC GUI from **All Programs > EDAC Demo > EDAC PF GUI**. Navigate to **COM Connect** and select the COM port.
4. Open the PolarFire EDAC GUI and select the COM port.

Figure 3-1. Selecting the COM Port



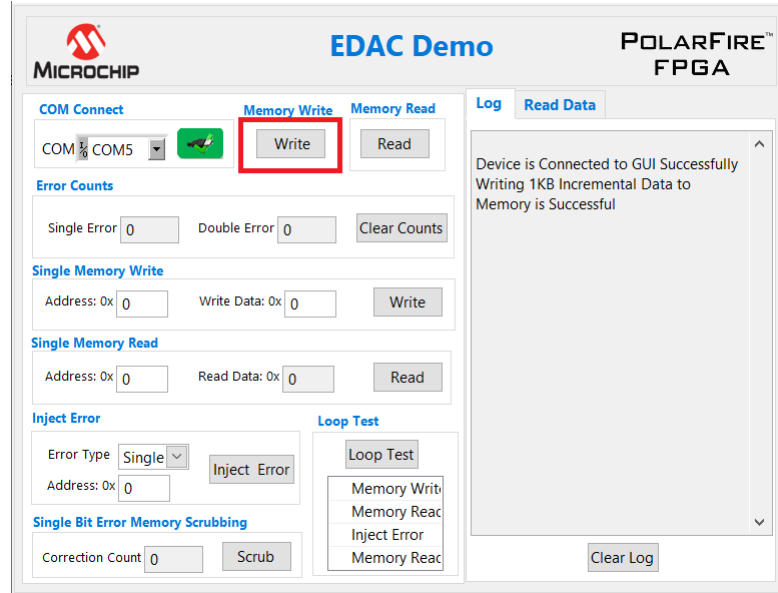
5. After selecting the COM port, click **Connect** icon as highlighted in the following figure. The log window displays connection successful message.

Figure 3-2. Device Connection Successful Message



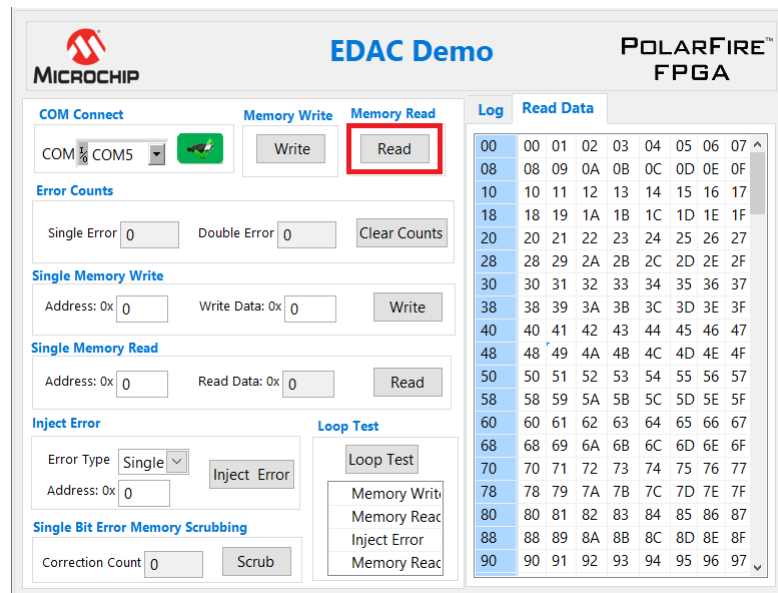
- Click **Write** as highlighted in the following figure to write 1 kb incremental data into the memory. The log window displays the write successful message.

Figure 3-3. Write Incremental Data to Memory



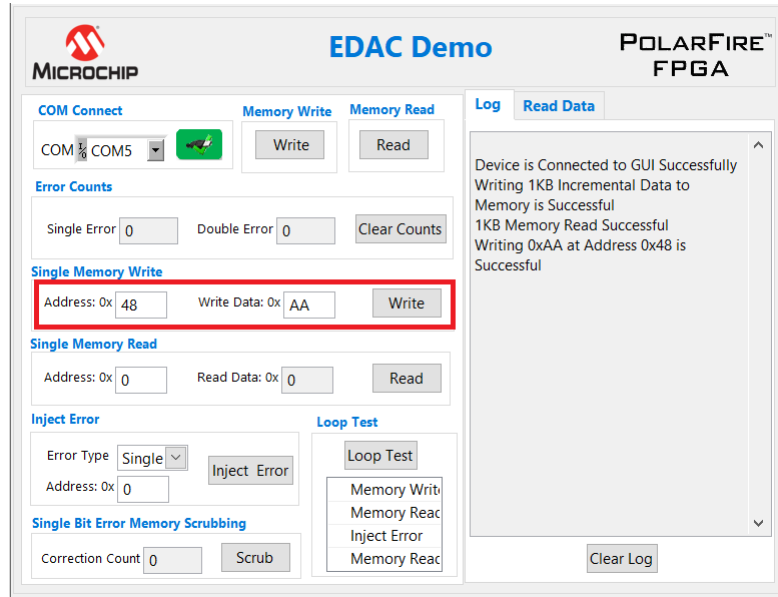
- Click **Read** as highlighted in the following figure to read 1 kb data. The read data is displayed in the **Read Data** tab and the single bit errors and double bit errors are displayed in their respective fields. Also, the **log** window displays the read successful message.

Figure 3-4. Read Incremental Data from Memory



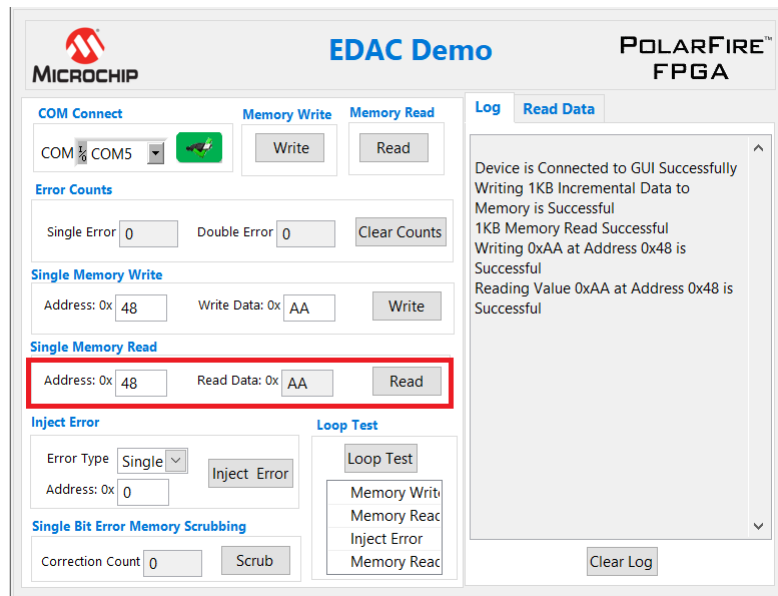
- For a single memory location, enter the address and data to be written and click **Write** as highlighted in the following figure.

Figure 3-5. Writing 0xAA at Address 0x48



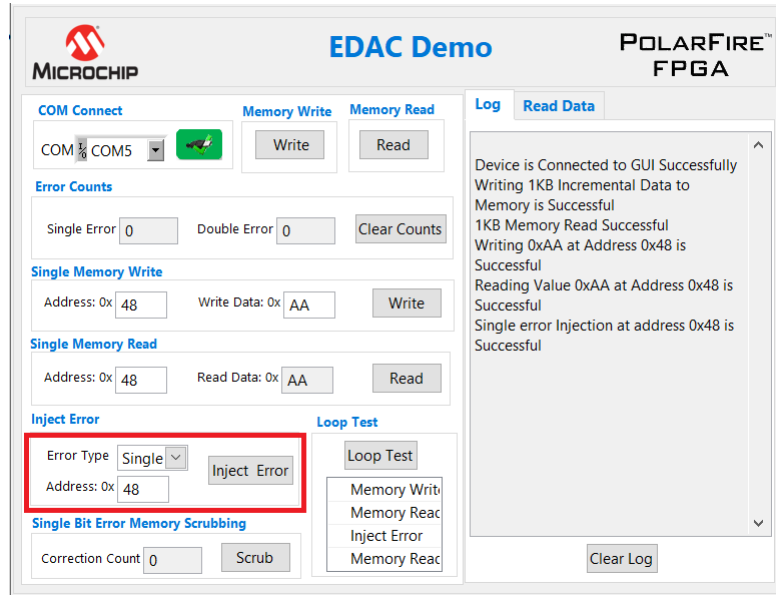
9. For reading a single location, provide the memory address and click **Read** as highlighted in the following figure. The corresponding data is displayed in the GUI.

Figure 3-6. Reading Value at 0xAA at Address 0x48



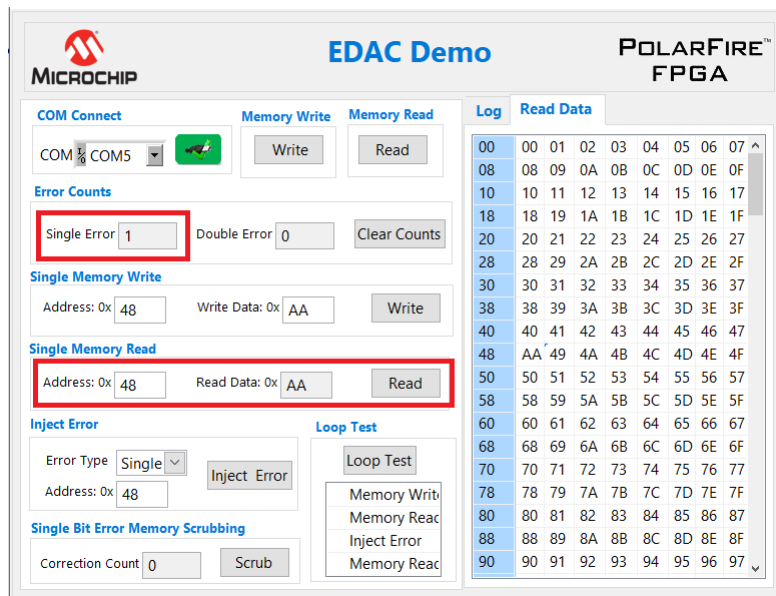
10. For injecting a single bit error, provide the memory address and click **Inject Error** as highlighted in the following figure.

Figure 3-7. Single Error Injection at Address 0x48



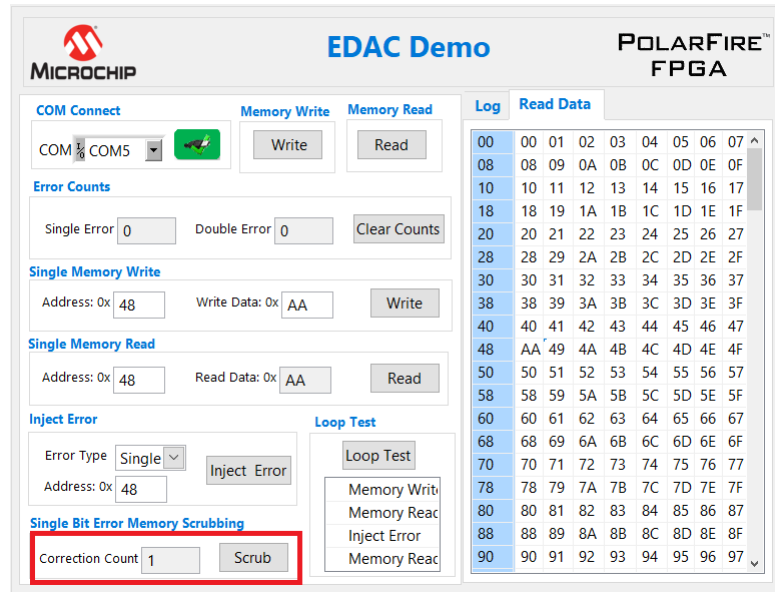
11. After Injecting a single bit error, click **Read** as highlighted in the following figure. The Single Error count is updated to 1.

Figure 3-8. Single Error Count



12. The Memory Scrubbing detects and corrects single bit errors. Click **Scrub** as highlighted in the following figure to perform scrubbing on the memory. After you complete the scrubbing, the **Correction Count** displays the number of single bit errors corrected during scrubbing.

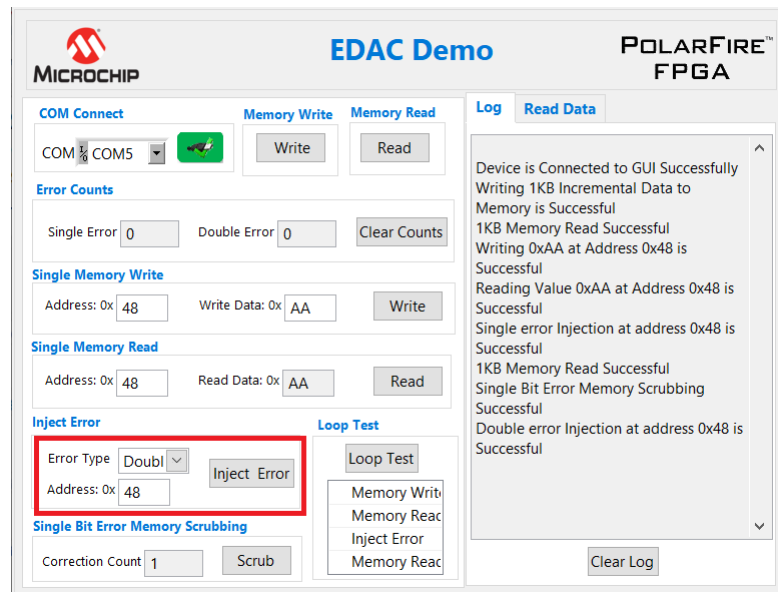
Figure 3-9. Single Bit Error Memory Scrubbing



Important: One single bit error is introduced in step 11. Hence, during scrubbing, the single bit error is corrected, and the correction value is updated to “1”.

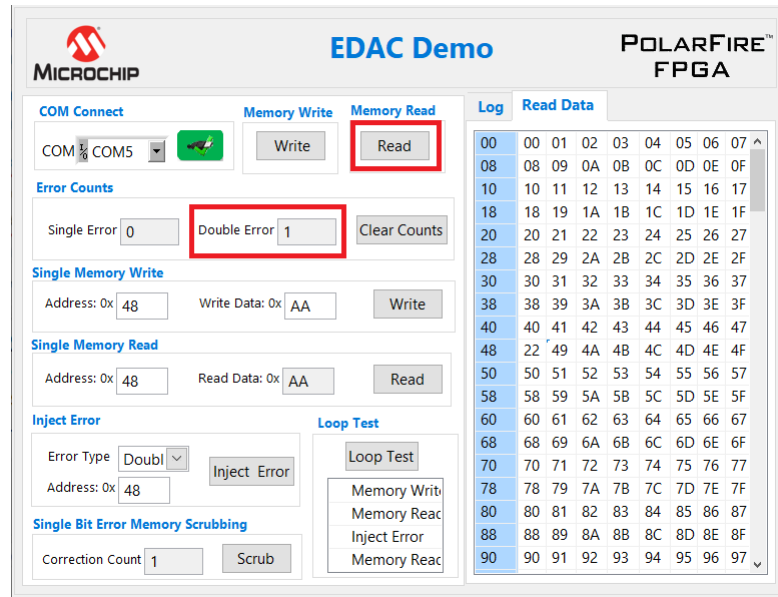
- For injecting Double bit error, select the **Error Type** to **Double**, provide the memory address and click **Inject Error** as highlighted in the following figure.

Figure 3-10. Double Error Injection at Address 0x48



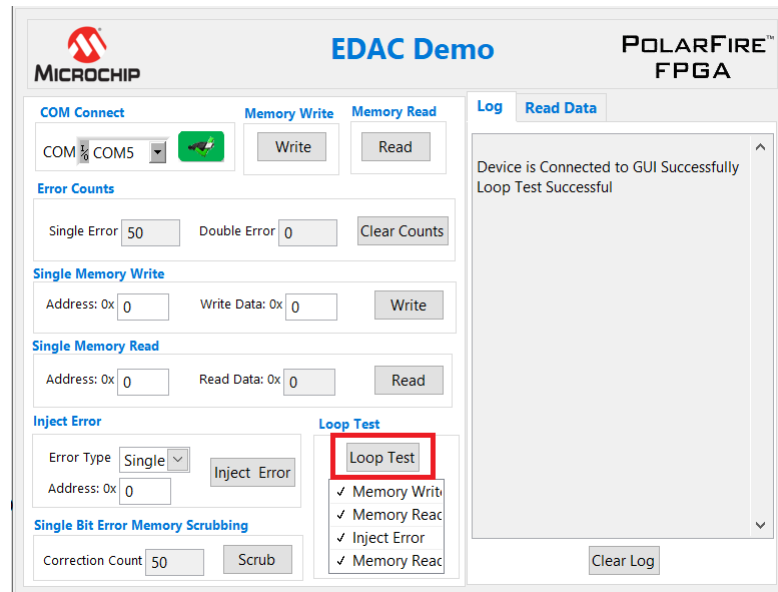
- Click **Read** as highlighted in the following figure. The **Double Error** is updated to “1”, indicating a double bit error exists in the memory. The **Single Error** is zero because the single bit error is corrected during scrubbing as mentioned in the previous step.

Figure 3-11. Double Error Count



15. Click **Loop Test** as highlighted in the following figure. The loop test performs the following operations.
 - Writes 1 kb incremental data into the memory
 - Reads 1 kb data from the memory
 - Injects 50 single bit errors into the memory
 - Reads the memory and displays the error count
 - Performs scrubbing on the memory and displays the scrubbing correction count

Figure 3-12. Loop Test



This concludes the PolarFire EDAC Demo.

4. Conclusion

This demo highlights the EDAC capabilities of the PolarFire μ SRAM memories. The 1-bit error or 2-bit error are introduced manually. 1-bit error correction and 2-bit error detection is observed using a GUI.

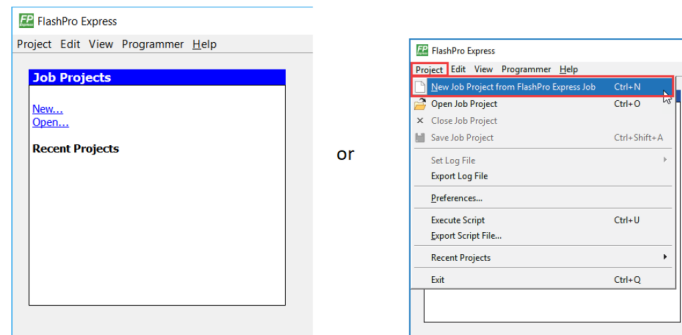
5. Appendix 1: Programming the Device Using FlashPro Express

This chapter describes how to program the PolarFire device with the job file using Flashpro Express. The job file is available at the following design files folder location: <\$Download_Directory>\mpf_an4895_v2022p3_df\Programming_Job

To program the device using the FlashPro Express, perform the following steps:

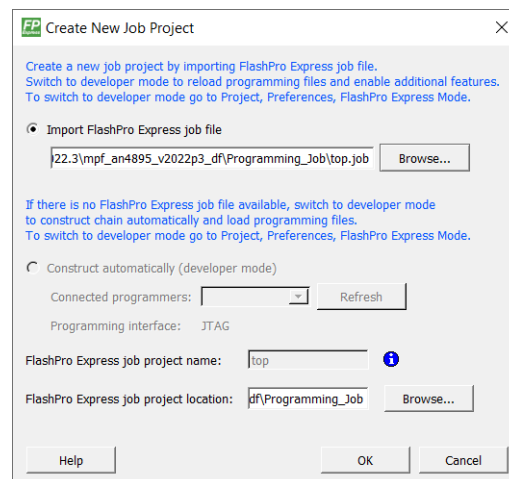
1. On the host PC, start the FlashPro Express software from its installation directory.
2. To create a new project, perform one of the following: Click **New** in the **Job Projects** panel. Select **Project** on the task bar. Click **New Job Project from FlashPro Express Job**.

Figure 5-1. FlashPro Express Job Project



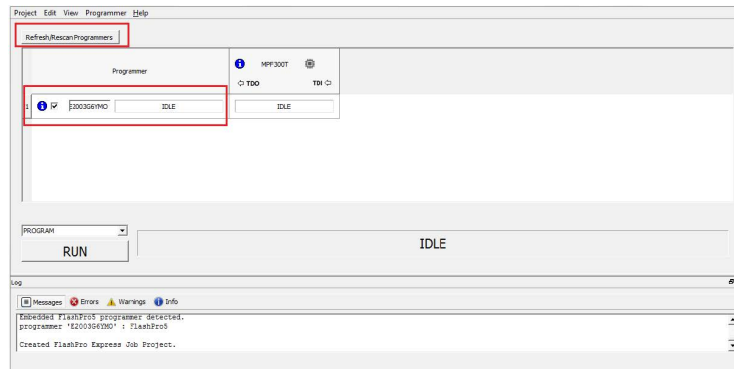
3. Enter the following in the New Job Project from FlashPro Express Job dialog box:
 - **Programming job file:** Click **Browse** and navigate to the location where the job file is located and select the file. You can use `Programming_Job` folder for your job project. The default location is: <\$Download_Directory>\Programming_Job.
 - **FlashPro Express job project location:** Select **Browse** and navigate to the location where you want to save the project.

Figure 5-2. New Job Project from FlashPro Express Job



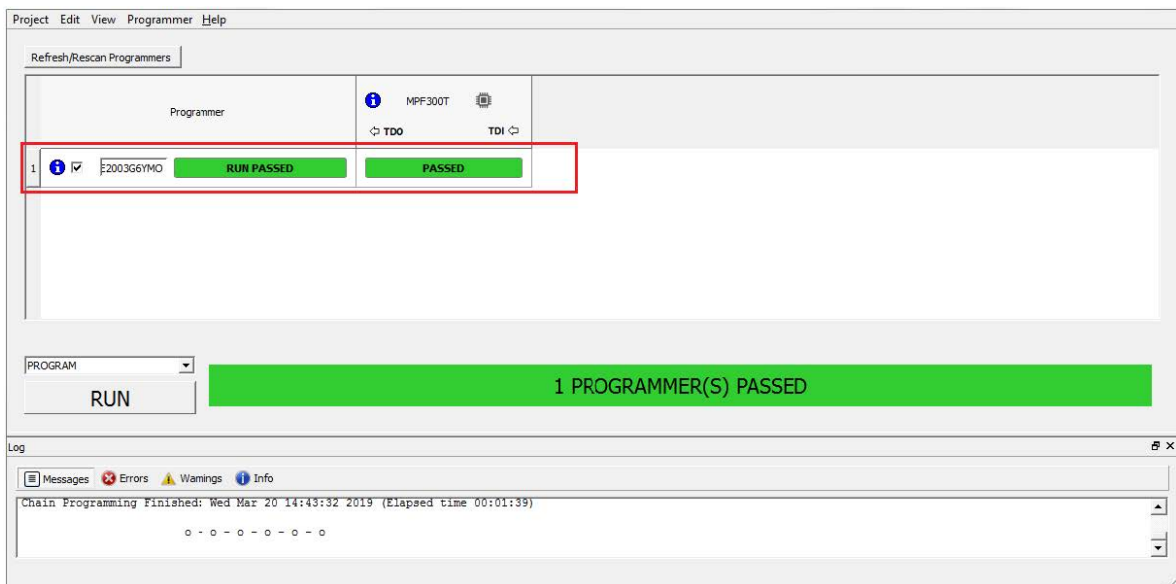
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The FlashPro Express window appears, as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

Figure 5-3. Programming the Device



- Click **RUN** to program the device. When the device is programmed successfully, a **RUN PASSED** status is displayed, as shown in the following figure.

Figure 5-4. FlashPro Express—RUN PASSED



- Close FlashPro Express (**Project > Exit**).

The PolarFire device is programmed.

6. Appendix 2: Running the TCL Script

TCL scripts are provided in the design files folder under directory `TCL_Scripts`. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, perform the following steps:

1. Launch the Libero software.
2. Select **Project > Execute Script....**
3. Click **Browse** and select `script.tcl` from the downloaded `TCL_Scripts` directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within `TCL_Scripts` directory.

For more information about TCL scripts, see `mpf_an4895_v2022p3_df/TCL_Scripts/readme.txt`

For more information on TCL commands, see [Tcl Commands Reference Guide](#). Contact Microchip Technical Support for any queries encountered, while running the TCL script.

7. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
B	04/2023	The following is the list of changes in revision B of the document: <ul style="list-style-type: none"> • Updated Figure 1-1. • Updated Figure 1-2.
A	02/2023	The following is the list of changes in revision A of the document: <ul style="list-style-type: none"> • Migrated the document to the Microchip template. • Updated the document number to DS00004895A from 51900491. • Updated Figure 1-6. • Updated all images in 3. Running the Demo. • Updated the design filepath and <code>.job</code> filepath, and TCL script filepath throughout the document.
2.0	—	Added 6. Appendix 2: Running the TCL Script
1.0	—	The first publication of this document.

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