

Application Note
VSC8211 in Synchronous Ethernet Applications

July 2008



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1 **Revision History**

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 **Revision 1.0**

Revision 1.0 was the first release of this document. It was published in July 2008.

2 Introduction

The growth of Ethernet in telecommunication applications has created a demand for Ethernet PHYs capable of supporting Synchronous Ethernet, as described in the ITU-T G.8261 and IEEE 1588 standards. The purpose of this application note is to assist a system developer or high-speed board designer in using the VSC8211 Gigabit Ethernet PHY for Synchronous Ethernet applications.

2.1 Audience

The target audiences for this document are system engineers and high-speed board designers interested in using the VSC8211 for Synchronous Ethernet applications.

2.2 References

- VSC8211 Datasheet.
- VSC8664 Datasheet.
- IEEE-802.3, CSMA/CD - Access Method and Physical Layer Specification.
- IEEE-802.3ah - Ethernet in the First Mile.
- IEEE-1588 - Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.
- ITU-T G.8261/Y.1361 - Timing and synchronization aspects in packet networks.

2.3 Terms and Abbreviations

Table 1 • Terms and Abbreviations

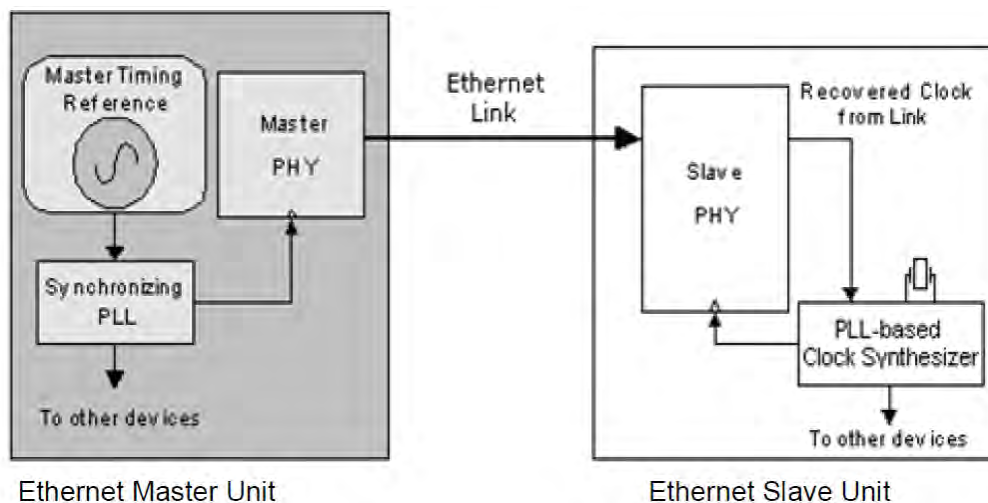
Term	Explanation
GMII	Gigabit Media Independent Interface
IEEE	Institute of Electrical and Electronics Engineers
ITU-T	International Telecommunications Union -Telecommunication Standardization Sector
LOS	Loss Of Signal
MAC	Media Access Control
MII	Media Independent Interface
PCS	Physical Coding Sublayer
PHY	PHYsical layer (device)
PMA	Physical Medium Attachment (sublayer)
RGMII	Reduced Gigabit Media Independent Interface
RTBI	Reduced Teb-Bit Interface (Gigabit only)

3 Synchronous Ethernet Overview

Modern 100-Megabit and 1-Gigabit per second Ethernet PHY devices are available, in both copper and optical physical layer variants, to enable system vendors to develop Synchronous Ethernet systems for the delivery of voice, video, and data in accord with ITU-T Recommendation G.8261/Y.1361. Unlike the older 10Base-T protocol with indeterminate pauses between frame transfers, the VSC8211 represents a new class of Ethernet PHYs that transmit data continuously, thereby making possible the necessary clock recovery needed for synchronous data transfer.

In order to achieve synchronization, one of the two linked parties must derive (recover) its clock from the signal received from the other to form a Master–Slave link connection, are as shown in the following figure. In this scheme the Ethernet link transmission includes a clock signal obtained from a master timing source (that is, primary reference clock), which may be recovered and passed along throughout an entire Ethernet network.

Figure 1 • Generic Synchronous Ethernet Scheme



The Master–Slave frequency lock sequence is achieved as follows:

1. Before the link between the two parties is established, the PLL-based Clock Synthesizer in the Slave unit must provide the Ethernet PHY device with a free-running clock, with a frequency offset and jitter in compliance with the IEEE 802.3 standard requirements. This initial reference clock enables the Slave unit to link up with the transmitting Master.
2. Once Ethernet linkage has been established, the Clock Slave starts deriving (recovering) its clock from the signal received from the Clock Master and in turn feeds the recovered clock to the Clock Synthesizer as the new reference.
3. The Clock Synthesizer locks onto the recovered clock and the PLL then distributes synchronized clocks throughout the board; this enables the entire Ethernet Slave unit to lock to the transmission clock of the relevant ports for the given frequency reference. This switching must occur smoothly enough to not disturb the existing Ethernet link or interfere in any way with the operation of the other ICs in the specific customer's design using the other clocks produced by the Clock Synthesizer.
4. If the established link disconnects, the same smooth switching must take place in the opposite direction.

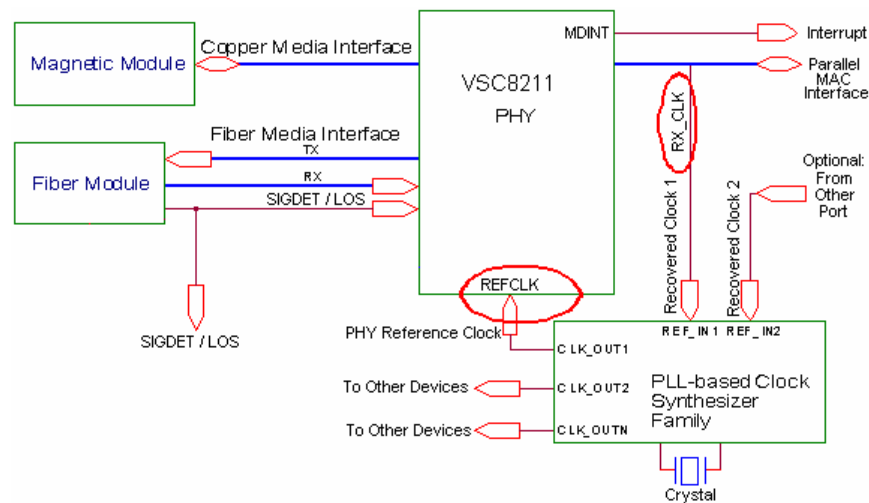
As an option, the multi-port Clock Slave device may simultaneously have several established Ethernet links, each potentially producing its own recovered clock. In this case the local system host must make a choice in selecting which of the received links to use for the Clock Synthesizer to lock onto, in accord with the requirements of the given application.

4 VSC8211-Based Synchronous Ethernet Scheme

An example of a VSC8211-based implementation of the above Synchronous Ethernet Scheme is as shown in the following figure. In this implementation a clock is recovered from either Copper or Fiber media by the VSC8211 and provided to an Ethernet MAC device connected over the parallel interface (RGMII, RTBI, GMII, and MII). An intelligent PLL-based Clock Synthesizer must be used to lock onto either of the two recovered clocks, with one selected as the primary and the other as the secondary reference. Here, the Clock Synthesizer must be capable of quickly switching to the secondary clock, whenever the primary clock disappears, and then switching back to the primary when it reappears.

Unlike Vitesse's newer VSC8664 PHY, the VSC8211 does not have a dedicated Fast Link Failure output pin to notify the system host whenever switching occurs (that is, either switching between the two recovered clocks or to a "free running" clock when both links are down). There are indirect methods of determining link failure with sufficient speed to accomplish this. The PHY Reference Clock, Recovered Clocks, and Fast Link Failure indication are described in the sections that follow.

Figure 2 • VSC8211-based Synchronous Ethernet clocking



4.1 Reference Clock (REFCLK) Input Requirements

4.1.1 Frequency Value

The PHY accepts reference clock frequency of either 25 MHz or 125 MHz.

4.1.2 Frequency Tolerance

To meet the IEEE and RGMII requirements, the maximum frequency tolerance of ± 50 ppm is required.

4.1.3 Jitter Tolerance

The following figures are the VSC8211 jitter 1000 Mb/s-mode tolerance data vs. frequency for a 25 MHz reference clock for Copper and Fiber media types, respectively. The plots show the maximum peak-to-peak sinusoidal jitter that can be allowed in the PHY reference clock to still meet the IEEE requirements (measurements were made at nominal voltage supply values).

Although reference clock jitter above the plotted values violates the IEEE specified limit, the link partner can generally tolerate levels of jitter somewhat above this strict limit (that is, the link will still function normally), however, meeting this limit allows for a more robust design under real life operating conditions.

Figure 3 • Maximum peak-to-peak sinusoidal jitter to meet IEEE requirements for 1000Base-T (25MHz reference clock)

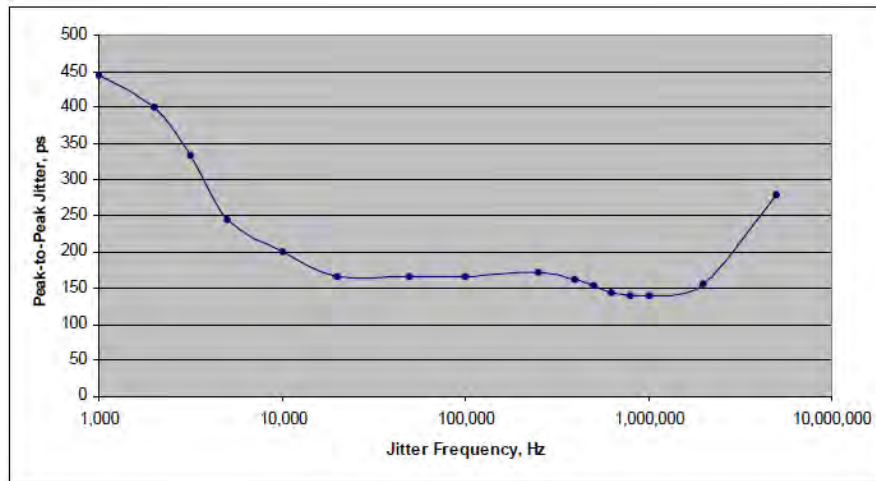
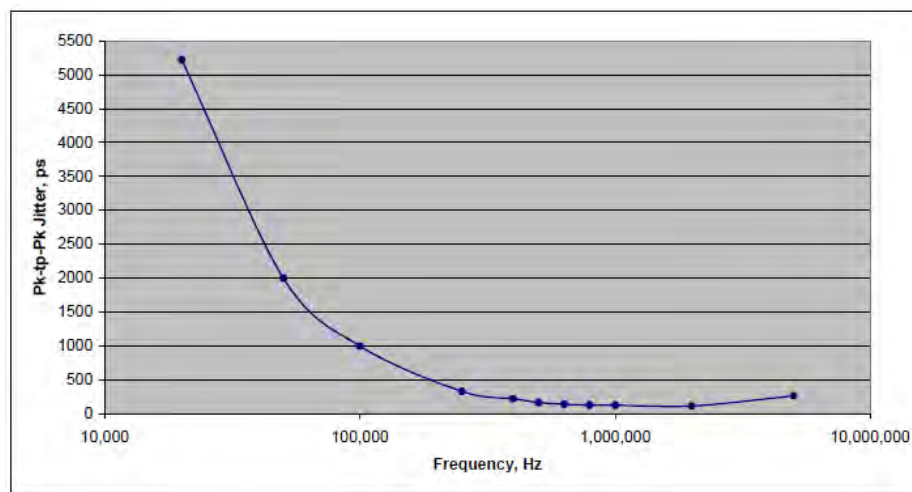


Figure 4 • Maximum peak-to-peak sinusoidal jitter to meet IEEE requirements for 1000Base-X (25MHz reference clock)



4.2 Recovered Clock Characteristics

4.2.1 RX_CLK as Recovered Clock

The parallel MAC interface' RX_CLK output pin delivers a clock synchronized to the active media link's clock and is useful for Synchronous Ethernet applications in the 100Base-T (100 Mb/s Copper variant), 100Base-FX (100 Mb/s Fiber variant), and 1000Base-T (1000 Mb/s Copper variant) operating modes. This pin is disabled when a Serial MAC interface is used.

4.2.2 Recovered Clock Origin - Copper Media

1. In the 10Base-T mode, as mentioned previously, a receiver does not produce a reliable continuous clock source due to indeterminate pauses between frame transfers.

2. In the 100Base-T mode, as long as the media link is up, the RX_CLK output signal is synchronized to its clock. When the link is down, it is synchronized to the PHY reference clock (REFCLK) input signal and is no longer useful for Synchronous Ethernet; therefore, the PLL-based Clock Synthesizer should switch to the hold-off mode, based on the Fast Link Failure indication (see 3.3).
3. In the 1000Base-T mode, the PHY must be configured (using its Register 9) to auto-negotiate to "Slave Timing"; then the RX_CLK output signal is synchronized to the active media link's clock. When a "Master" or no media link, the PHY is synchronized to the reference clock (REFCLK) input signal (which is local), and RX_CLK is no longer useful for Synchronous Ethernet; therefore, the PLL-based Clock Synthesizer should switch to the hold-off mode, based on the Fast Link Failure indication (see 3.3).

4.2.3 Recovered Clock Origin - Fiber Media

- The 100Base-FX case is similar to the 100Base-T one.
- In the 1000Base-X mode, the signal's origin depends on the Fiber link status:
 - If up, RX_CLK is recovered from the data stream coming from the link partner (Clock Master),
 - If down, the internal VSC8211's PLL is generally locked on the free-running local clock source (REFCLK) but periodically watches the input Fiber signal to lock on, and this algorithm makes the delivered RX_CLK signal's jitter too high for clock recovery, and the PLL-based Clock Synthesizer should switch to the hold-off mode, based on the Fast Link Failure indication (See Sec 3.3, below).

4.2.4 Recovered Clock Frequency

In accord with the IEEE-802.3 standard, the RX_CLK frequency value must be either 25MHz or 125MHz for the 100Mb/s and 1000Mb/s operating modes, respectively.

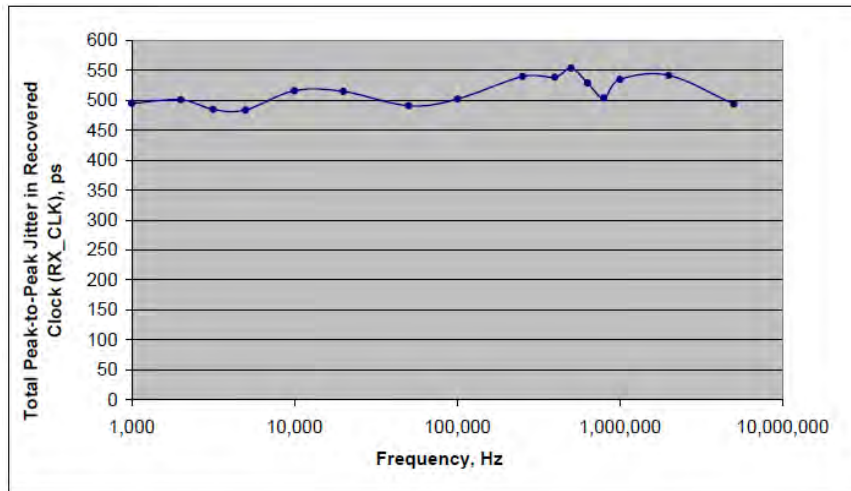
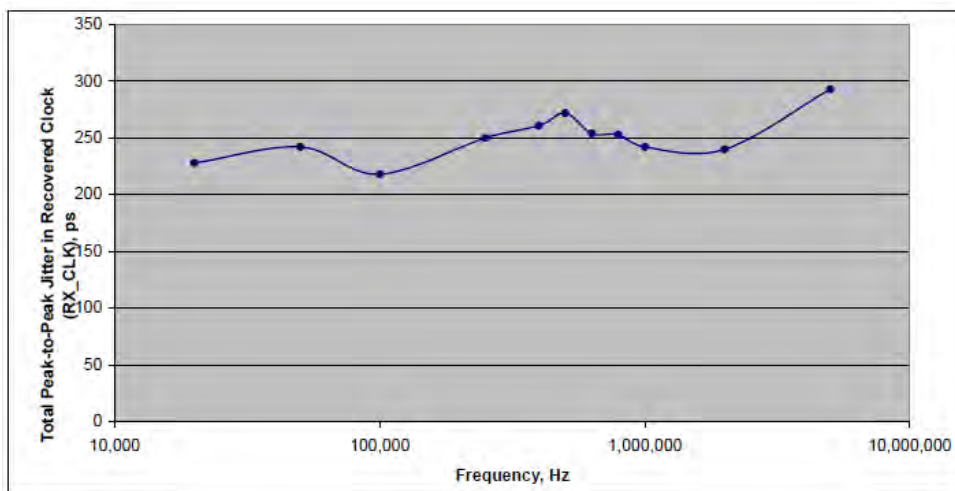
4.2.5 Recovered Clock Jitter

The amount of jitter present in the received media signal influences the jitter figures of the RX_CLK signal recovered from it. Presented below, in Figures 5, 6, are the jitter transfer characteristics of the VSC8211 incurred when providing the recovered clock signals obtained from the various Ethernet media types. (Note, this data was obtained at the nominal VSC8211 voltage supply settings.)

The jitter transfer data makes it possible to evaluate the amount of jitter contained in the recovered clock signal for a given media input, and is therefore useful in selecting an appropriate PLL-based Clock Synthesizer type, that is able to tolerate these jitter levels at the frequencies covered.

In contrast to the VSC8664, the VSC8211 produces a higher level of jitter (especially in the Copper case) and little frequency dependency. This results from the fact that in the VSC8211, the RX_CLK is not a dedicated recovered clock signal, as is the case for the VSC8664, but a part of the parallel MAC block, which is digital and quite noisy by its nature.

The higher jitter levels exhibited for operation with Copper media is a result of the more powerful line drivers used for the Copper section of the PHY, which when active, interfere (through the shared power rails on the silicon die) with the other PHY modules, thus deteriorating their performance. So the media type used in the given application is an important factor in selecting the appropriate Clock Synthesizer.

Figure 5 • 1000Base-T Jitter Transfer**Figure 6 • 1000Base-X jitter transfer**

4.3 Fast Link Failure Indication

When a given port is being used as a synchronization-timing link for the system and its link goes down (fails), the system host must be immediately notified that the Clock Synthesizer input is being switched to either the secondary recovered clock or, in the case of both clock links failing, to a free-running clock. Such rapid notification is critical for metro Ethernet traffic and overall system synchronization.

4.3.1 Copper Media Implementation

A Clock Slave PHY operating in the 1000Base-T mode must auto-negotiate to "Slave Timing". The amount of time required by the PHY to ascertain link status is from 340 to 360 ms, as defined in the IEEE 802.3 standard (Sec 40.4.5.2, Timers). Neither the "Link Status" (as indicated in VSC8211 Register 1, bit 2) nor the appropriate LED state will indicate the status change until the specified amount of time has elapsed. A technique making use of the PMA descrambler "lock-state", however, can provide a faster alternative for indicating a link failure in 100Base-TX and 1000Base-T modes.

The PMA block in the VSC8211 PHY uses data scrambling to randomize the sequence of transmitted symbols to prevent the presence of spectral lines. Since any two connected PHYs should always have their scrambler and descrambler synchronized prior to PCS operation, the descrambler's "lock-loss" event indicator can be used to indicate a link failure. (This is true because a synchronization loss of always precedes a "link-down" indication in the PCS block.) Although PHYs are not required to display this information to a user, Vitesse Ethernet PHYs make this event visible using register bits (Bit 7 of Registers 25 and 26, expressed as 25.7, 26.7) accessible by the host.

Implementation of a fast "link-fail" indicator depends on whether the PHY's interrupt pin is enabled or disabled by the 25.7 register bit value. When the interrupt is enabled and the descrambler lock-loss event occurs, the interrupt pin is triggered within units of milliseconds. The interrupt service routine must then check the 26.7 register bit value. If the bit is set, this means that a descrambler lock-loss has occurred and the link is about to fail. An example of the host code when the interrupt pin is enabled is as follows:

Example 1, Procedure when interrupt pin is enabled

```
/* Enable PHY interrupt pin and enable descrambler lock-loss interrupt mask; this
should be done only once during PHY initialization. */
PhyWrite (reg_num(dec), 16_bit_unsigned_data(hex))
PhyRead (reg_num(dec))
PhyWrite 25 0x8080;
/* Check the interrupt status register and send "Link-Fail" message to the host if
the "Lock-Loss" bit is asserted. */ If ((PhyRead 26)&0x0080 == 1) Action(Link_Fail);
Else if((PhyRead 1)&0x0004 == 0) Action(link_Fail);
Else return;
```

When the PHY's interrupt pin is disabled, the 26.7 register bit value should be continuously polled. Presented below is a configuration example for the case in which the VSC8211 interrupt pin is disabled:

Example 2, Procedure when interrupt pin is disabled

```
/* Enable descrambler lock-loss interrupt mask. This should be done only once during
PHY initialization. */
PhyWrite (reg_num(dec), 16_bit_unsigned_data(hex))
PhyRead (reg_num(dec))
PhyWrite 25 0x0080;
/* Continually check the linked up port. Assertion of the 26.7 register bit indicates
that descrambler lock-loss occurred for 100Base-TX or 1000Base-T, which implies that
link failure is about to take place. */
If ((PhyRead 26)&0x0080 == 1)
Action(Link_Fail);
Else if((PhyRead 1)&0x0004 == 0)
Action(link_Fail);
Else return;
```

Lab tests were conducted for a 1000Base-T media connection using the above-described technique, and the Link Failure indication time was found to be in the neighborhood of 165ms.

4.3.2 Fiber Media implementation

In the case of fiber based media the fast Link Failure indicator can be accomplished by simply monitoring the status of the "LOS" pin of the fiber module indicating the status of the 1000Base-X link. In the 100Base-FX case, the same approach can be applied as for the Copper media described in 3.3.1.

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