VSC8502
User Guide
VSC8502 Evaluation Board

January 2019

Microsemi
a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Revision 1.1 of this datasheet was published in January 2019. The new Microchip template was added to the document.

1.2 Revision 1.0

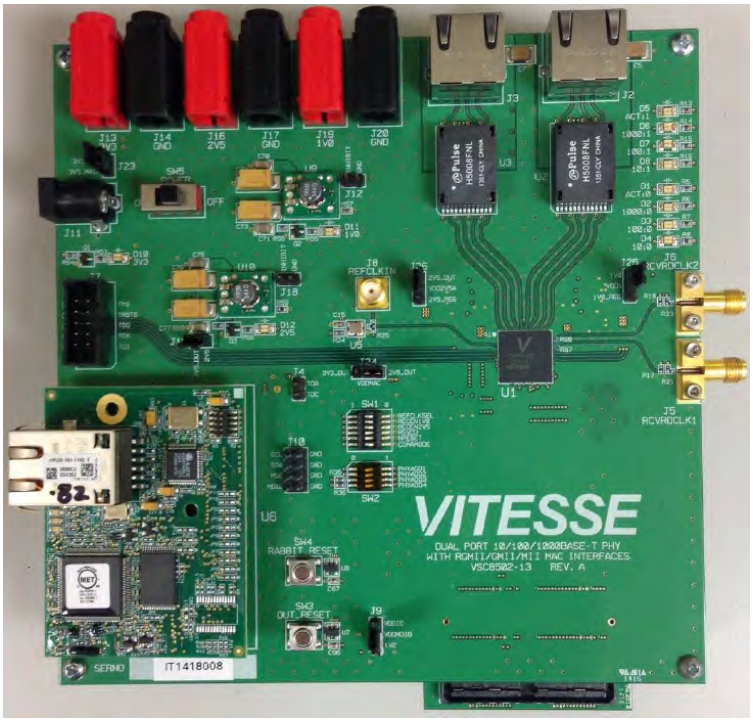
Revision 1.0 of this datasheet was published in May 2014. This was the first publication of the document.

2 Introduction

The VSC8502 device is a low-power, cost-optimized, dual-port gigabit Ethernet PHY. It features integrated, line-side termination to conserve board space, lower EMI, and improved system performance. To further reduce system complexity, component count, and system cost, the VSC8502 device can operate from a single 3.3 V supply using integrated voltage regulators. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines. The device also optimizes power consumption in all link operating speeds and features Wake-on-LAN (WOL) power management using magic packets.

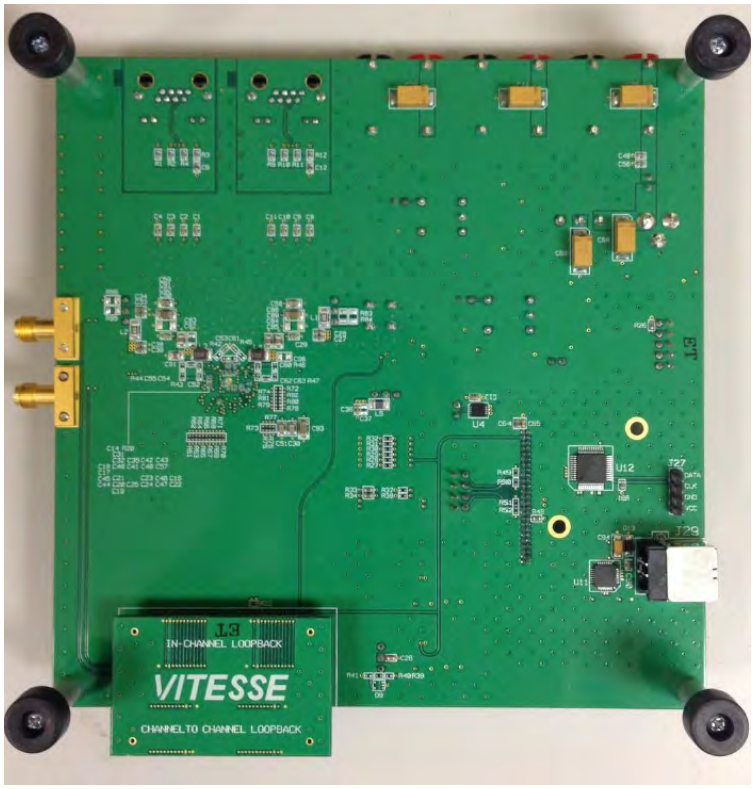
This document describes the architecture and usage of the VSC8502 Evaluation Board (VSC8502EV). The Quick Start section describes how to install and run the graphical user interface (GUI) to fully control the evaluation board.

Figure 1 • VSC8514 Evaluation Board (Top View)



The following illustration shows the bottom view of the VSC8502 evaluation board.

Figure 2 • VSC8514 Evaluation Board (Bottom View)



Additional VSC8502 collateral for both the VSC8502 device and VSC8502EV, including schematics, layout, GUI, and application notes can be found on the VSC8502 product web page at: https://www.vitesse.com/products/product.php?number=VSC8502.

3 General Description

The evaluation board, shown in Figure 1, provides the user a way to evaluate the VSC8502 device in multiple configurations. Two RJ-45 connectors are provided for copper media interfaces. The MAC interface is exposed via SAMTEC connector (J1) that allows for the complete eval board to be mated with a motherboard having the necessary signals for operating the device.

For standalone access to all of the features of the device, an external microcontroller is used to configure the VSC8502 via the MDIO bus. The GUI enables the user to read and write device registers.

3.1 Key Features

This section shows the key features for VSC8502.

3.1.1 Copper Port RJ45 Connections

PHY ports 0 and 1 use generic RJ45 connectors with discrete pulse H5008NL magnetics.

GMII MAC Connector

The parallel MAC interface is available through a Samtec connector J1. As described in section 2.1.7, it can be configured with the companion daughtercard installed at J1 as
either single-port loopback or port-port traffic passing modes.

Switch Block Control

See Figure 3 for definition of SW1 controls.

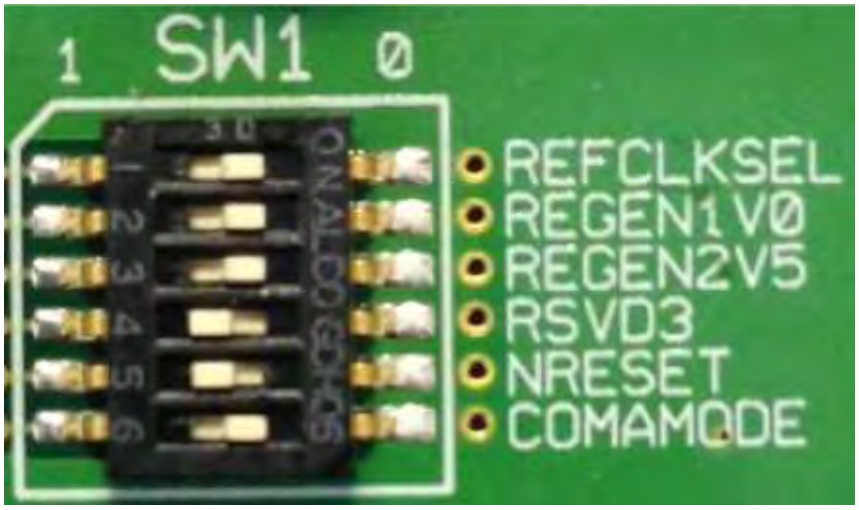
See Figure 4 for the default settings.

Table 1 • DIP Switch 1 Options

DUT Control Signal	DIP SW1	pos '1' = pull up to VDDMAC; pos '0' = pull down to GND
REFCLK_SEL	SW1.1	0=125 MHz (default); 1 =25 MHz
REGEN_10	SW1.2	0=OFF (default); 1= ON
REGEN_25	SW1.3	0=OFF (default); 1= ON
RESERVED3/CLK_SQUELCH_IN	SW1.4	1=enabled(default); 0 = disabled
NRESET	SW1.5	1=operational (default); 0=held in reset
COMA_MODE	SW1.6	0=disabled (default); 1=enabled

The following image shows the SW1 switch control for the VSC8502EV.

Figure 3 • SW1 Switch Control



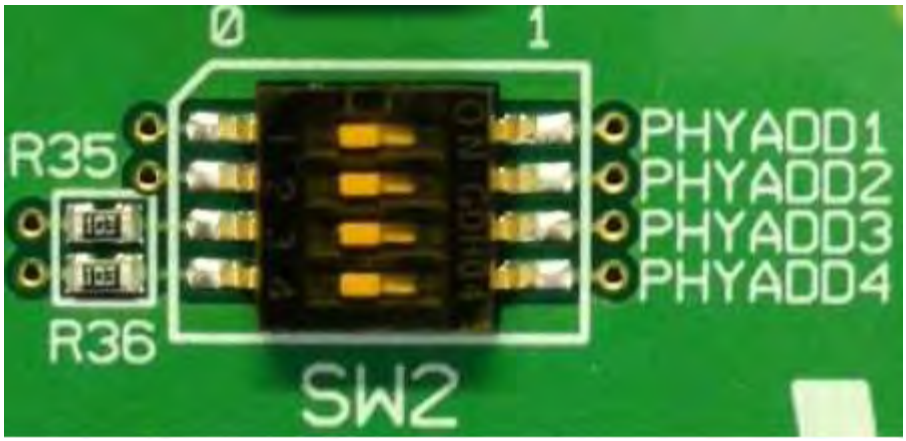
The following table shows the DIP switch options for the VSC8502 evaluation board.

Table 2 • DIP Switch 2 Options

DUT Control Signal	DIP SW1	pos '1' = pull up to VDDMAC; pos '0' = pull down to GND
RCVRDCLK1/PHYADD1	SW1.1	0=default
RCVRDCLK2/PHYADD2	SW1.2	0=default
PHYADD3	SW1.3	0=default
PHYADD4	SW1.4	0=default

Note: R17 and R18 0 ohm options must be installed for PHYADD1 and PHYADD2 to be affected by SW2, otherwise they are internally pulled to GND. Also, PHYADD3-4 pins
are internal PD on the VSC8502 IC, and are weakly pulled to GND when their corresponding SW2 pins are kept in '0' position.

Figure 4 • SW2 Switch Control



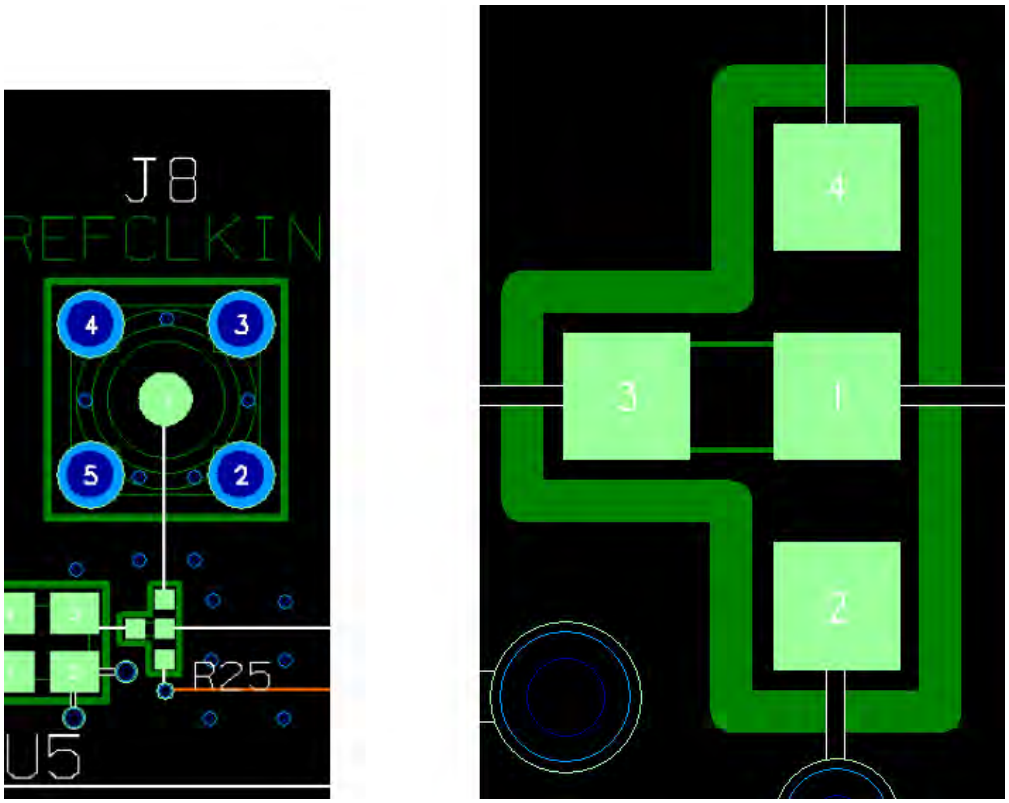
3.1.2 External RefClk Option

The user may choose to provide an external PHY REFCLK via SMA connection to J8 (as shown in Figure 1). To route the SMA signal to the device the user must reorient the zero ohm resistor R25, as shown from the PCB layout view in Figure 7.

Note: external PHY REFCLK must be connected via SMA to J8 if 3.3 V VDDIO/VDDMAC is used, since the on-board crystal oscillator (U5) is a 2.5 V CMOS driver.

R25 can also be connected across pins 1 and 2 if a user wants to provide DUT REFCLK input from the Samtec connector J1.

Figure 5 • REFCLK Input Options - R25 3-Way Orientation



3.1.3 Recovered Clocks

There are two recovered clocks available from the VSC8502, through SMA connections J5 (RCVRDCLK1) and J6 (RCVRDCLK2). In the default configuration, CLK_SQUELCH_IN is pulled down, which disables the clock squelching and RCVRDCLK1/RCVRDCLK2 are connected to the Samtech header J1. To route RCVRDCLK1 and RCVRDCLK2 to SMAs J5 and J6, reorient zero ohm resistors R21 and R23, respectively.

Software Interface Microcontroller Card
A Silabs F340 microcontroller is included to facilitate a software interface to the registers on the VSC8502 through a USB port.

Note: Alternatively, a Rabbit card is available for an IP-based manager of the PHY register space, installed in the keep-out area (U6) of the board's top-side. Or, MDC and MDIO can be accessed on stake header J10 if desired for another microcontroller to host the PHY register space.

3.1.4 GMII loopback card

The VSC8502EV ships with a daughter card that mounts to J1 to loop-back the GMII/RGMII interface.

As shown in Figure 8 and Figure 9 below, one orientation of the loopback card will loop each port back to itself (IN-CHANNEL LOOPBACK in Figure 8). The other orientation
forwards bidirectional traffic from one port to the other (CHANNEL TO CHANNEL LOOPBACK).

Figure 6 • Loopback Card (Side A)

Figure 7 • Loopback Card (Side B)

Note: this daughter card loopback only supports 1000 BASE-T in GMII mode and 10/100/1000 in RGMII mode. It will not support 10/100 in MII mode.
However, there are other internal loopback modes that will support BER testing of MII mode such as far-end loopback (MII Register 23.3).

3.2 Key Features

This section shows the power supply options for VSC8502.

3.2.1 Single 3.3 V Input for Both DUT and Other Components

This option allows for one external 3.3 V supply connected to J11 to power everything on the board. Use the following steps:

- SW1 REGEN1V0 = REGEN2V5 = 0: disable on-chip regulators
- Insert a 3.3 V DC supply (rated for 1 Amp) into J11
- Unplug banana connectors J16(+): J17(GND)
- Unplug banana connectors J19(+): J20(GND)
- Populate J23: 3V3_DUT = 3V3_MAIN
- Populate J15: 2V5_DUT = 2V5
- Populate J26: VDD25A = 2V5_DUT
- Remove J18: on-board 3.3 V to 2.5 V regulator enabled
- Populate J25: VDD1 = 1V0
- Remove J12: on-board 3.3 V to 1.0 V regulator enabled
- Populate J24: VDDMAC = 3V3_DUT or 2V5_DUT (VDDMAC is tied to VDDIO. The DUT's VDDIO can operate at either 2.5 V or 3.3 V)
- Populate J9: VDDMDIO = VDDIO (1.2 V option is not available at this time, due to inability to drive 1.2 V from on-board microcontroller options)

DUT Power Rails Isolated from non-DUT Power
This option allows for the DUT power supplies to be isolated from the rest of the board power. Use the following steps:

- SW1 REGEN1V0 = REGEN2V5 = 0: disable on-chip regulators
- Insert a 3.3 V DC supply (rated for 1 Amp) into J11
- Populate banana jacks J13(+): J14(GND) with 3.3 V supply
- Populate banana jacks J16(+): J17(GND) with 2.5 V supply
- Populate banana jacks J19(+): J20(GND) with 1.0 V supply
- Remove J23: 3V3_DUT = J13 (3.3 V)
- Remove J15: 2V5_DUT = J16 (2.5 V)
- Populate J26: VDD25A = 2V5_DUT
- Remove J18: on-board 3.3 V to 2.5 V regulator enabled
- Populate J25: VDD1 = 1V0 (note: 1V0 = J19)
- Populate J12: on-board 3.3 V to 1.0 V regulator disabled
- Populate J24: VDDMAC = 3V3_DUT or 2V5_DUT (VDDMAC is tied to VDDIO. The DUT's VDDIO can operate at either 2.5 V or 3.3 V)
- Populate J9: VDDMDIO = VDDIO (1.2 V option is not available at this time, due to inability to drive 1.2 V from on-board microcontroller options)

3.2.2 DUT On-chip Regulator Power

The on-chip regulator option for this board is for engineering purposes only. There are performance issues associated with using the on-chip regulator on this board, so it is
an unsupported board feature.

4 Quick Start

This section shows the quick start for VSC8502.

4.1 Connecting the Power Supply

The evaluation board offers choices of how to power the 3.3 V, 2.5 V, and 1.0 V rails which drive the devices as well as modules; please see section 2.2 for reference. The simplest power option for the evaluation board is to use the power pack for 3.3 VDC. Simply plug the AC adaptor into a wall socket and the barrel end into J11 (see the upper left corner of Figure 1). Immediately the user should see several LEDs turn on.

Note: for proper power-on sequencing on this board, please toggle NRESET input to the DUT using either SW3 (push-button) or SW1 (DIP) after board power is applied but prior to launching the GUI.

4.2 PC Software Installation

1. Download the ZIP file from Vitesse's website onto a PC that has a USB port
2. Install the GUI by launching the setup.exe file
3. USB communication is assisted by the Silabs USBXpress® drive. If not present on the PC, the user will need to download the
   USBXpress development kit from the Silicon Labs website (URL: http://www.silabs.com/products/mcu/Pages/USBXpress.aspx)
4. Double click the desktop icon to launch the GUI

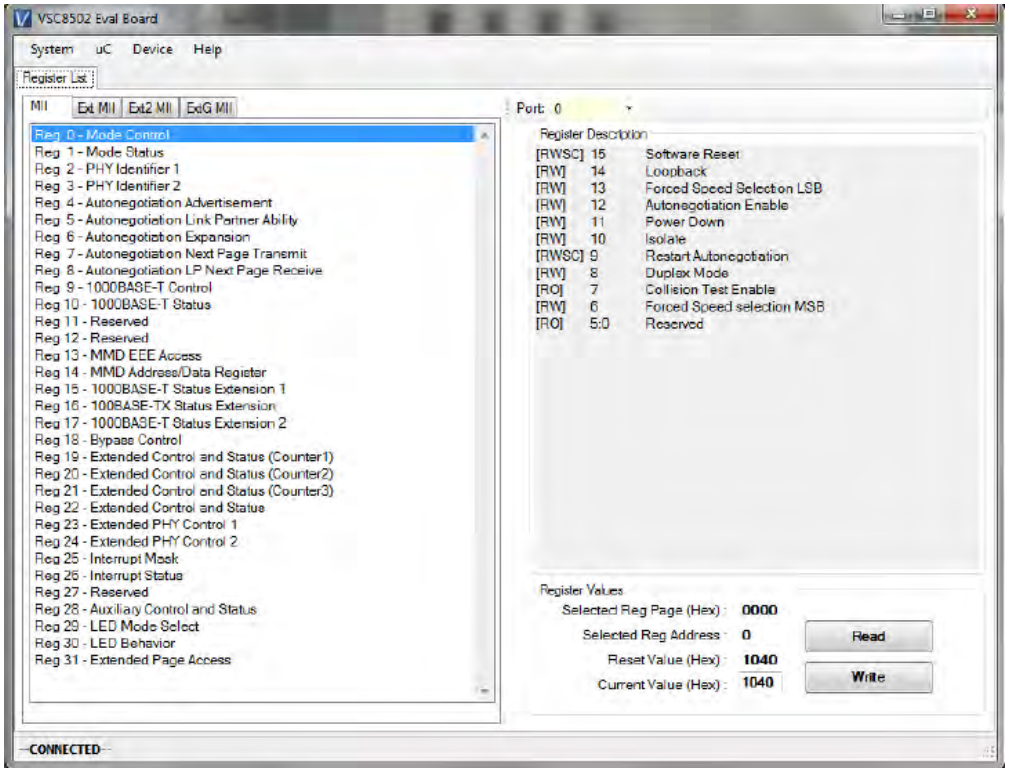
4.3 Connecting to the Board to the PC

Launch the GUI either by clicking on the desktop shortcut or clicking on the "Star t> Programs > Vitesse Semiconductor Corp > VSC8502_GUI" icon. The initial window will detect the attached USB devices automatically. Figure 10 shows a typical EVB Connection window.

Figure 8 • GUI Connection Window

The EVB serial number should appear. If not, click on "Scan For USB Devices." Select that EVB serial number then click "Launch GUI". The Register List window will appear as shown in Figure 11.

Figure 9 • MII Registers GUI Window



Be sure the device is up and running by reading MII Register 0. It should read back 0 × 1040. Reading back all 0's or all 1's indicates a problem. For a multi-port device, the corresponding PHY port number is accessed via the "Port:" pick list shown above the Register Description in Figure 11.

As Figure 11 indicates, the extended MII register pages can be accessed to read or write by clicking on one of the ExtMII/Ext2MII/ExtGMII tabs.

4.3.1 Board Initialization

Note: if J1 is used for an evaluation session, the SAMTEC connector J1 should be populated prior to power-on of the board (for example, with the companion GMII loopback card show in section 2.1.7 for a desired external loopback mode). Once the evaluation board connectivity has been established and confirmed, the PHY should be initialized. Initialization can be accomplished by running an init-script sequence, such as performed by the pre- and post-reset functions of the PHY API standalone app.

While the init-script sequence may not be required for specific operational modes, an init-script sequence is highly recommended to ensure correct performance over the greatest set of user scenarios for the PHY. After initialization is performed, refer to the PHY Datasheet section on configuring the PHY and PHY Interfaces for the desired application.

4.3.2 Copper Media Operation (Auto-negotiation Enabled)

The easiest configuration for passing traffic is with Autoneg enabled (MII 0 bit 12 = 1). Use MII Register 0, 4 and 9 to change speed and restart autoneg (MII 0 bit 9) to advertise new settings. As per the datasheet descriptions, the commonly-used speed advertisement definitions are as follows:

Table 3 • Auto-Negotiation Advertisements

	MII reg 4 bits 8:7	MII reg 4 bits 6:5	MII reg 9 bits 12:11	MII reg 9 bits 9:8
1000BT Master mode	N/A	N/A	11	11
1000BT Slave mode	N/A	N/A	10	11
100 BASE-TX Full Duplex	11	N/A	N/A	00
10 BASE-T Full Duplex	00	11	N/A	00

The following steps are used to configure a link:

1. Set up the Copper traffic source (i.e., IXIA or Smartbits)
2. Connect Ethernet cable(s) to a single or multiple RJ-45 ports
3. Configure auto-negotiation as per above and re-start ANEG (MII bit 0.12)
4. The linkup bit is in MII Reg 1, bit 2 (MII 1.2), read it twice to update

Traffic should now be flowing.

4.3.3 Driving Recovered Clock Output

To output the a recovered clock from the PHY on this evaluation board, ensure zeroohm resistors R21 and R23 are oriented as per section 2.1.5 and perform the following register writes to enable RCVRDCLK1 with PHY0 as the clock source:

- Write 0×8101 to register 23 of the “General Purpose Registers” when PHY0’s link is up in a non-EEE mode and not 1000BT master or 10BT
- Set MII Register bit 9.12 to enable manual slave configuration then issue an auto negotiation restart through register bit 0.9

To select a different port as the clock source or enable a recovered clock for EEE mode, refer to register 23 G/24 G in the datasheet for the programming detail.

Note: The recovered clock output is intended to drive a CMOS load, not a DCcoupled low impedance such as a scope 50-Ohm termination. The recommended measurement equipment is an active (high-impedance) differential probe. Refer to the device datasheet for additional loading and performance specifications.

4.4 Useful Test Features

4.4.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. The EPG sends traffic in multiple of 10,000 frames regardless of when you stop transmit activity. Refer to the datasheet for configuration options.

A good CRC packet counter is in ExtMII 18.13:0. The good CRC packet counter is a modulo 10,000 counter so values will always be between 0-9,999. A read of the register reads back the good CRC packets and then clears the register so the subsequent reads will be 0 if no traffic has been received. If traffic has been received since the last read, bit 15 will be set.

4.4.2 Copper PHY Error Counters

Idle errors = MII 10.7:0
RX errors = MII 19.7:0
False carrier = MII 20.7:0
Disconnects = MII 21.7:0
CRC errors = ExtMII 23.7:0

4.4.3 Near-End Loopback

When the near-end loopback test feature is enabled, the transmitted data is looped back in the PCS block on the receive data signals. To enable the loopback, set register bit 0.14 to 1. Near-end loopback mode involves traffic flow over the GMII/RGMII interface, so a breakout of the MAC interface on SAMTEC connector J1 must be connected to another system for this mode to pass traffic.

4.4.4 Far-End Loopback

When the far-end loopback test feature is enabled, incoming data from a link partner on the Copper interface to be transmitted back to the link partner on the Copper interface. To enable the loopback, set register bit 23.3 to 1.

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

© Microsemi. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www microsemi.com.

VPPD-03741