KSZ879x/KSZ877x/KSZ876x Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the Microchip KSZ879x/KSZ877x/KSZ876x Ethernet switches, which include the following devices:

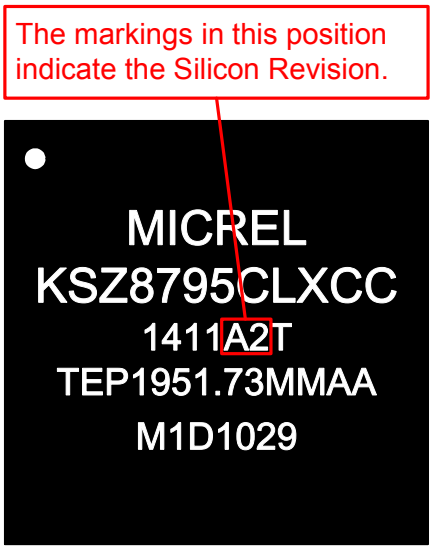
- KSZ8795CLXCC / KSZ8795CLXIC
- KSZ8794CNXCC / KSZ8794CNXIC
- KSZ8775CLXCC / KSZ8775CLXIC
- KSZ8765CLXCC / KSZ8765CLXIC

The silicon errata discussed in this document are for silicon revisions as listed in Table 1. The silicon revision can be determined by the device's top marking as indicated in Figure 1. A summary of KSZ879x/KSZ877x/KSZ876x silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
KSZ8795CLXCC, KSZ8795CLXIC, KSZ8794CNXCC, KSZ8794CNXIC, KSZ8775CLXCC, KSZ8775CLXIC, KSZ8765CLXCC, KSZ8765CLXIC	A2 and older

FIGURE 1: TOP MARKING DATE CODE INDICATION



Note: The purpose of Figure 1 is to detail the top markings of an example part and highlight the location of the date code. Other top marking values may differ (lot codes, location of manufacture, etc.).

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TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary
1.	Transmission errors in 100BASE-TX Mode when Auto-Negotiation is disabled
2.	Link drops with some EEE link partners
3.	Establishing a link through low loss connections
4.	Idle transmitter common mode voltage drift at cold temperature
5.	Transmission halt with late collisions

Silicon Errata Issues

Module 1: Transmission errors in 100BASE-TX Mode when Auto-Negotiation is disabled

DESCRIPTION

When a PHY port is configured to disable Auto-Negotiation (AN) and forced to 100BASE-TX full/half-duplex mode, transmission errors may be output from the egress port.

END USER IMPLICATIONS

When this issue occurs, transmitted errors output from egress port may result in an unstable link with the partner.

Only PHY ports (Ports 1 to 4 for the KSZ8765/KSZ8775/KSZ8795, ports 1 to 3 for the KSZ8794) are affected by this issue. The Gigabit MAC processor port is unaffected. Additionally, PHY ports will not exhibit this issue if configured to Auto-Negotiation mode or forced to 10BASE-T mode.

Work Around

This issue can be prevented by using the appropriate script below when setting the port to force 100BASE-TX link (full-duplex) mode:

- Auto-MDI/MDIX Mode:

```
w nd 40 //Disable TX by writing 40h register NDh
w n9 00 //Set to Auto-MDI/MDIX by writing 00h to register N9h
w nc ff //Force 100 FD mode (disable AN)by writing FFh to register NCh
w nd 00 //Enable TX by writing 00h to register NDh
```

- Force-MDI Mode:

```
w nd 44 //Disable TX and Force to MDI by writing 44h to register NCh
w nc ff //Force 100 FD mode (disable AN) by writing FFh to register NCh
w nd 04 //Enable TX by writing 04h to regsiter NDh
```

- Force-MDIX Mode:

```
w nd 46 //Disable TX and Force to MDIX by writing 46h to register NDh
w nc ff //Force 100 FD mode (disable AN) by writing FFh to register NCh
w nd 06 //Enable TX by writing 06h to register NDh
```

In the scripts above, "*n*" is the Port value 1,2,3 or 4. For example, to disable TX on Port 3: w 3d 40.

If the force 100BASE-TX half-duplex mode is required, then write 'df' instead of 'ff' to register nc. For example, on port 3: w 3c df.

PLAN

This errata will not be corrected in a future revision.

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Module 2: Link drops with some EEE link partners

DESCRIPTION

An issue with the EEE next page exchange between the KSZ879x/KSZ877x/KSZ876x and some EEE link partners may result in the link dropping.

END USER IMPLICATIONS

With certain EEE link partners, the KSZ879x/KSZ877x/KSZ876x may inadvertently drop the link between devices.

Work Around

Disable the EEE next page exchange in EEE Global Register 2 (0x35) by setting bits [3:0] to 0x0 (bits [3:0] default to 0xF).

PLAN

This errata will not be corrected in a future revision.

Module 3: Establishing a link through low loss connections

DESCRIPTION

The receiver of the embedded PHYs is tuned by default to support long cable length applications. This was developed using low quality, high loss cables. Because of this, the equalizer in the PHY may amplify high amplitude receiver signals to the point that the signal is distorted internally, preventing a link from being established.

END USER IMPLICATIONS

When connecting the PHY ports to link partners through low loss connections, the port may take a long time to establish a link, or may not link at all. This includes standard unshielded twisted pair cables less than 5m, capacitive coupled connections between two chips on the same PCB, or custom cables with low impedance loading.

Work Around 1

A more balanced receiver setting has been found that still functions at the long cable lengths and also supports low loss applications. To change this setting, write to the following registers:

```
w 6e a0 //Write A0h to register 6Eh to set up an indirect register write
w 6f 3c //Write 3Ch to register 6Fh to set the indirect register address to 3Ch
w a0 15 //Write 15h to the PHY equalizer register
```

Note: All PHYs are impacted by this new setting, the change is not PHY specific.

Work Around 2

If work around 1 does not solve the short cable issue in a CAT-5E or CAT-6 application, change the work around 1 register (0x3C) to its default value (0x0A), and use the following settings:

```
w 6e a0 //Write A0h to register 6Eh to set up an indirect register write
w 6f 4c //Write 4Ch to register 6Fh to set the indirect register address to 4Ch
w a0 40 //Write 40h to the indirect register 4Ch, the default value is 00h
```

PLAN

This errata will not be corrected in a future revision.

Module 4: Idle transmitter common mode voltage drift at cold temperature

DESCRIPTION

Below 0°C, the voltage controlled output of the transmitter, when inactive, can become unstable and affect the receiver of the link partner. This voltage instability is only observed when the transmitter is in a low activity state, such as auto-negotiation and 10Base-T idle conditions.

END USER IMPLICATIONS

This errata can manifest in long delays for the port to establish a link at cold temperatures, as well as errors when connected with a 10Base-T connection.

Work Around

If the transmitter is always actively driving the voltage levels, the cold temperature instability does not occur. The transmitters can be permanently enabled by executing the following commands:

```
w 6e a0 //Write A0h to register 6Eh to set up an indirect register write
w 6f 4e //Write 4Eh to register 6Fh to set the indirect register address to 4Eh
w a0 40 //Write 40h to enable the transmitter to actively transmit at all times
```

This workaround will increase the VDDAT current in auto-negotiation mode and 10Base-T Idle mode by ~60mA, but it will not increase the maximum current draw of the device at full traffic.

Note:	All PHYs are impacted by this new setting, the change is not PHY specific.

PLAN

This errata will not be corrected in a future revision.

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Module 5: Transmission halt with late collisions

DESCRIPTION

Section 4 of the IEEE 802.3 Specification details Carrier Sense Multiple Access / Collision Detection (CSMA/CD) parameters when operating in half-duplex mode. The first 512 bit times are designated as the slotTime, which is the maximum amount of time allowed for a collision to occur. If a link partner is configured incorrectly, where the PHY is linking in half-duplex mode but the MAC is configured in full-duplex mode, there is a chance that the link partner will generate a collision after the first 512 bit times, violating the IEEE 802.3 specification. These late collisions, combined with other factors, can cause the switch port transmitter to lock up and stop sending packets. The receiver will still function.

END USER IMPLICATIONS

If this erratum occurs, the switch will stop transmitting data to the half-duplex port, making it seem the half-duplex link partner has stopped communicating to the network. The more traffic there is, the greater the risk of the violating link partner generating a late collision that will affect the port.

Work Around

Ideally, the link partner that is violating the specification would need to be updated so the MAC and PHY are correctly configured to the same duplex setting. If the link partner cannot be modified to conform to the IEEE 802.3 specification, the switch can be re-configured to full-duplex when late collisions are detected to avoid a lock up condition. Of note, each switch port functions independently. Therefore, any work around must be implemented separately for each port.

Method 1:

To avoid transmitter lock up, when a port is linked in half-duplex mode, the software should monitor the TxLateCollision MIB counter (MIB Offset 0x16). If the number is ever non-zero, the software should force the link to function in full-duplex mode by disabling auto-negotiation and setting full-duplex and the appropriate speed in the Port Control 9 Registers (addresses 0x1C, 0x2C, etc.)

Method 2:

To detect transmitter lock up, the software should monitor the Port x Tx Total Bytes and the Port x Rx Total Bytes. If the Port x Rx Total Bytes is incrementing but the Port x Tx Total Bytes remains the same, the software should perform a hard reset of the switch.

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000687C (08-03-18)	Module 5.	Added new erratum for Transmission halt with late collisions
	Module 3.	Updated to add additional second work around method. Changed length of cable in end user implications to 5m.
DS80000687B (11-21-17)	Modules 3. and 4.	Added modules 3 and 4
DS80000687A (01-06-16)	All	Initial release

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