TB3260

How to Create Non-Cacheable Memory Region on Cortex-M7 (SAM S70/ E70/ V70/ V71) MCUs Using MPLAB Harmony v3

Introduction

The cache coherency issue is inevitable on applications running on microcontrollers (MCUs) that have cacheable memory regions, which utilize Direct Memory Access (DMA) for data transfer operations. This is due to the CPU performing a read/write from the cache while the DMA transfers data between the peripheral and physical memory.

One of the methods to address cache coherency is to create a coherent or non-cacheable memory region and place data variables in contention within it. When the data is made coherent, the CPU always accesses the data from the main memory (SRAM).

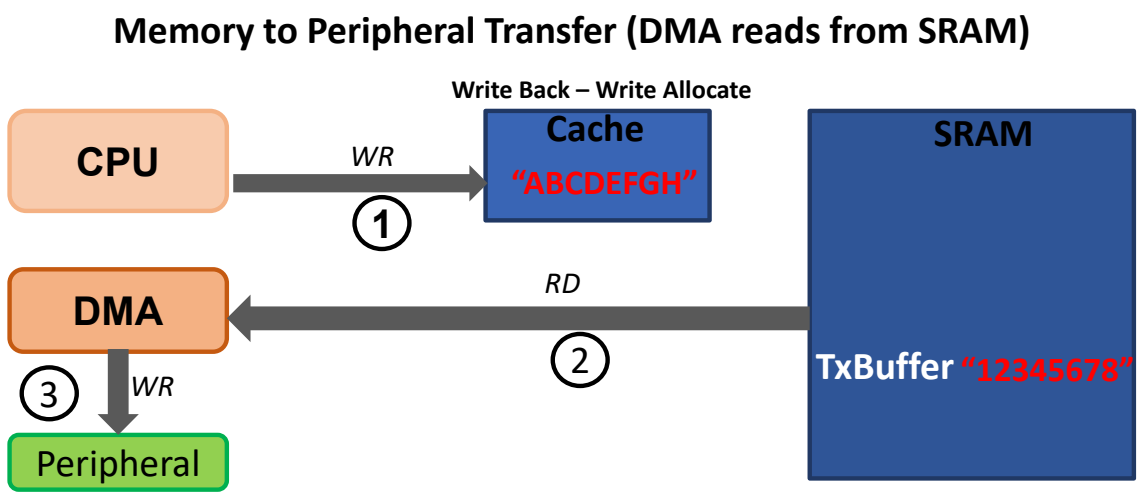
This document explains how to create a non-cacheable memory region and allocate data variables under contention in the non-cacheable region using MPLAB® Harmony v3.

Note: The concepts discussed in this document are common for all Arm®Cortex®-M7 MCUs, and the SAM E70 MCU is used as an example to discuss the concepts.

1. Description

The following figure illustrates one form of cache coherency issue observed on the SAME70 MCU.

Figure 1-1. Cache Coherency (DMA Reads from SRAM)

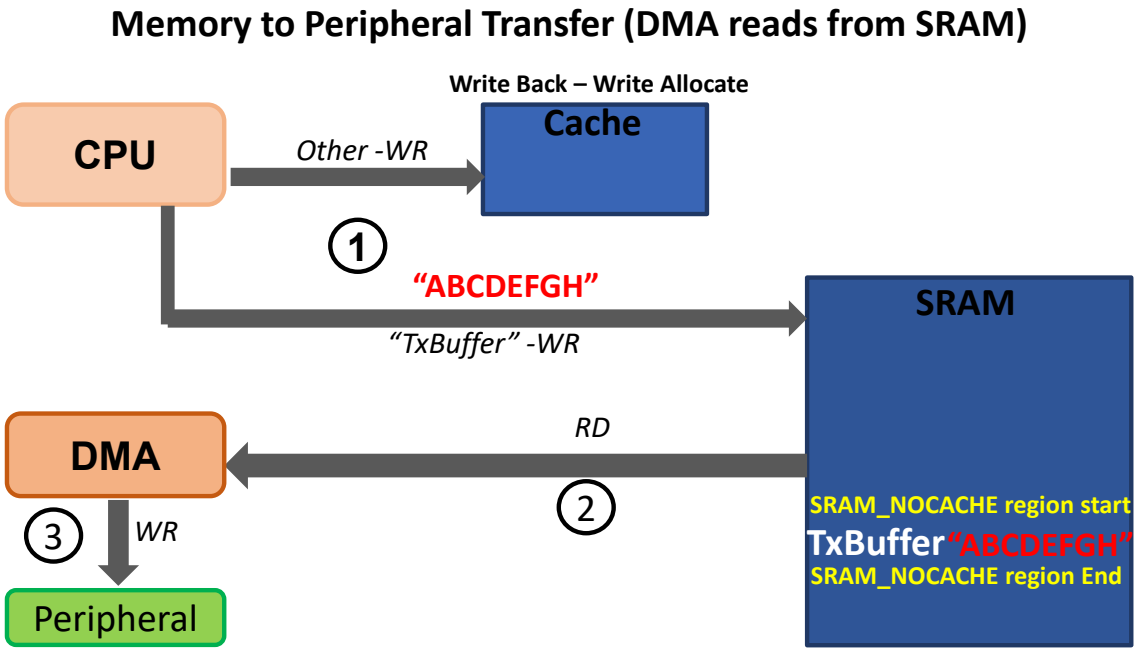


The application submits request to transfer the data buffer (TxBuffer) (value ABCDEFGH) to the peripheral. The CPU populates the DMA write buffer (TxBuffer) with the data to be written (value ABCDEFGH) to the peripheral. However, due to the set cache policy, *Write Back and Write Allocate,* the DMA write buffer (TxBuffer) is available in the data cache. Therefore, it is not updated to the main memory. The DMA write buffer (TxBuffer) in the main memory still contains the old value (12345678).

When the DMA is triggered to initiate the memory-to-peripheral transfer, the DMA reads the buffer (TxBuffer) from the main memory (12345678). As a result, the DMA ends up transferring stale data to the peripheral.

One of the ways to address the above cache coherency issue in the SAME70 MCU is to create a non-cacheable region and allocate the data in contention to the non-cacheable region. The following figure illustrates how the cache coherency issue observed in the figure above is addressed by creating a non-cacheable region.

Figure 1-2. Cache Coherency Solution (Non-Cacheable Region)



The user configures the Memory Protection Unit (MPU) in the SAME70 to not cache a part of the SRAM memory and allocates the DMA write buffer (TxBuffer) in the non-cacheable memory region.

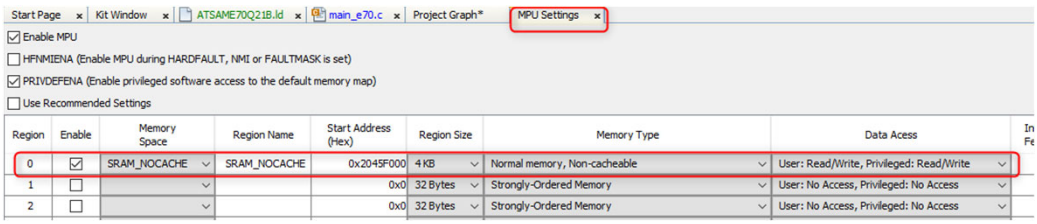
An access by the CPU to populate the DMA write buffer (TxBuffer) goes to the main memory as it is configured to be unavailable in the data cache. However, due to the set cache policy Write Back and Write Allocate, the other data accessed by the application continues to be cached.

When the DMA is triggered to initiate the memory-to-peripheral transfer, the DMA reads the buffer (TxBuffer) from the main memory (ABCDEFGH). As a result, the DMA transfers the correct data to the peripheral.

The following steps are used to create a non-cacheable region at address 0x2045F000 with a size of 4 Kb. The DMA write buffer (TxBuffer) will be allocated in this region.

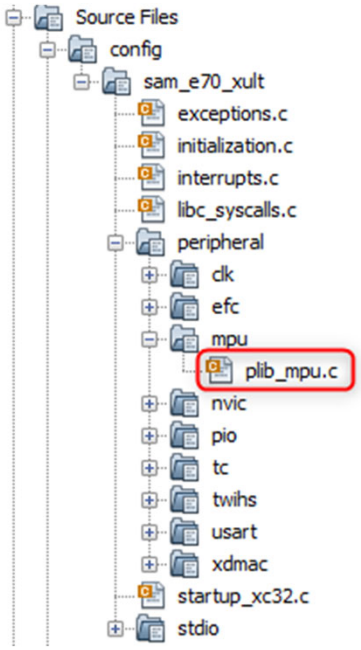
1. To configure a non-cacheable region using MPU Configurator, follow these steps:
   a. Open MPLAB Harmony v3 project and launch the MPLAB Code Configurator (MCC).
   b. To launch the MPU Configurator Window, in the MHC, select *Tools* > *MPU Configuration*.
   c. Configure the non-cacheable region as SRAM_NOCACHE as shown in the following figure:

   Figure 1-3. MPU settings - SRAM_NOCACHE Region



   d. Regenerate the MPLAB Harmony v3 project.
   e. If it is not present, the peripheral library (PLIB) for MPU is added to the project:

Figure 1-4. MPU PLIB



f. In the PLIB file, `plib_mpu.c`, the `MPU_Initialize` function has the following code added to configure the non-cacheable region:

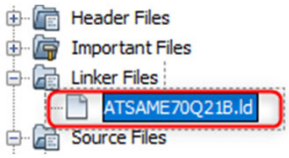
```
    /*** Configure MPU Regions  ***/

    /* Region 0 Name: SRAM_NOCACHE, Base Address: 0x2045f000, Size: 4KB  */
    MPU->RBAR = MPU_REGION(0, 0x2045f000);
    MPU->RASR = MPU_REGION_SIZE(11) |
MPU_RASR_AP(MPU_RASR_AP_READWRITE_Val) | MPU_ATTR_NORMAL \
                | MPU_ATTR_ENABLE | MPU_ATTR_EXECUTE_NEVER ;
```

g. The function `MPU_Initialize` is called from the source file, `startup_xc32.c`.

2. To create a non-cacheable SRAM section, the default linker script file used by the MPLAB Harmony v3 project must be customized.. To create a non-cacheable SRAM section in the linker script file, follow these steps.
   a. Depending on the MCU part selected in the MPLAB Harmony v3 project, the MPLAB X IDE uses the default linker script file available in the XC32 toolchain (compiler) path, available at `C:\Program Files (x86)\Microchip\xc32\v2.30\pic32c\lib\proc`.
   b. For the SAME70 MCU, the MPLAB Harmony v3 project with ATSAME70Q21B as the MCU uses the following linker script file `C:\Program Files (x86)\Microchip\xc32\v2.30\pic32c\lib\proc\ATSAME70Q21B\ATSAME70Q21B.ld`.
   c. Copy the default linker script file, `ATSAME70Q21B.ld`, and paste it in the src folder of the MPLAB Harmony v3 project.
   d. Add the linker script file in the src folder of the MPLAB Harmony v3 project in MPLAB X IDE under the ‘Linker Files’ as shown below.

Figure 1-5. Adding Linker Script



e. Add the following sections in the linker script file:

- Under Memory-Region Macro Definitions add the highlighted code:

```
#ifndef RAM_ORIGIN
#  define RAM_ORIGIN 0x20400000
#endif
#ifndef RAM_LENGTH
#  define RAM_LENGTH 0x60000
#elif (RAM_LENGTH > 0x60000)
#  error RAM_LENGTH is greater than the max size of 0x60000
#endif

#ifndef SRAM_NOCACHE
#  define SRAM_NOCACHE 0x2045F000
#endif
#ifndef SRAM_NOCACHE_LENGTH
#  define SRAM_NOCACHE_LENGTH 0x1000
#elif (SRAM_NOCACHE_LENGTH > 0x60000)
#  error SRAM_NOCACHE_LENGTH is greater than the max size of 0x60000
#endif
```

- Under Memory-Region Definitions add the highlighted code:

```
MEMORY
{
  rom (LRX) : ORIGIN = ROM_ORIGIN, LENGTH = ROM_LENGTH
  ram (WX!R) : ORIGIN = RAM_ORIGIN, LENGTH = RAM_LENGTH-
__XC32_ITCM_LENGTH-__XC32_DTCM_LENGTH
  ram_nocache (RWX) : ORIGIN = SRAM_NOCACHE, LENGTH =
SRAM_NOCACHE_LENGTH
  itcm (WX) : ORIGIN = ITCM_ORIGIN, LENGTH = __XC32_ITCM_LENGTH
  dtcm (WX!R) : ORIGIN = DTCM_ORIGIN, LENGTH = __XC32_DTCM_LENGTH
  config_D0000000 : ORIGIN = 0xD0000000, LENGTH = 0x4
  config_D0000004 : ORIGIN = 0xD0000004, LENGTH = 0x4
  config_D0000008 : ORIGIN = 0xD0000008, LENGTH = 0x4
  config_D000000C : ORIGIN = 0xD000000C, LENGTH = 0x4
  config_D0000010 : ORIGIN = 0xD0000010, LENGTH = 0x4

}
```

- Under Section Definitions add the highlighted code:

```
    .vectors :
    {
        . = ALIGN(4);
        _sfixed = .;

KEEP(*(.vectors .vectors.* .vectors_default .vectors_default.*))
        KEEP(*(.isr_vector))
        KEEP(*(.reset*))
        KEEP(*(.after_vectors))
    } > VECTOR_REGION

    .ram_nocache (NOLOAD):
    {
        . = ALIGN(4);
        _s_ram_nocache = .;
```

```
        *(.ram_nocache .ram_nocache.*)
          . = ALIGN(4);
        _e_ram_nocache = .;
    } > ram_nocache
```

- Save the custom linker script file, `ATSAME70Q21B.ld`.

3. Assigning the DMA write buffer (TxBuffer) in the non-cacheable region.
   In the application code, while declaring the DMA write buffer (TxBuffer), use the attribute as shown below to allocate it in the non-cacheable region:

```
uint8_t __attribute__ ((section (".ram_nocache")))TxBuffer[100] = {0};
```

   The application uses the DMA write buffer (TxBuffer) in the DMA transfer APIs:

```
 XDMAC_ChannelTransfer(XDMAC_CHANNEL_0, TxBuffer,
                       (const void *)&(USART1_REGS->US_THR), strlen((const
char*)TxBuffer));
```

The following are non-cacheable region approach to address the cache coherence issues:

- Keeps the application simple.
- No explicit cache management is required.
- No requirement for buffer alignment and buffer size.

Though the non-cacheable region approach provides the above benefits, it comes with a cost of some performance degradation as the coherent or non-cached data can only be accessed from the main memory.

2. References

1. Managing Cache Coherency on Cortex-M7 Based MCUs: ww1.microchip.com/downloads/en/DeviceDoc/Managing-Cache-Coherency-on-Cortex-M7-Based-MCUs-DS90003195A.pdf.
2. Arm Cortex-M7 Processor Technical Reference Manual: infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0489d/Chdcghid.html.
3. Usage of XDMAC on SAM S/SAM E/SAM V: www.microchip.com/wwwappnotes/appnotes.aspx?appnote=en592128.

3. Revision History

Revision B - 09/2022
The following updates were performed in this revision:

- Corrected typographical errors
- Updated `ram_nocache` code in Description for line item 2.5

Revision A - 04/2020
This is the initial released version of the document.

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