AVR 8-bit Microcontrollers

AT06609: Differences between ATmega48/88/168 Variants and the new ATmega48/88/168PB

APPLICATION NOTE

Introduction

This application note assists users of Atmel® ATmega48/88/168 variants to understand the differences and use of the Atmel ATmega48/88/168PB.

ATmega48/88/168PB is not a drop-in replacement for ATmega48/88/168 variants, but a new device. However, the functions are backward compatible with the existing ATmega48/88/168 functions. Existing code for these devices will work in the new devices without changing existing configuration or enabling new functions. The code that is available for your existing ATmega48/88/168 variants will continue to work on the new ATmega48/88/168PB device.

For differences in errata, typical, and electrical characteristics between ATmega48/88/168 variants and ATmega48/88/168PB, refer to the specific device datasheets.

For complete device details, refer to the latest version of the ATmega48/88/168PB datasheet available at http://www.atmel.com.

Features

- Pin functionality difference
- Code compatibility
- Enhancement and added features
- Updated features

Note: Code compiled for ATmega48/88/168 variants are compatible and can be executed in the ATmega48/88/168PB device (exception, see this application note). Whereas, reverse code compatibility is not guaranteed.

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1. Pin Functionality Difference

1.1. Added/Modified Pin Functionality

ATmega48/88/168PB supports four additional GPIOs on PORTE [3:0].

GPIO pins PE2 and PE3 are added to Pin19 and Pin22. PE2 and PE3 are multiplexed with ADC6 and ADC7.

Pin3 (GND) and Pin6 (VCC) are replaced by PE0 and PE1 respectively. PE0 is multiplexed with ACO.

Table 1-1. Pin Functionality Difference between ATmega48/88/168 Variants and ATmega48/88/168PB

32-pin TQFP/MLF package	ATmega48/88/168 variants	ATmega48/88/168PB
Pin3	GND	PE0/ACO
Pin6	VCC	PE1
Pin19	ADC6	ADC6/PE2
Pin22	ADC7	ADC7/PE3

1.2. Alternate Pin Configuration

The alternate pin configurations are:

- **ADC7– Port E, Bit 3**
  PE3 can also be used as ADC input channel 7.
  Note: ADC input channel 7 uses analog power AVCC.
- **ADC6 – Port E, Bit 2**
  PE2 can also be used as ADC input channel 6.
  Note: ADC input channel 6 uses analog power AVCC.
- **None – Port E, Bit 1**
  No alternate function.
- **ACO – Port E, Bit 0**
  ACO Analog Compare Output pin is multiplexed with PE0.

1.3. Register Description

1.3.1. PINE – Port E Input Pins Address

Name: PINE
Offset: 0x2C
Reset: N/A
Property: When addressing as I/O Register: address offset is 0x0C

Bit	7	6	5	4	3	2	1	0
					PINE3	PINE2	PINE1	PINE0
Access					R/W	R/W	R/W	R/W
Reset					x	x	x	x

Bit 3 – PINE3: Port E Input Pin Address 3
Writing to the pin register provides toggle functionality for I/O.

Bit 2 – PINE2: Port E Input Pin Address 2
Writing to the pin register provides toggle functionality for I/O.

Bit 1 – PINE1: Port E Input Pin Address 1
Writing to the pin register provides toggle functionality for I/O.

Bit 0 – PINE0: Port E Input Pin Address 0
Writing to the pin register provides toggle functionality for I/O.

1.3.2. DDRE – Port E Data Direction Register

Name: DDRE
Offset: 0x2D
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x0D

Bit	7	6	5	4	3	2	1	0
					DDRE3	DDRE2	DDRE1	DDRE0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – DDRE3: Port E Data Direction 3

Bit 2 – DDRE2: Port E Data Direction 2

Bit 1 – DDRE1: Port E Data Direction 1

Bit 0 – DDRE0: Port E Data Direction 0

1.3.3. PORTE – Port E Data Register

Name: PORTE
Offset: 0x2E
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x0E

Bit	7	6	5	4	3	2	1	0
					PORTE3	PORTE2	PORTE1	PORTE0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – PORTE3: Port E Data 3

Bit 2 – PORTE2: Port E Data 2

Bit 1 – PORTE1: Port E Data 1

Bit 0 – PORTE0: Port E Data 0

2. Code Compatibility

ATmega48/88/168 variants are code compatible with ATmega48/88/168PB devices. Code compiled for ATmega48/88/168 variants will execute the same in the ATmega48/88/168PB device whereas reverse code compatibility is not guaranteed.

3. Enhancement and Added Features

This chapter summarizes the enhancements or added features in ATmega48/88/168PB compared with ATmega48/88/168 variants.

- USART start frame detection is available in all sleep modes
- Analog Comparator output is available on a pin. This pin is multiplexed with PE0.
- Serial Number (unique device ID) to identify the device

3.1. USART

In addition to the existing wake-up modes, ATmega48/88/168PB USART start-of-frame detection can also wake up the MCU from all sleep modes when a start bit is detected.

When a high-to-low transition is detected on RxDn, the internal 8MHz oscillator is powered up and the USART clock is enabled. After start-up the rest of the data frame can be received, provided that the baud rate is slow enough to allow the internal 8MHz oscillator to start up. Start-up time of the internal 8MHz oscillator varies with supply voltage and temperature.

The USART start frame detection works both in asynchronous and synchronous modes. It is enabled by writing a one to the Start Frame Detection Enable bit (SFDE) in “UCSRD – USART Control and Status Register D”. If the USART RX Start- Interrupt Enable (RXSIE) bit is set, the USART Receive Start Interrupt is generated immediately when a start is detected.

When using the feature without the Receive Start Interrupt, the start detection logic activates the internal 8MHz oscillator and the USART clock while the frame is being received only. Other clocks remain stopped until the Receive Complete Interrupt optionally wakes up the MCU.

The maximum baud rate in synchronous mode depends on the sleep mode the device is woken up from, as follows:

- Idle or ADC Noise Reduction sleep mode: system clock frequency divided by four
- Standby or Power-down: 500kbps

The maximum baud rate in asynchronous mode depends on the sleep mode the device is woken up from, as follows:

- Idle sleep mode: the same as in active mode

3.1.1. UCSRD – USART Control and Status Register D

Name: UCSRD
Offset: 0xC3
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	RXIE	RXS	SFDE					
Access	R/W	R/W	R/W					
Reset	0	0	0					

Bit 7 – RXIE: USART RX Start Interrupt Enable
Writing this bit to one enables the interrupt on the RXS flag. In sleep modes this bit enables start frame detector that can wake up the MCU when a start condition is detected on the RxD line. The USART RX Start Interrupt is generated only if the RXSIE bit, the Global Interrupt flag, and RXS are set.

Bit 6 – RXS: USART RX Start
The RXS flag is set when a start condition is detected on the RxD line. If the RXSIE bit and the Global Interrupt Enable flag are set, an RX Start Interrupt will be generated when the flag is set. The flag can only be cleared by writing a logical one on the RXS bit location.

If the start frame detector is enabled (RXSIE = 1) and the Global Interrupt Enable flag is set, the RX Start Interrupt will wake up the MCU from all sleep modes.

Bit 5 – SFDE: Start Frame Detection Enable
Writing this bit to one enables the USART Start Frame Detection mode. The start frame detector is able to wake up the MCU from sleep mode when a start condition, i.e. a high (IDLE) to low (START) transition, is detected on the RxD line.

Table 3-1. USART Start Frame Detection Modes

SFDE	RXSIE	RXSIE (RX complete interrupt enable)	Description
0	x	x	Start frame detection disabled
1	0	0	Reserved
1	0	1	Start frame detector enabled. RXC flag wakeup the MCU from all sleep mode
1	1	0	Start of frame detector enabled. RXS flag wakeup the MCU from all sleep mode

3.2. Analog Comparator

Analog comparator output is available on a pin. The analog comparator's output is tied to PE0 when the AC output is enabled by writing a one to the Analog Comparator Output Enable bit (ACOE) in “ACSR0 – Analog Comparator Output Control Register”.

3.2.1. ACSR0 – Analog Comparator Control and Status Register

Name: ACSR0
Offset: 0x4F
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x2F

Bit	7	6	5	4	3	2	1	0
								ACOE
Access								R/W
Reset								0

Bit 0 – ACOE: Analog Comparator Output Enable
Setting this bit makes the output of AC available on PE0. If this bit is not set, PE0 can be used as general I/O pin.

3.3. Serial Number

In Atmel ATmega48/88/168PB, the serial number (also called unique device ID) is to identify each individual part. There are two approaches to get the serial number information.

One way is to read the Signature Row from software. For detailed information, refer to section "Reading the Signature Row from Software" of the latest datasheet.

Table 3-2. Signature Row Addressing

Signature byte	Z-pointer address
Device Signature Byte 1	0x0000
Device Signature Byte 2	0x0002
Device Signature Byte 3	0x0004
RC Oscillator Calibration Byte	0x0001
Serial Number Byte 1	0x000E
Serial Number Byte 0	0x000F
Serial Number Byte 3	0x0010
Serial Number Byte 2	0x0011
Serial Number Byte 5	0x0012
Serial Number Byte 4	0x0013
Serial Number Byte 6	0x0015
Serial Number Byte 7	0x0016
Serial Number Byte 8	0x0017

Another way is to read I/O address 0xF0 - 0xF8, as the ATmega48/88/168PB serial number can be accessible through I/O registers SNOBRx. The serial number is made from concatenating the nine bytes read out from these read-only registers. See registers below for more detail.

3.3.1. Serial Number byte 0

Name: SNOBR0
Offset: 0xF3
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 0 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 0 [7:0]: Serial Number byte 0

3.3.2. Serial Number byte 1

Name: SNOBR1
Offset: 0xF4
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 1 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 1 [7:0]: Serial Number byte 1

3.3.3. Serial Number byte 2

Name: SNOBR2
Offset: 0xF5
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 2 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 2 [7:0]: Serial Number byte 2

3.3.4. Serial Number byte 3

Name: SNOBR3
Offset: 0xF6
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 3 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 3 [7:0]: Serial Number byte 3

3.3.5. Serial Number byte 4

Name: SNOBR4
Offset: 0xF7
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 4 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 4 [7:0]: Serial Number byte 4

3.3.6. Serial Number byte 5

Name: SNOBR5
Offset: 0xF8
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 5 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 5 [7:0]: Serial Number byte 5

3.3.7. Serial Number byte 6

Name: SNOBR6
Offset: 0xF2
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 6 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 6 [7:0]: Serial Number byte 6

3.3.8. Serial Number byte 7

Name: SNOBR7
Offset: 0xF1
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 7 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 7 [7:0]: Serial Number byte 7

3.3.9. Serial Number byte 8

Name: SNOBR8
Offset: 0xF0
Reset: Serial Number value
Property: --

Bit	7	6	5	4	3	2	1	0
	Serial Number byte 8 [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – Serial Number byte 8 [7:0]: Serial Number byte 8

4. Updated Features

4.1. Full Swing Oscillator

Clock source options of the ATmega48/88/168 variants include full swing crystal oscillator, which can be selected by configuring the flash fuse. However, in the new ATmega48/88/168PB, the full swing crystal oscillator is removed. Refer to the "Clock Sources" chapter of relative datasheet.

Table 4-1. Full Swing Oscillator Removed from ATmega48/88/168PB

Device function	ATmega48/88/168PB	ATmega48/88/168 variants
Full swing crystal oscillator	No	Yes

4.2. Parallel Programming

Parallel programming timing in ATmega48/88/168PB has been modified, comparing with ATmega48/88/168 variants. See below table "Parallel programming timing differences" in detail.

Table 4-2. Parallel Programming Timing Differences

Symbol	Parameter	ATmega48/88/168PB		ATmega48/88/168 Variants		Units
		Min.	Max.	Min.	Max.	
t_{WLRH}	WR Low to RDY/BSY High	3.2	3.4	3.7	4.5	ms
t_{WLRH_CE}	WR Low to RDY/BSY High for Chip Erase	9.8	10.5	7.5	9	ms
t_{BVDV}	BS1 Valid to DATA valid	--	350	--	250	ns
t_{OLDV}	OE Low to DATA Valid	--	350	--	250	ns

4.3. Power Save Mode

Power consumption in power save modes for ATmega48/88/168PB will be higher when comparing with the device ATmega48/88/168 variants. For more detail, refer to the relative datasheets.

4.4. NVM

Write wait delay for NVM in ATmega48/88/168PB is increased when comparing with ATmega48/88/168 variants.

Table 4-3. Minimum wait delay for NVM

Symbol	ATmega48/88/168PB	ATmega48/88/168 variants	Unit
t_{WD_FLASH}	2.6	4.5	ms
t_{WD_EEPROM}	3.6	3.6	ms
t_{WD_ERASE}	10.5	9	ms
t_{WD_FUSE}	4.5	--	ms

4.5. Signature Bytes

All Atmel microcontrollers have a three-byte signature code, which identifies the device. This code can be read in both serial and parallel mode, also when the device is locked. The three bytes reside in a separate address space. For the device signature bytes, there are differences between ATmega48/88/168PB and ATmega48/88/168 variants, see the table below for more detail.

Table 4-4. Device ID Differences

Part	Signature bytes address		
	0x000	0x001	0x002
ATmega48	0x1E	0x92	0x05
ATmega48PB	0x1E	0x92	0x10
ATmega88	0x1E	0x93	0x0A
ATmega88PB	0x1E	0x93	0x16
ATmega168	0x1E	0x94	0x06
ATmega168PB	0x1E	0x94	0x15

5. Other Related Documents

Refer the following migration notes to know the changes between Atmel ATmega48/88/168 and ATmega48/88/168P, and ATmega48/88/168P and ATmega48/88/168PA.

Atmel AVR®512: Migration from ATmega48/88/168 to ATmega48P/88P/168P

Atmel AVR528: Migration from ATmega48/88/168P to ATmega48/88/168PA

6. Revision History

Doc Rev.	Date	Comments
42374C	09/2016	A minor change of the table setup in Section Signature Bytes
42374B	08/2016	Added "Updated features"
42374A	10/2014	Initial document release

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 / Rev.: Atmel-42374C-Differences-between-ATmega48/88/168-Variants-and-the-new-ATmega48/88/168PB_AT06609_Application Note-09/2016