SY58011U

7 GHz, 1:2 CML Fanout Buffer/Translator with Internal I/O Termination

Features

- Precision 1:2, 400 mV CML Fanout Buffer
- Low Jitter Performance:
  - 49 fs_{RMS} Phase Jitter (typ)
- Guaranteed AC Performance Over Temperature/ Voltage:
  - > 7 GHz f_{MAX} Clock
  - < 60 ps t_r / t_f Times
  - < 250 ps t_{pd}
  - < 15 ps Max. Skew
- Accepts an Input Signal as Low as 100 mV
- Unique Input Termination and V_T Pin Accepts DC-coupled and AC-coupled Differential Inputs: LVPECL, LVDS, and CML
- 50Ω Source Terminated CML Outputs
- Power Supply 2.5V ±5% and 3.3V ±10%
- Industrial Temperature Range: –40°C to +85°C
- Available in 16-lead (3 mm × 3 mm) VQFN Package

Applications

- All SONET and GigE Clock Distribution
- Fibre Channel Clock and Data Distribution
- Backplanes
- Data Distribution: OC-48, OC-48+FEC, XAUI
- High-end, Low Skew, Multiprocessor Synchronous Clock Distribution

General Description

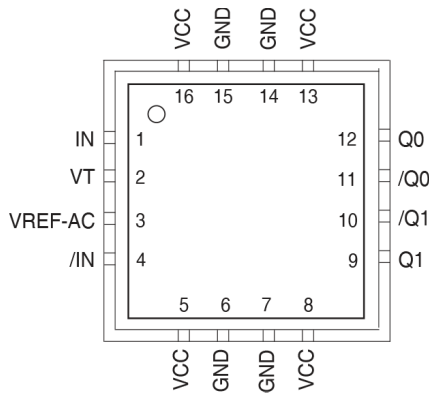
The SY58011U is a 2.5V/3.3V precision, high-speed, fully differential 1:2 CML fanout buffer. Optimized to provide two identical output copies with less than 15 ps of skew and only 49 fs_{RMS} phase jitter, the SY58011U can process clock signals as fast as 7 GHz or data patterns up to 10.7 Gbps.

The differential input includes Microchip's unique, 3-lead input termination architecture that interfaces to LVPECL, LVDS, or CML differential signals, (AC-coupled or DC-coupled) as small as 100 mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the VT pin. The outputs are compatible with 400 mV typical swing into 50Ω loads, with extremely fast rise/fall times guaranteed to be less than 60 ps.

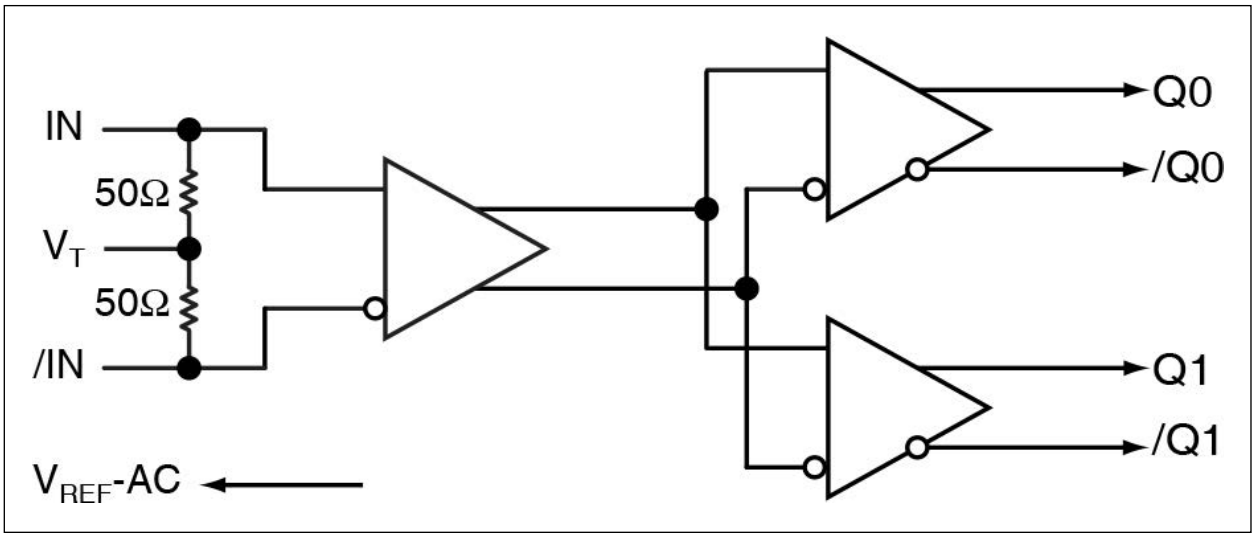
The SY58011U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL outputs, consider the SY58012U or SY58013U 1:2 fanout buffer with 800 mV and 400 mV output swing, respectively. The SY58011U is part of Microchip's high-speed Precision Edge® product line.

Package Type

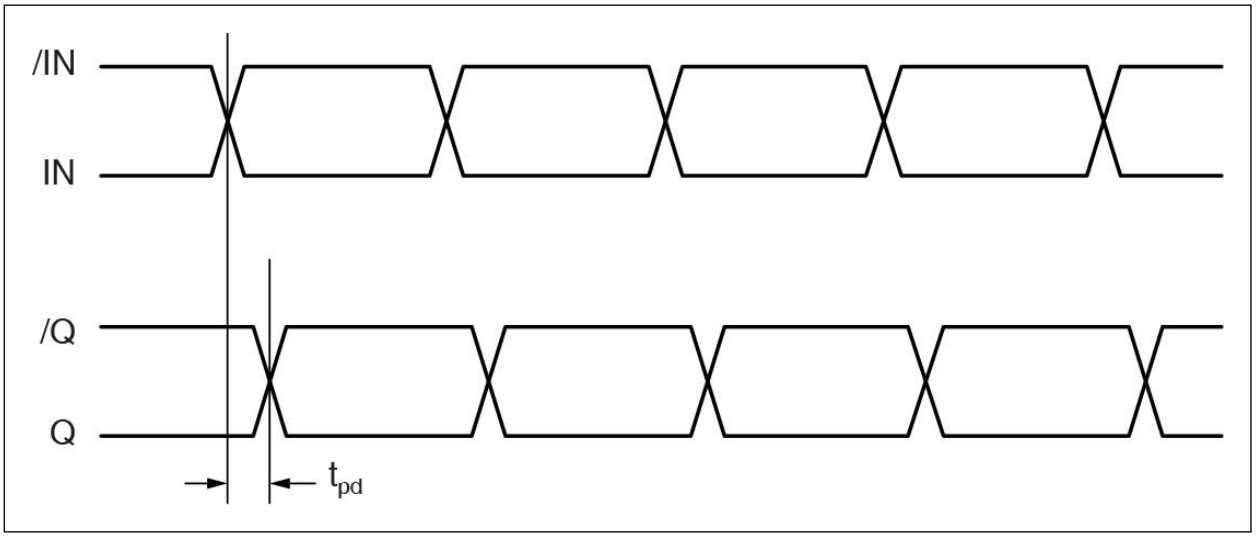
SY58011U
16-Lead VQFN



Functional Block Diagram



Timing Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC} – 1.0V to V_{CC} + 0.5V
Current (V_T), Source or Sink Current on VT Pin ..... ±100 mA
Input Current, Source or Sink Current on IN, /IN ..... ±50 mA
Current (V_{REF}), Source or sink current on V_{REF-AC} (Note 1) ..... ±1.5 mA

Operating Ratings††

Supply Voltage (V_{CC}) ..... +2.375V to +3.60V
Operating Temperature Range (T_A) ..... –40°C to +85°C

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	2.375	—	3.60	V	—
Power Supply Current	I_{CC}	—	75	95	mA	No load, max. V_{CC}
Input HIGH Voltage	V_{IH}	V_{CC} – 1.6	—	V_{CC}	V	IN, /IN, Note 2
Input LOW Voltage	V_{IL}	0	—	V_{IH} – 0.1	V	IN, /IN
Input Voltage Swing	V_{IN}	0.1	—	1.7	V	See Figure 7-1
Differential Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	See Figure 7-2
Into VT Resistance	R_{IN}	40	50	60	y	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—
	IN to V_T	—	—	1.28	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: V_{IH} (min) not lower than 1.2V.

TABLE 1-2: CML DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C; R_L = 100Ω across each output pair, or equivalent, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	V_{CC} – 0.020	V_{CC} – 0.010	V_{CC}	V	Q0, /Q0, Q1, /Q1
Output Voltage Swing	V_{OUT}	325	400	—	mV	Q0, /Q0, Q1, /Q1; see Figure 7-1
Differential Output Voltage Swing	V_{DIFF_OUT}	650	800	—	mV	Q0, /Q0, Q1, /Q1; see Figure 7-2
Output Source Impedance	R_{OUT}	40	50	60	Ω	Q0, /Q0, Q1, /Q1

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across each output pair, or equivalent, unless otherwise stated. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Operating Frequency	f_{MAX}	—	10.7	—	Gbps	NRZ Data
		7	8	—	GHz	V_{OUT} > 200 mV
Propagation Delay	t_{pd}	100	170	250	ps	V_{IN} > 100 mV
Channel-to-Channel Skew	t_{CHAN}	—	3	15	ps	Note 2
Part-to-Part Skew	t_{SKEW}	—	—	100	ps	Note 3
RMS Phase Jitter	t_{JITTER}	—	49	—	fs_{RMS}	Output = 622 MHz, Integration Range: 12 kHz–20 MHz
Output Rise/Fall Time	t_r, t_f	20	40	60	ps	20%–80% at full output swing

Note 1: High frequency AC electricals are guaranteed by design and characterization.

2: Skew is measured between outputs of the same bank under identical transitions.

3: Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	260	—	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 1)						
VQFN, Still Air (junction to ambient)	θ_{JA}	—	60	—	°C/W	—
VQFN, 500 lfpm (junction to ambient)	θ_{JA}	—	54	—	°C/W	—
VQFN (junction to top-center)	Ψ_{JB}	—	33	—	°C/W	—

Note 1: Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the pcb.

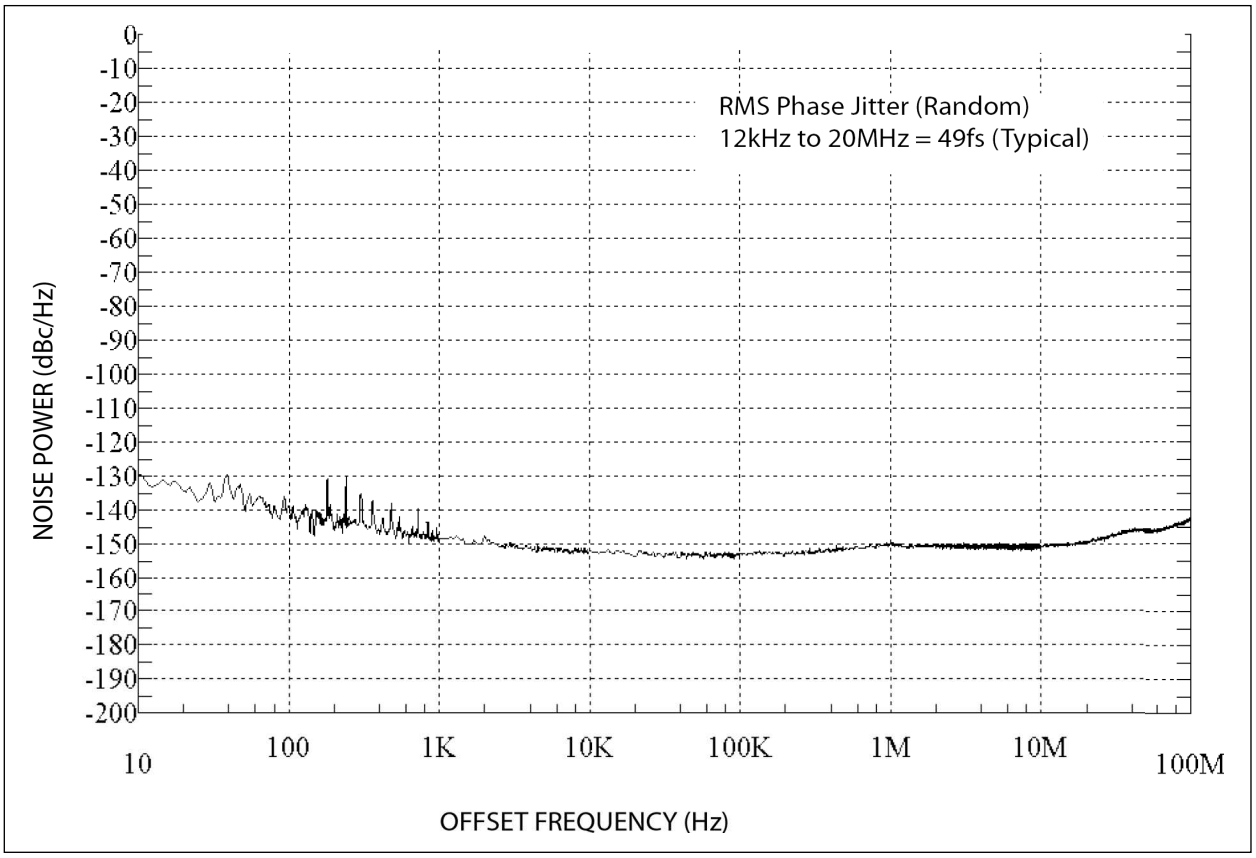
2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 4	IN, /IN	**Differential Input.** This input pair is the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section.
2	VT	**Input Termination Center-Tap.** Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See “Input Interface Applications” section.
3	VREF-AC	**Reference Output Voltage.** This output biases to V_{CC} –1.2V. It is used when AC-coupling the inputs (IN, /IN). Connect VREF-AC directly to the VT pin. Bypass with 0.01 µF low ESR capacitor to VCC. Maximum current source or sink is 0.5 mA. See “Input Interface Applications” section.
5, 8, 13, 16	VCC	**Positive Power Supply.** Bypass with 0.1 µF//0.01 µF low ESR capacitors as close to the VCC pins as possible.
6, 7, 14, 15	GND (Exposed Pad)	**Ground.** Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
12, 11	Q0, /Q0	**CML Differential Output Pairs.** Differential buffered output copy of the input signal. The output swing is typically 400 mV. Unused output pairs may be left floating with no impact on jitter. See “CML Output Termination” section.
9, 10	Q1, /Q1	

3.0 PHASE NOISE PLOT: 622 MHZ @ 3.3V



4.0 TYPICAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100 mV, T_A = 25°C, unless otherwise stated.

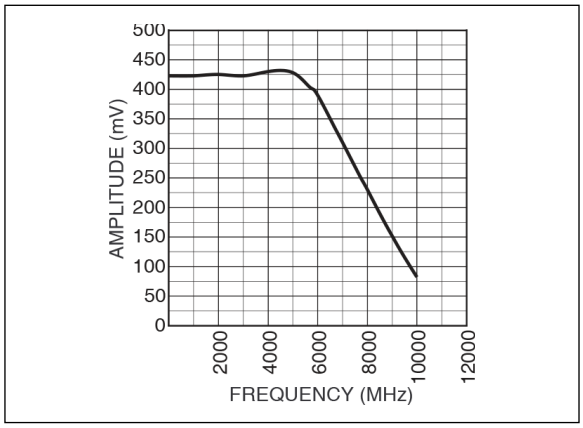


FIGURE 4-1: FREQUENCY VS. AMPLITUDE.

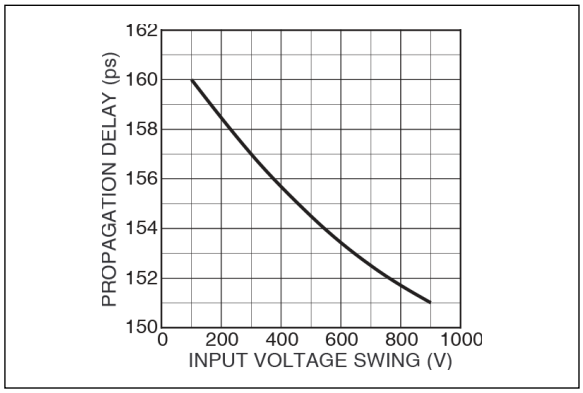


FIGURE 4-3: PROPAGATION DELAY VS. INPUT VOLTAGE SWING.

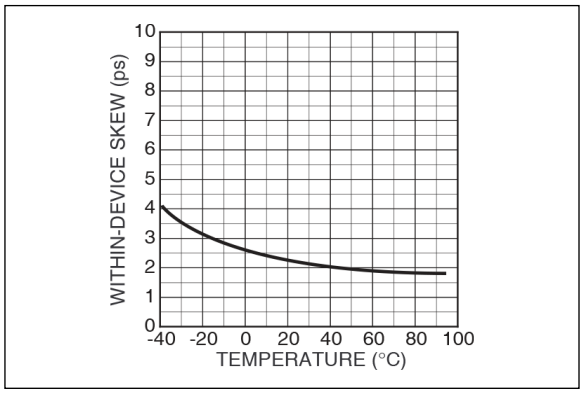


FIGURE 4-2: WITHIN-DEVICE SKEW VS. TEMPERATURE.

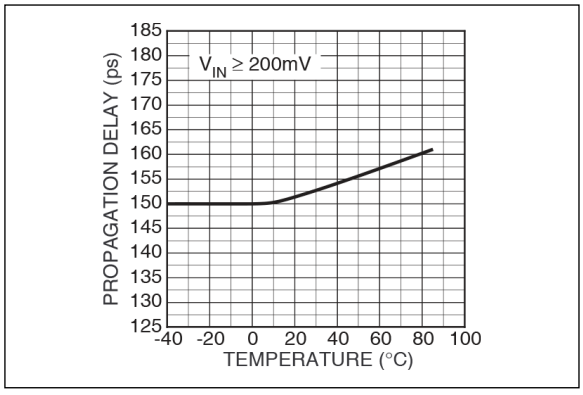


FIGURE 4-4: PROPAGATION DELAY VS. TEMPERATURE.

5.0 FUNCTIONAL CHARACTERISTICS

Typical output waveforms. V_{CC} = 2.5V; GND = 0V; V_{IN} = 100 mV; T_A = 25°C, unless otherwise noted.

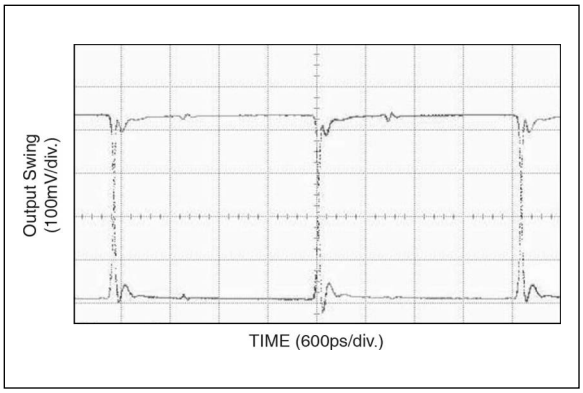


FIGURE 5-1: 200 MHZ OUTPUT.

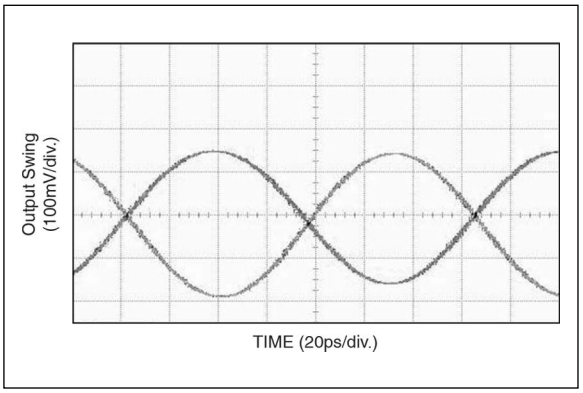


FIGURE 5-3: 7 GHZ OUTPUT.

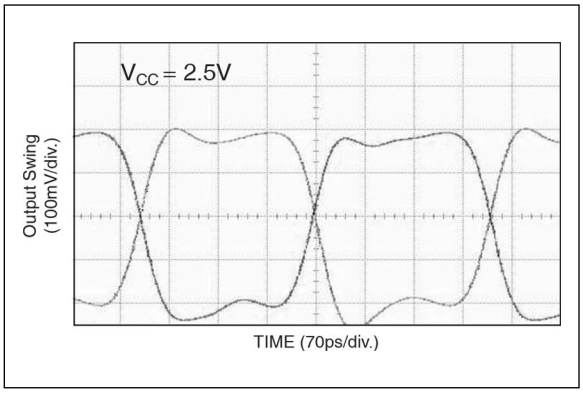


FIGURE 5-2: 2 GHZ OUTPUT.

6.0 INPUT STAGE

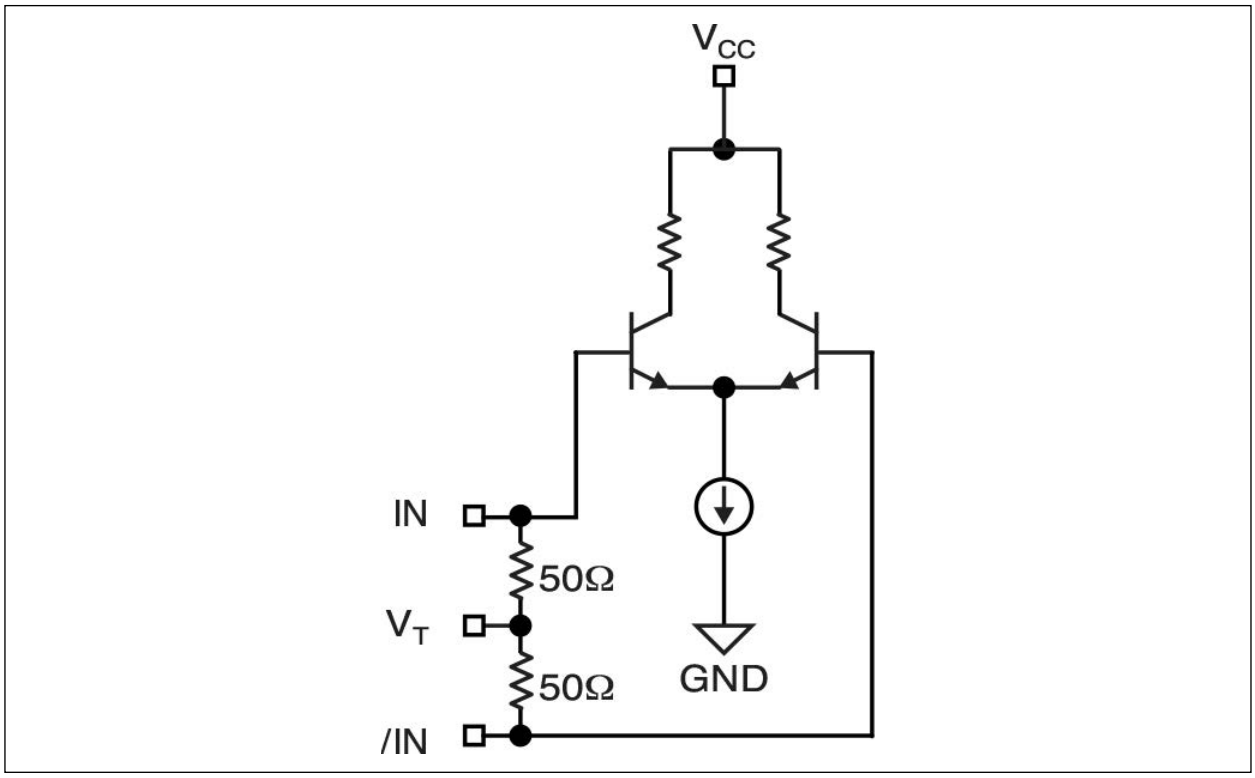


FIGURE 6-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.

7.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

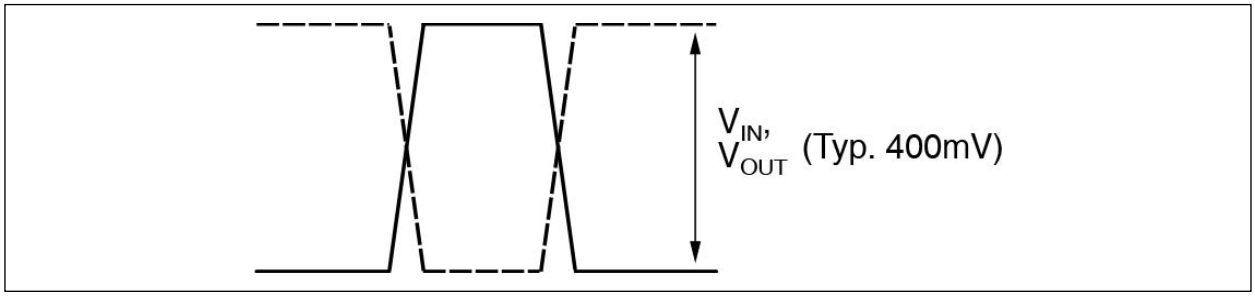


FIGURE 7-1: SINGLE-ENDED VOLTAGE SWING.

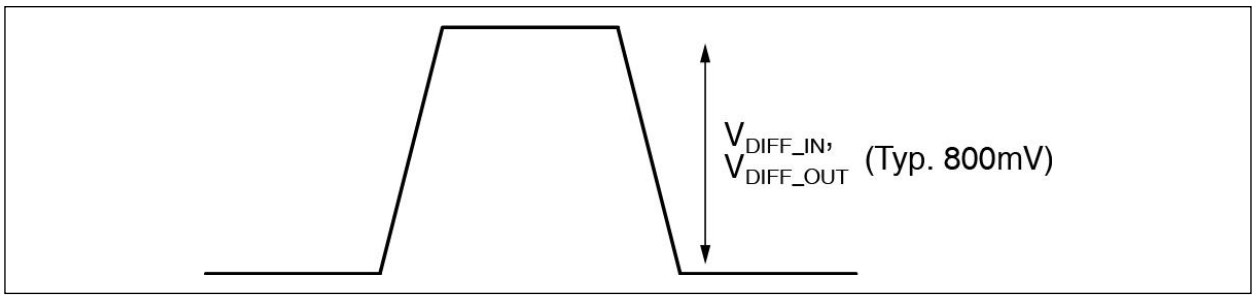


FIGURE 7-2: DIFFERENTIAL VOLTAGE SWING.

8.0 INPUT INTERFACE APPLICATIONS

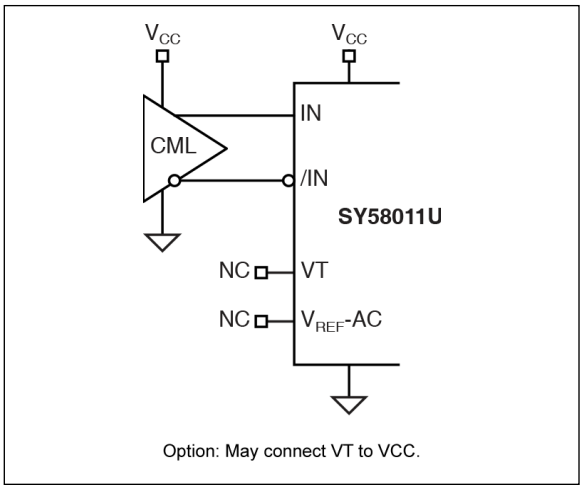


FIGURE 8-1: DC-COUPLED CML INPUT INTERFACE.

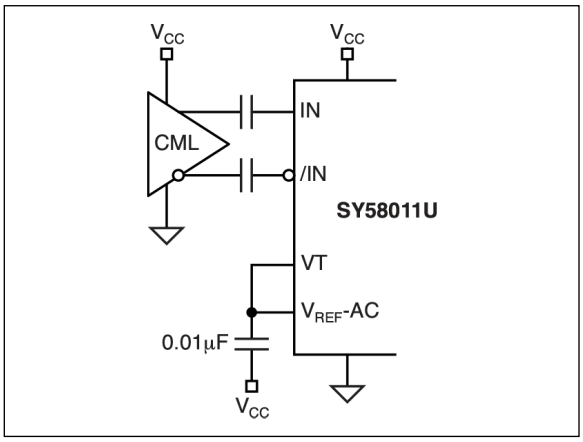


FIGURE 8-2: AC-COUPLED CML INPUT INTERFACE.

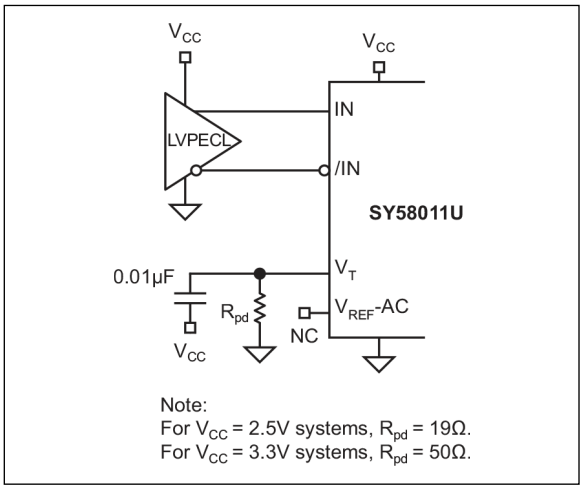


FIGURE 8-3: DC-COUPLED LVPECL INPUT INTERFACE.

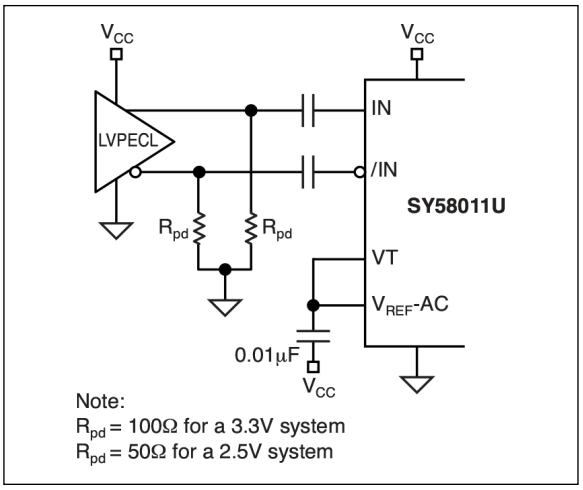


FIGURE 8-4: AC-COUPLED LVPECL INPUT INTERFACE.

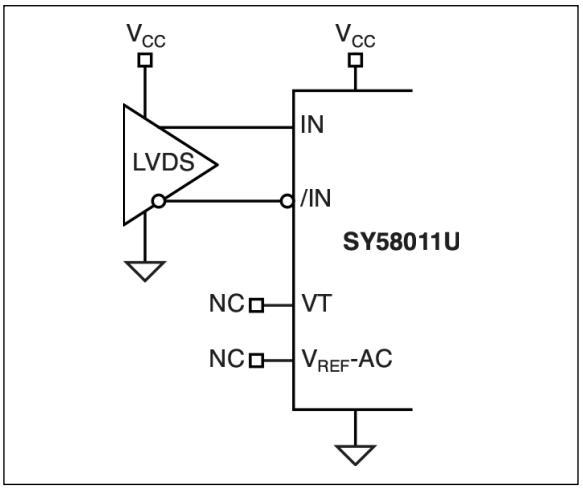


FIGURE 8-5: DC-COUPLED LVDS INPUT INTERFACE.

9.0 CML OUTPUT TERMINATION

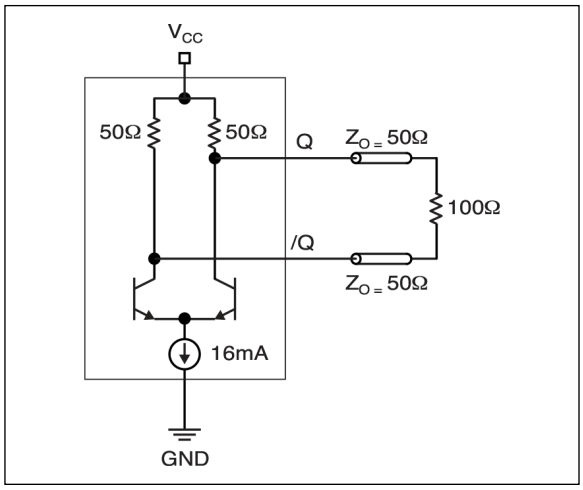


FIGURE 9-1: CML DC-COUPLED TERMINATION.

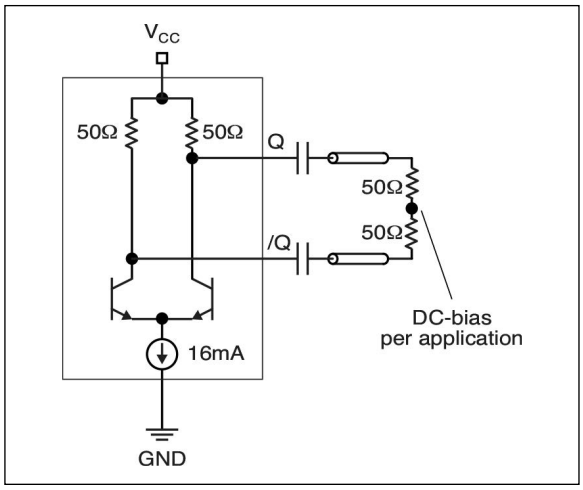
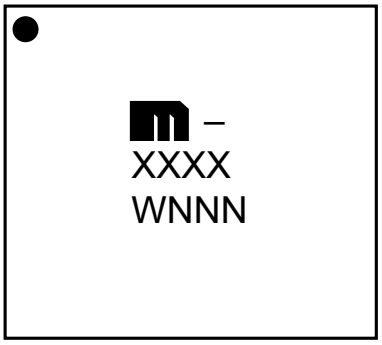


FIGURE 9-2: CML AC-COUPLED TERMINATION.

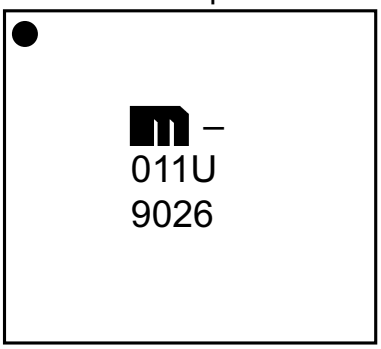
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

16-Lead VQFN*



Example*



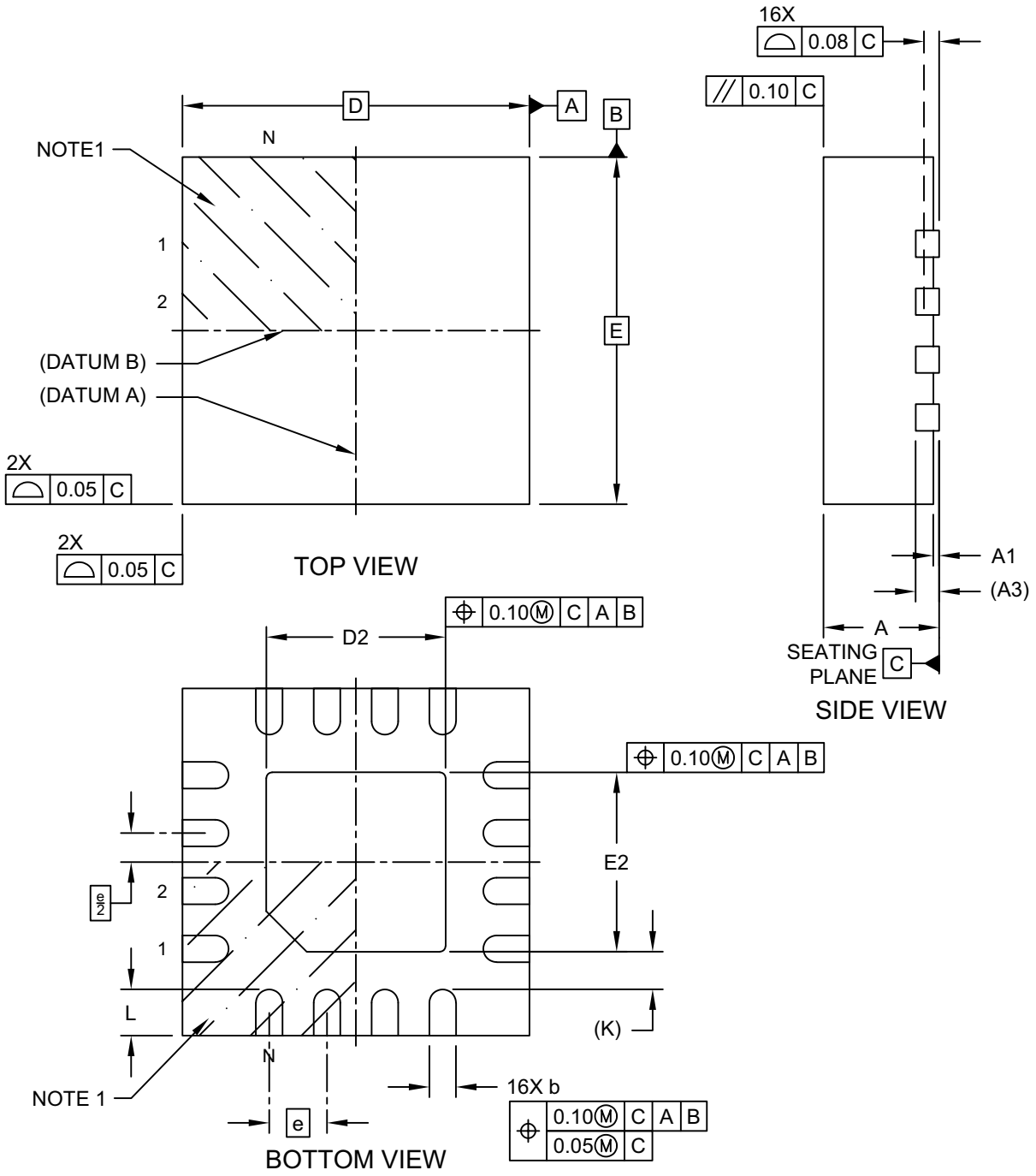
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

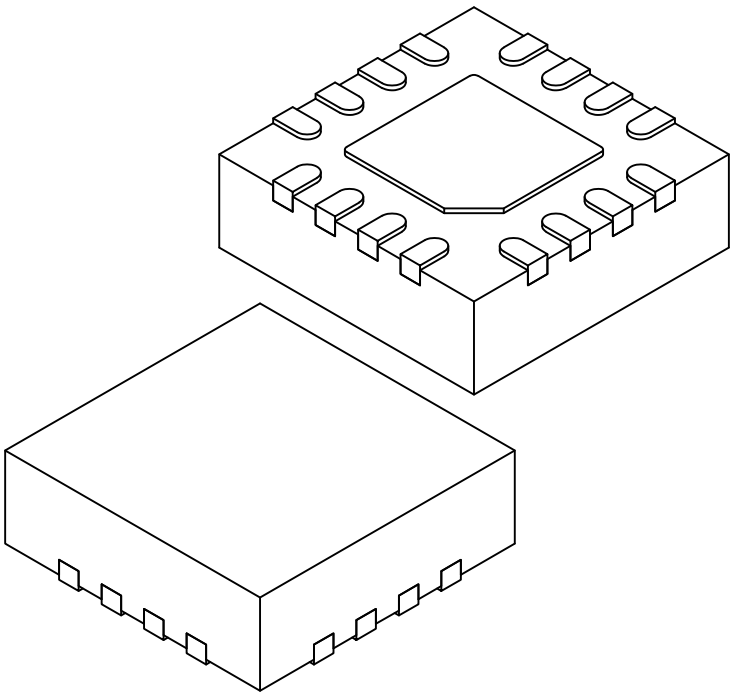
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

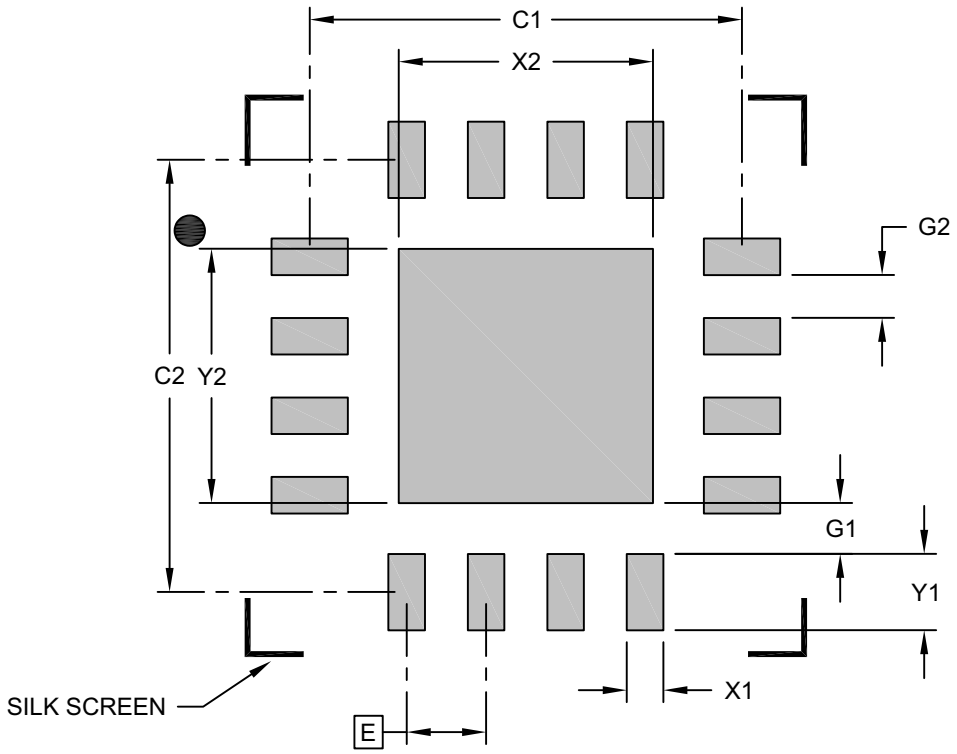
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2025)

- Converted Micrel data sheet for SY58011U to Microchip format as DS20006864A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY58011	=	7 GHz, 1:2 CML Fanout Buffer/ Translator with Internal I/O Termination (Precision Edge®)
Voltage Option:	U	=	2.5V/3.3V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	-TR	=	1,000/Tape & Reel

Examples:

a) **SY58011UMG**

2.5V/3.3V, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY58011UMG-TR**

2.5V/3.3V, 16-Lead VQFN, –40°C to 85°C, 1,000/Tape & Reel

NOTES:

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-1263-3

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.