TB3008

PLL Jitter and its Effects on ECAN™ Technology Communications

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INTRODUCTION

Phase Locked Loop (PLL) circuits are increasingly used in microcontrollers to achieve higher internal clock frequencies. Incorporation of PLL circuits allows better performance while reducing overall noise. Microchip's dsPIC33F Digital Signal Controllers and PIC24H 16-bit microcontrollers feature programmable PLLs in their clock generation circuits.

One point of interest in the use of PLL circuits is that they create a small, but still measurable, level of transient phase shifts, or *jitter*. This technical brief shows the influence of PLL jitter on CAN communications using the dsPIC33F/PIC24H ECAN module, and explains how the combined effects of jitter and crystal drift are well below the CAN 2.0 specification.

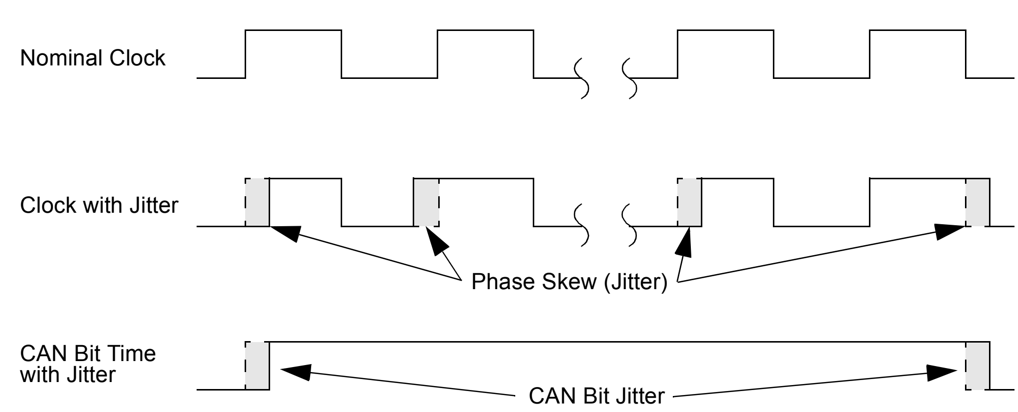
EXTERNAL CRYSTALS, SYSTEM CLOCK AND MEASURABLE JITTER

The clock frequency generated from a PLL circuit is subject to jitter, also defined as Phase Jitter or Phase Skew. This jitter is random in nature, and hence the total error caused by this jitter tends to cancel itself over time. For the dsPIC33F and PIC24H device families, Microchip specifies Clock Jitter (D_{CLK}) as being in the range of -3% to +3%.

Therefore, Total Jitter is (2 * D_{CLK}) = 6%.

The CAN protocol uses a bit stuffing technique that inserts a bit of a given polarity, following five bits with the opposite polarity. This gives a worst-case total of 10 bits transmitted without resynchronization (compensation for jitter or phase error). However, often the Total Jitter per Bit is the parameter of interest. For a single bit, it is necessary to consider only two jitter intervals to correct for jitter induced error: one interval in the beginning of the bit period, and another at the end. The overall effect is shown in Figure 1.

FIGURE 1: EFFECTS OF PHASE JITTER ON THE SYSTEM CLOCK AND CAN BIT TIME



For a single bit, it is possible to show that the relation between the jitter and the total frequency error can be defined as:

EQUATION 1:

$$\Delta f = \frac{\textit{Total Jitter}}{\text{NBT}} = \frac{2 \times D_{CLK}}{\text{NBT}}$$

where jitter is expressed in terms of time, and NBT is the Nominal Bit Time.

For example, assume a CAN bit rate of 33.33 kbps, which gives an NBT of 30 μs. For a 32 MHz clock generated from the PLL, the jitter at this clock frequency is:

EQUATION 2:

$$3\% \times \frac{1}{32\ \text{MHz}} = \frac{0.03}{32 \times 10^6} = 0.9388\ \text{ns}$$

The resultant frequency error is:

EQUATION 3:

$$\frac{2 \times (0.9388 \times 10^{-9})}{30 \times 10^{-6}} = 6.3438 \times 10^{-5} = 0.006\%$$

This is clearly smaller than the expected drift of a crystal oscillator, typically specified at 100 ppm or 0.01%. If we add jitter to oscillator drift, we have a total frequency drift of 0.016%.

Consider another example: assume a CAN bit rate of 83.33 kbps, which gives an NBT of 12 µs. For a 32 MHz clock generated from the PLL, the jitter at this clock frequency is 0.09388 ns as calculated above. The resultant frequency error is:

EQUATION 4:

$$\frac{2 \times (0.9388 \times 10^{-9})}{12 \times 10^{-6}} = 15.6467 \times 10^{-5} = 0.016\%$$

If we add jitter to oscillator drift, we have a total frequency drift of 0.026%.

Table 1 shows the relation between the clock generated by the PLL and the frequency error from jitter as a percentage of the nominal clock frequency. The frequency error is directly proportional to the CAN bit rate, and will therefore be even smaller if the CAN bit rate is lower than those listed in Table 1. As expected, the frequency error is inversely proportional to the system clock frequency, which is equivalent to the PLL output if the PLL is enabled.

The total oscillator frequency errors for common clock frequencies and bit rates, including both oscillator drift and jitter per bit, are shown in Table 2.

CONCLUSION

For Microchip's dsPIC33F and PIC24H device families, the sum of the errors introduced by the crystal drift and the errors introduced by the PLL jitter on a per-bit basis is well below the maximum jitter specified by the CAN 2.0 bus specification over a wide range of device clock speeds and CAN bit rates. This makes the usage of the internal PLL in the above device families well-suited for high-speed CAN bus-based communications.

TABLE 1: FREQUENCY ERROR FROM JITTER AT VARIOUS PLL GENERATED CLOCK SPEEDS

PLL Output	Resultant Device Operating Speed	P_{jitter}	T_{jitter}	Frequency Error at Various Nominal Bit Times (Bit Rates)					
				30 µs (33.33 Kb/s)	12 µs (83.33 Kb/s)	8 µs (125 Kb/s)	4 µs (250 Kb/s)	2 µs (500 Kb/s)	1 µs (1 Mb/s)
80 MHz	40 MIPS	0.375 ns	0.75 ns	0.003%	0.006%	0.009%	0.019%	0.038%	0.075%
40 MHz	20 MIPS	0.75 ns	1.5 ns	0.005%	0.013%	0.019%	0.038%	0.075%	0.150%
32 MHz	16 MIPS	0.9388 ns	1.88 ns	0.006%	0.016%	0.023%	0.047%	0.094%	0.190%

TABLE 2: TOTAL FREQUENCY ERROR AT VARIOUS PLL GENERATED CLOCK SPEEDS (100 ppm OSCILLATOR DRIFT INCLUDING ERROR FROM JITTER)

PLL Output	Resultant Device Operating Speed	Frequency Error at Various Nominal Bit Times (Bit Rates)					
		30 µs (33.33 Kb/s)	12 µs (83.33 Kb/s)	8 µs (125 Kb/s)	4 µs (250 Kb/s)	2 µs (500 Kb/s)	1 µs (1 Mb/s)
80 MHz	40 MIPS	0.013%	0.016%	0.019%	0.029%	0.048%	0.085%
40 MHz	20 MIPS	0.015%	0.023%	0.029%	0.048%	0.085%	0.160%
32 MHz	16 MIPS	0.016%	0.026%	0.033%	0.057%	0.104%	0.200%

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