

PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F15324/44 family devices that you have received conform functionally to the current Device Data Sheet (DS40001889C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F15324/44 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on [page 6](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15324/44 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A1	A3
PIC16F15324	30C2h	2001h	2003h
PIC16LF15324	30C3h	2001h	2003h
PIC16F15344	30C4h	2001h	2003h
PIC16LF15344	30C5h	2001h	2003h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC16(L)F153XX Memory Programming Specification" (DS40001838) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A1	A3
Electrical Specifications	SMBus 2.0	1.1	The maximum V _{IL} level changes when V _{DD} is below 4.0V at 125°C.	X	
	Fixed Voltage Reference (FVR) Accuracy	1.2	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X
	Minimum V _{DD} Specification for LF Devices	1.3	V _{DDMIN} specifications are changed for LF devices only.	X	X
	ADC Offset Error	1.4	ADC Offset Error specification changed.	X'	X
Host Synchronous Serial Port (MSSP)	SPI Client Mode	2.1	The SSPBUF transmit shift register may be corrupted under certain conditions.	X	
Nonvolatile Memory (NVM)	WRERR Bit Operation	3.1	When performing an NVM high-voltage operation, if a Reset is issued in the middle of the operation, the WRERR bit is set. Then, if the user clears the WRERR bit and a Reset occurs again, this sets the WRERR bit because the internal latch has not been cleared earlier.	X	
Windowed Watchdog Timer (WWDT)	Window Operation in DOZE Mode	4.1	Window feature of the WWDT does not operate correctly in DOZE mode.	X	
Timer0	Timer0 Clock Source	5.1	Operation of Timer0 is incorrect when Fosc/4 is used as the clock source.	X	
Reference Clock Output Module (CLKR)	CLKR Output	6.1	First output pulse of reference clock output module is incorrect when CLKREN is enabled.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Electrical Specifications

1.1 SMBus 2.0 V_{IL} Level

At 125°C when the V_{DD} voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the V_{IL} parameter is 0.8V. When V_{DD} drops below 4.0V, the maximum SMBus voltage level for V_{IL} drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A3						
X	X						

1.3 Minimum V_{DD} Specifications for LF Devices

V_{DDMIN} parameter (D0002) at -40°C to +25°C = 2.3V. (See [TABLE 37-1: Supply Voltage](#) on page 5 for reference.)

Work around

None.

1.4 ADC Offset Error

The table containing the Offset Error specification (AD04:EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error is +/-3.0 LSB.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

2. Module: Host Synchronous Serial Port (MSSP)

2.1 SSPBUF May Become Corrupted

When operating in SPI Client mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted client byte cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around

Method 1 (Interrupt Based Using $\overline{SS}$):

1. Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS} == 0$ when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
 - Add a delay that ensures the first SCK clock will be complete, or
 - Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Once either of these is complete, it is safe to return to program execution.

Method 2 (Bit Polling Based Using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
 2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.nSS == 0)).
 3. When $\overline{SS}$ is active ($\overline{SS} == 0$), do either of the following:
 - Add a delay that ensures the first SCK clock will be complete, or
 - Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.
- Once one of these two methods is complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ Not Available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A1	A3						
X							

3. Module: Nonvolatile Memory (NVM)

3.1 WRERR Bit Operation

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit of the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset occurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

4. Module: Windowed Watchdog Timer (WWDT)

4.1 Window Feature of the WWDT Does Not Operate Correctly in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

1. Use the Windowed mode of operation in any other mode than DOZE. If disabling the DOZE mode is not an option, use the WWDT module without the window being enabled.
2. If the device is in DOZE mode, perform the arming process for the window in NORMAL mode, and return to the DOZE mode.
3. If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A1	A3						
X							

5. Module: Timer0

5.1 Operation of Timer0 Is Incorrect When Fosc/4 Is Used as the Clock Source

Clearing the T0ASYNC bit in the T0CON1 register when Timer0 is configured to use Fosc/4 may cause incorrect behavior. This issue is only valid when Fosc/4 is used as the clock source.

Work around

Set the T0ASYNC bit in the T0CON1 register when using Fosc/4 as the Timer0 clock.

Affected Silicon Revisions

A1	A3						
X							

6. Module: Reference Clock Output Module (CLKR)

6.1 First Output Pulse of Reference Clock Output Module Is Incorrect When CLKREN Is Enabled

If CLKREN bit is set by the user, the number of input clock cycles taken to generate the reference clock output might vary by one cycle due to a race condition. This condition occurs only if LCx_out or NCOx_out are the inputs (CLKRCLK bits) to the CLKR module.

Work around

Ignore the first output pulse of the CLKR output signal.

Affected Silicon Revisions

A1	A3						
X	X						

TABLE 37-1: SUPPLY VOLTAGE

PIC16LF15324/44			Standard Operating Conditions (Unless Otherwise Stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D002	VDD		1.8	—	3.6	V	FOSC ≤ 16 MHz, +25°C ≤ TA ≤ +125°C
			2.3	—	3.6	V	FOSC ≤ 16 MHz, -40°C ≤ TA ≤ +25°C
			2.5	—	3.6	V	FOSC > 16 MHz

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001889C):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

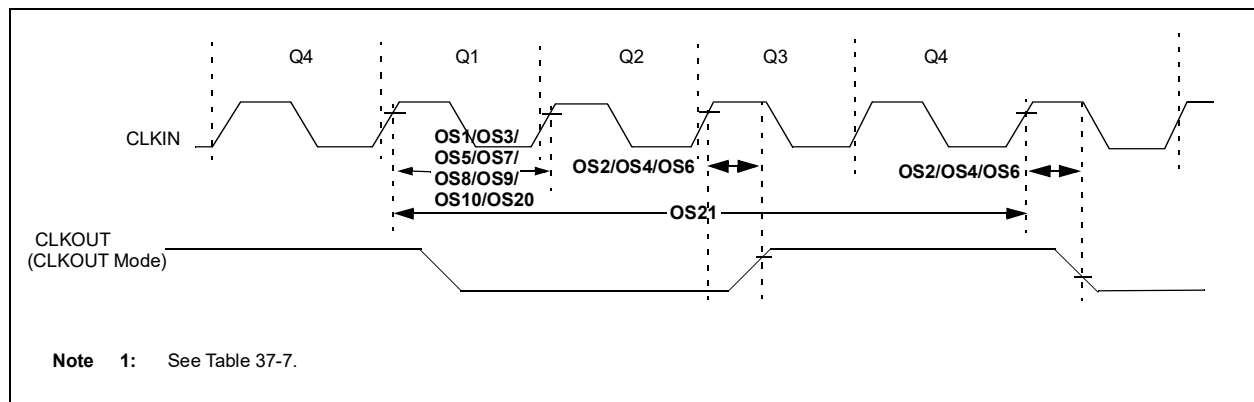
1. Module: Table 36.3 Instruction Set Literal Operations

LITERAL OPERATIONS									
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	0001	01kk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

2. Module: Electrical Specifications

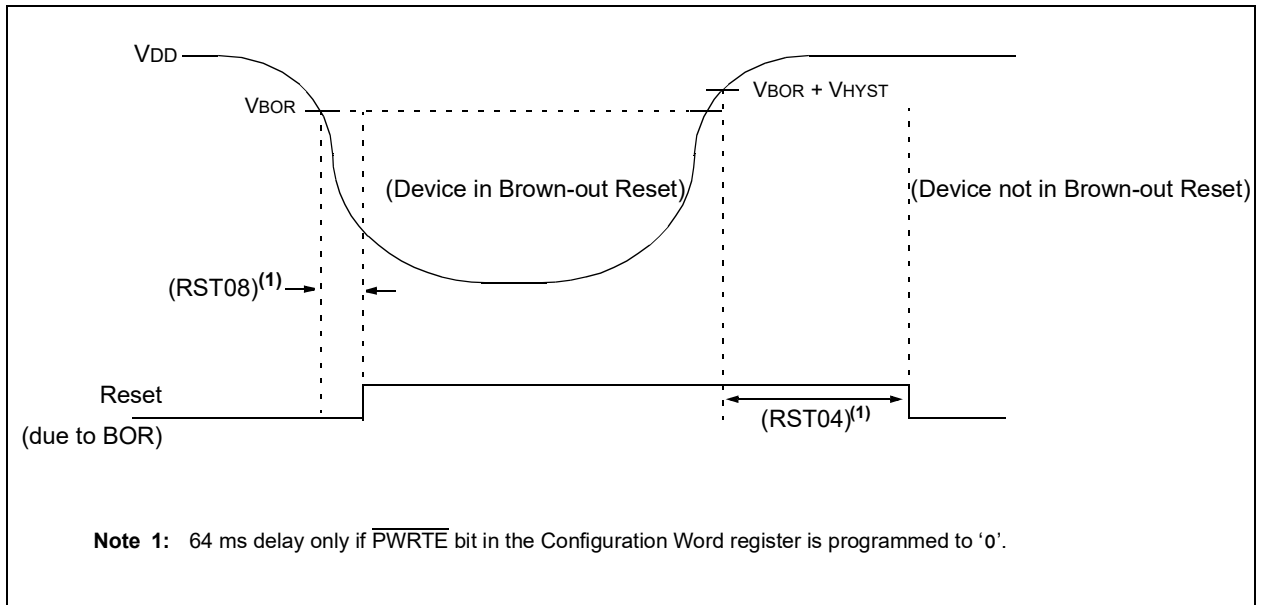
2.1 Figure 37-5: Clock Timing

Figure 37-5 incorrectly shows the location of parameters OS1, OS2, OS3, OS4, OS5, OS6, OS7, OS8, OS9, OS10, OS20 and OS21. The correct location for the above-mentioned parameters is depicted in the following figure.



2.2 Figure 37-9: Brown-Out Reset Timing and Characteristics

Note 1 in Figure 37-9 is incorrect. The correct note along with the figure is depicted below.



APPENDIX A: DOCUMENT REVISION HISTORY

Rev D Document (03/2021)

Updated Table 2 and 37-1 and Section 1.3 Minimum VDD Specifications. Other minor corrections.

Data Sheet Clarifications:

Added Module 2: Electrical Specifications.

Rev C Document (11/2020)

Added section 1.4; Updated Table 2 and added Table 37-1; Other minor corrections.

Rev B Document (07/2019)

Updated Table 1, Table 2 and section 1. Added new section 3, section 4 and section 5. Added section 6. Other minor corrections.

Data Sheet Clarifications:

Added Module 1: Table 36.3 Instruction Set

Rev A Document (03/2017)

Initial release of this document.