

General Description

The KS8995M/X features dual media independent interfaces (MIIs), which enable the system designer to use the chip in multiple applications. The switch MII allows the KS8995M/X to be connected directly to a CPU or to an external PHY device. The PHY-5 MII interface lets the system designer recover the use of the 5th PHY, saving BOM costs in small office/home office (SOHO) gateway solutions.

This application note describes the two different MIIs on the KS8995M/X and illustrates their different applications.

MII Interface

MII-SW Interface

The first MII on the KS8995M/X is the MII-SW interface. This MII connects directly to the internal switch. The MII-SW interface can be configured for either PHY-mode or MAC-mode. PHY-mode is used to connect the MII-SW interface to an external MAC. MAC-mode is used to connect the MII-SW interface to an external PHY. A typical application for the MII-SW interface in PHY mode is the integrated broadband router where the KS8995M/X is connected to a CPU, as shown in Figure 1.

The typical pin connections from the KS8995M/X to the CPU MII interface in PHY-mode are given in Figure 2. The addition of series termination resistors is recommended, as shown in Figure 2, near the MII signal sources for EMI purposes.

The MII-SW interface can also be configured for MAC-mode. This enables the system designer to connect an external PHY device to the KS8995M/X's internal switch, as shown in Figure 3.

The typical pin connections from the KS8995M/X to the external PHY MII interface in MAC-mode are given in Figure 4. The addition of series termination resistors is recommended, as shown in Figure 4, near the MII signal sources for EMI purposes.

MII-P5 Interface

The second MII interface on the KS8995M/X is the MII-P5. This MII interface connects to the 5th PHY unit in the KS8995M/X. In other devices, once the MII-SW interface is used, the 5th PHY unit functionality is lost. However, in the KS8995M/X, the MII-P5 interface allows the system designer to recover the functionality of the 5th PHY device and use it either as a WAN port or to connect it to another external MAC device. A typical example of this is the broadband gateway application, as shown in Figure 5. This added MII port feature can save BOM costs

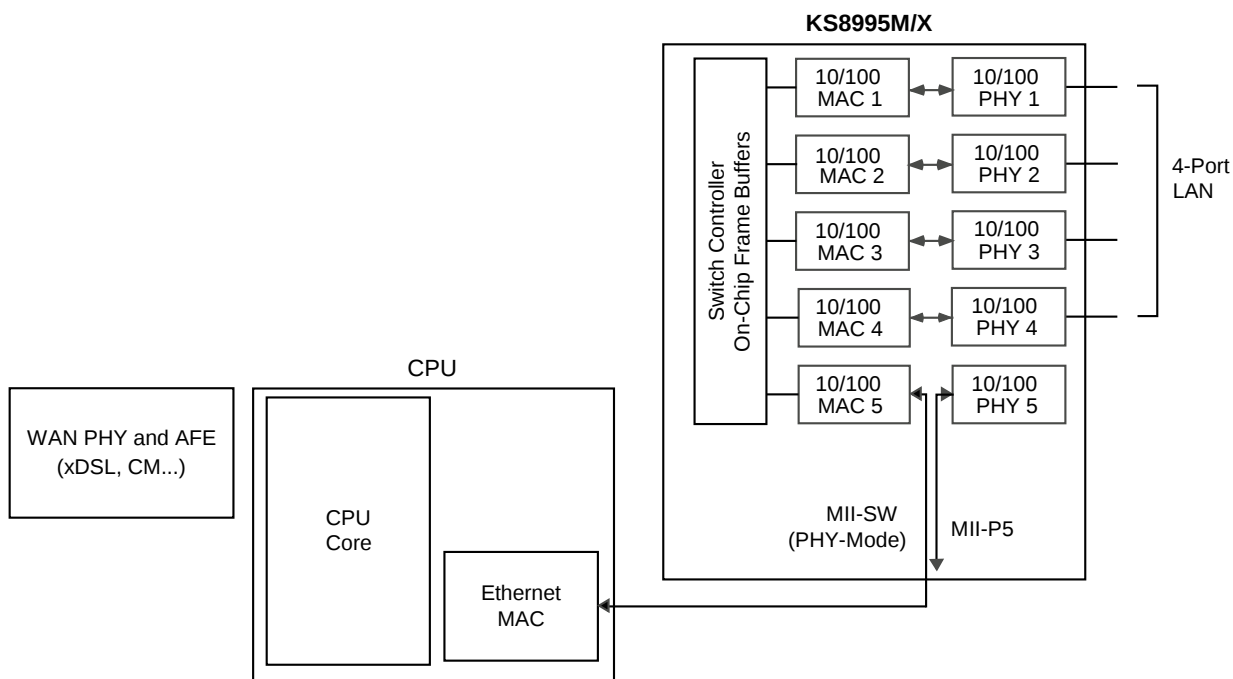


Figure 1. Integrated Broadband Router Application

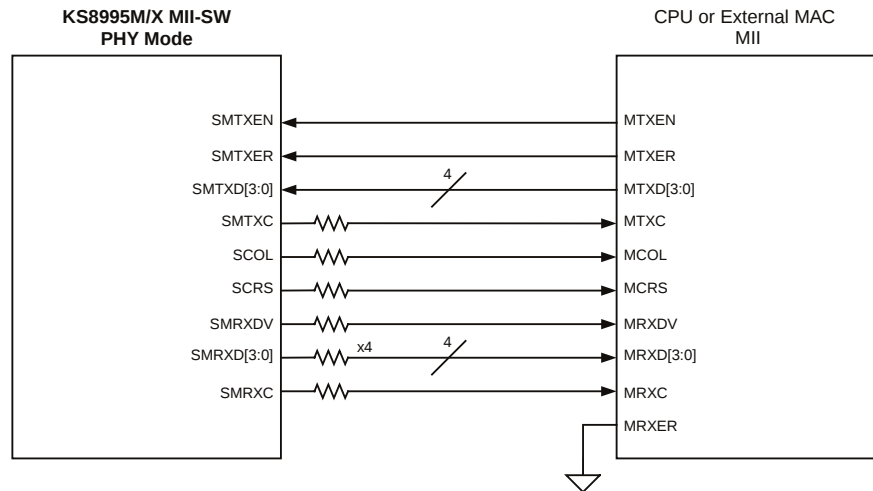


Figure 2. MII-SW PHY-Mode Connections

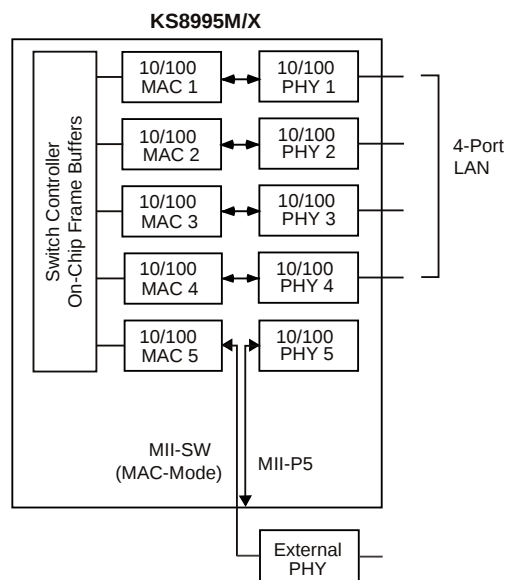


Figure 3. KS8995M/X with an External PHY

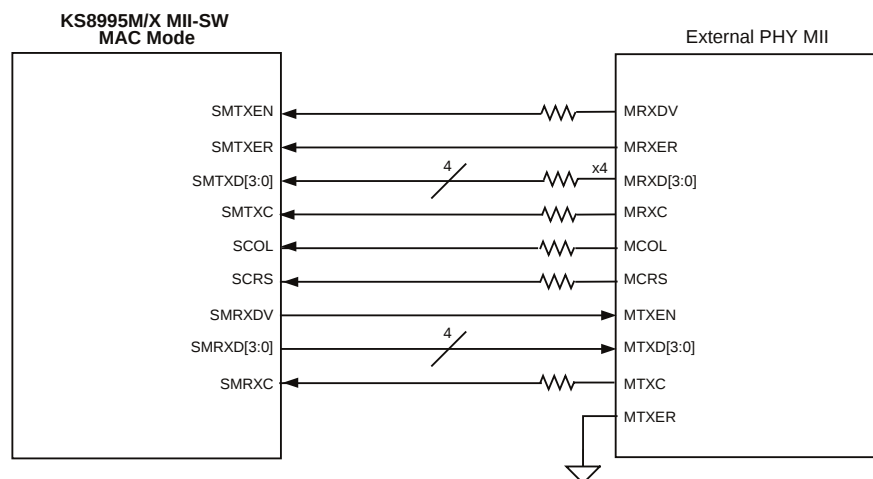


Figure 4. MII-SW MAC-Mode Connections

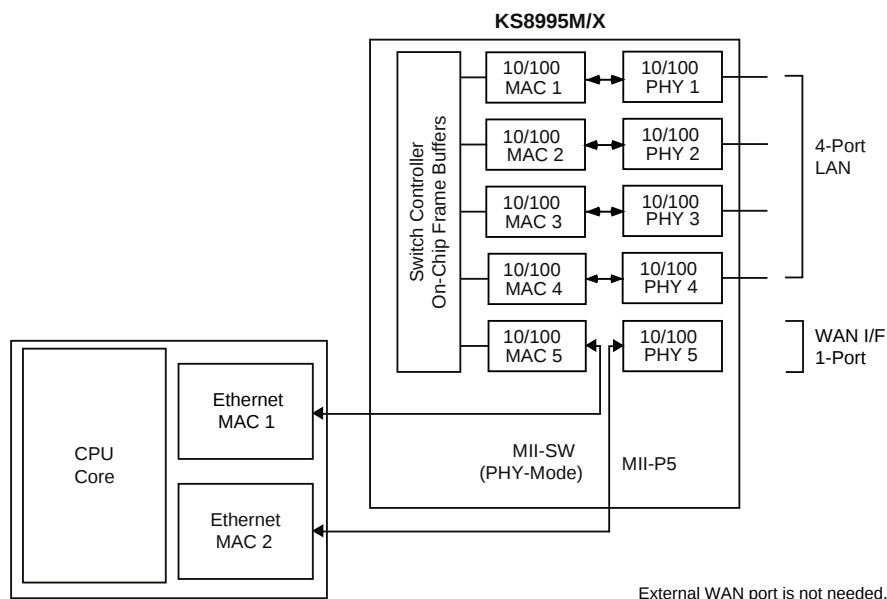


Figure 5. Broadband Gateway Application

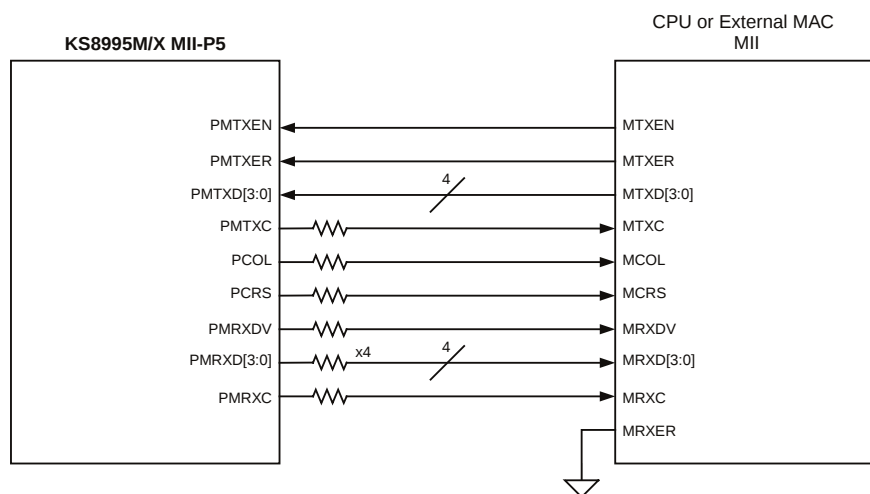


Figure 6. MII-P5 Connections

The typical pin connections from the KS8995M/X MII-P5 to an external MAC interface are shown in Figure 6. The addition of series termination resistors is recommended, as shown in Figure 6, near the MII signal sources for EMI purposes.

Conclusion

The dual MII feature of the KS8995M/X gives the system designer a decided advantage when implementing next generation SOHO solutions. The KS8995M/X has the flexibility to be used in integrated broadband router applications, with different external PHYs such as HomePNA⁽¹⁾ or wireless LAN, and in broadband gateway applications.

In the broadband gateway application, the KS8995M/X's 5th PHY unit can be recovered for use as a WAN port saving BOM costs. In addition, the broadband gateway configuration shown in Figure 5 provides for a physical LAN and WAN separation, which adds additional security for local traffic.

For additional support, contact your local Micrel Field Application Engineer or salesperson.

Note:

1. HomePNA: Home Phoneline Networking Alliance.

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