AN 17.9

Migrating from the LAN9217 to the LAN9211

1 Objective

The purpose of this application note is to assist SMSC customers with existing LAN9217 designs when upgrading to the new LAN9211 device. This upgrade is straightforward, but does require a PCB change to support a different package. This application note addresses all the differences between the LAN9217 and the LAN9211 devices, making this transition as easy as possible.

1.1 References

- LAN9211 Datasheet
- One-Page Reference Design for the LAN9211
- One-Page Reference Design for the LAN9217

1.2 Overview of Changes Required

Table 1.1 summarizes the changes needed to migrate from the LAN9217 to the LAN9211.

Table 1.1 Summary of Changes Required

CHANGE REQUIRED	COMMENTS	REFERENCES
New PCB	Needed to support device package 56-pin QFN with exposed VSS Pad	This application note and 1-Page Reference Design are available at www.smsc.com.
Firmware Upgrade	Needed to take advantage of faster Host Bus timing and mixed endian support	This application note and LAN9211 Datasheet are available at www.smsc.com.
Upgrade drivers	Recognize new device ID and utilize new Checksum Offload Engine	Refer to Table 5.1

2 Hardware Changes

2.1 Component Changes

2.1.1 Device Package

The LAN9211 is packaged in a 56-pin QFN with an exposed VSS pad. Therefore, the LAN9211 is not a drop in replacement for the LAN9217 and will require a new PCB. The recommended PCB land pattern can be found in Chapter 8 of the LAN9211 Datasheet. It is recommended to place a 4x4 grid of vias at 60mil spacing in the exposed pad area for connection to the board's ground plane, as shown in Figure 2.1 below. Please consult with your Assembly House for their process capabilities and recommendations.

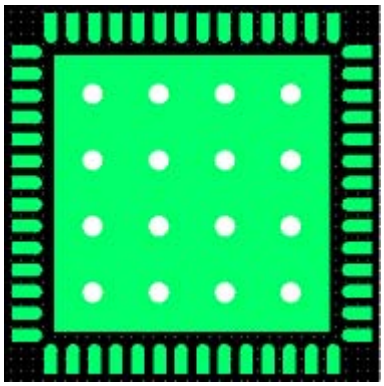

Figure 2.1 PCB Land Pattern

2.2 Pin Changes

2.2.1 Pin Cross-Reference

Table 2.1 below cross-references signal/pin changes between the LAN9217 and the LAN9211.

Table 2.1 Pin Cross-Reference

LAN9217		LAN9211	
SIGNAL	**PIN**	**SIGNAL**	**PIN**
D[15:0]	43-46, 49-53, 56-59, 62-64	D[15:0]	19-23, 25-29, 31-36
A[7:1]	12-18	A[7:1]	6-12
nRD	92	nRD	15
nWR	93	nWR	16
nCS	94	nCS	17
IRQ	72	IRQ	43
Reserved	71, 84, 90, 91	Reserved	14
AMDIX_EN	73	AMDIX_EN	52

Table 2.1 Pin Cross-Reference (continued)

LAN9217		LAN9211	
SIGNAL	**PIN**	**SIGNAL**	**PIN**
SPEED_SEL	74		
FIFO_SEL	76	FIFO_SEL	13
TPO+	79	TPO+	45
TPO-	78	TPO-	44
TPI+	83	TPI+	48
TPI-	82	TPI-	47
EXRES1	87	EXRES1	50
EEDIO	67	EEDIO	38
EECS	68	EECS	39
EECLK	69	EECLK	40
XTAL1	6	XTAL1	55
XTAL2	5	XTAL2	54
nRESET	95	nRESET	42
PME	70	PME	41
GPIO[2:0]	100, 99, 98	GPIO[2:0]	5, 4, 3
RBIAS	10		
ATEST	9		
VREG	2		
VDD_IO	20, 28, 35, 42, 48, 55, 61, 97	VDD_IO	1, 18, 24, 30, 56
GND_IO	19, 27, 34, 41, 47, 54, 60, 96		
VDD_A	81, 85, 89	VDD_A33	46, 49,51
VSS_A	77, 80, 86, 88		
VDD_CORE	3, 65	VDD_CORE	2, 37
GND_CORE	1, 66		
VDD_PLL	7		
VSS_PLL	4		
VDD_REF	8		
VSS_REF	11		
		VDD_A18	53
		VSS	Exposed Pad
TX_CLK	40		
TXD[3:0]	36-39		
TX_EN	21		
RX_CLK	26		
RX_ER	25		

Table 2.1 Pin Cross-Reference (continued)

LAN9217		LAN9211	
SIGNAL	**PIN**	**SIGNAL**	**PIN**
COL	33		
RXD[3:0]	24, 23, 22, 75		
CRS	32		
RX_DV	29		
MDIO	30		
MDC	31		

2.2.2 Signal Pins not Available on the LAN9211

The following signal pins are not available on the LAN9211:

- SPEED_SEL
- RBIAS
- ATEST
- TX_CLK, TXD[3:0], TX_EN
- RX_CLK, RX_ER, RXD[3:0], RX_DV
- COL, CRS
- MDIO, MDC

2.2.3 Power and Ground Pin Changes

The LAN9217 has several different ground pins (GND_IO, VSS_A, GND_CORE, VSS_PLL and VSS_REF). However, the LAN9211 uses a single ground connection (VSS) on the exposed pad. Also, the LAN9211 does not have VDD_PLL, VDD_REF and VREG power pins.

The LAN9211 has a VDD_A18 (pin 53) that must be externally connected to VDD_CORE (pins 2, 37) with traces at least 10 mil wide and connected to a 10uF low ESR ceramic capacitor. Each of these 3 pins must be individually decoupled with a 0.01uF capacitor as close as possible to the pin, as shown in Figure 2.2, "Power Connections".

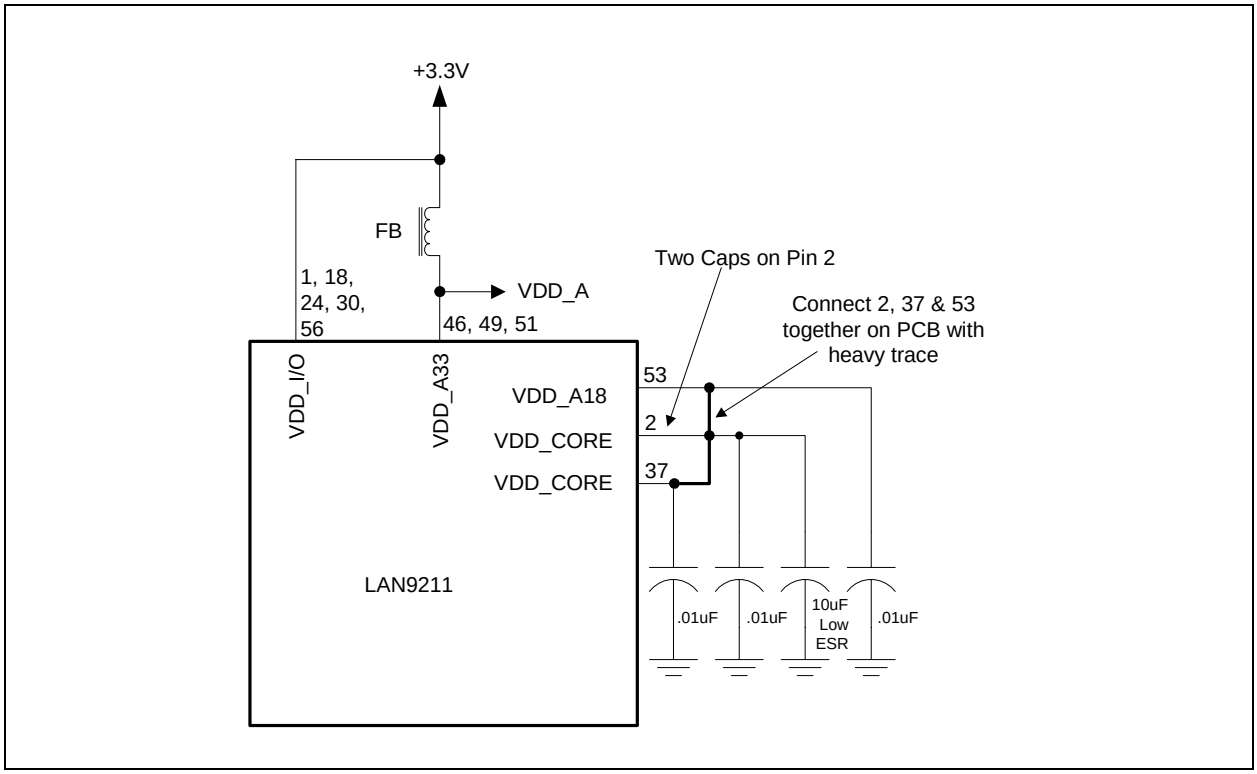

Figure 2.2 Power Connections

2.2.4 AMDIX_EN (Pin 52)

On the LAN9217, the AMDIX_EN pin (Pin73) has an internal pull-down and can be left unconnected to disable Auto-MDIX. However, on the LAN9211 this pin has an internal pull-up and must be pulled low to disable Auto-MDIX. This pin can be pulled high or left unconnected to enable Auto-MDIX.

2.2.5 EMC Considerations

For LAN9211 designs that must operate in an EMI constrained environment, the designer should include four low valued capacitors (less than 15pF) on the TPO+, TPO-, TPI+ & TPI- pins and terminate them to digital ground. These capacitors should be placed as close as possible to the magnetics. These capacitors can then be populated as required for EMI compliance. The 49.9 ohm termination resistors on the TPO/TPI signal lines should be placed as close as possible to the LAN9211. Additionally, the use of a discrete magnetic and RJ-45 connector is highly recommended, as the integrated magnetics are known to cause EMI compliance issues.

3 Register Changes

3.1 SCSR Register Changes

3.1.1 ID_REV Register (offset: 50h)

- Bit 31:16 changed to 9211h

3.1.2 HW_CFG Register (offset: 74h)

- Bits 6:2 become reserved
- Bit 28 becomes FSELEND, Direct FIFO Access Endian Ordering**.** This control bit determines the endianess of RX and TX data FIFO host accesses when accessed using the FIFO_SEL signal. When this bit is cleared, FIFO_SEL accesses utilize little endian byte ordering. When this bit is set, FIFO_SEL accesses utilize big endian byte ordering. Please refer to Section 3.8 of the LAN9211 Datasheet for more information on this feature.
- Bit 29 becomes FPORTEND, FIFO Port Endian Ordering. This control bit determines the endianess of RX and TX data FIFO host accesses when accessed through the RX/TX Data FIFO ports, including the alias addresses (any access from 00h to 3Ch). When this bit is cleared, data FIFO port accesses utilize little endian byte ordering. When this bit is set, data FIFO port accesses utilize big endian byte ordering. Please refer to Section 3.8 of the LAN9211 Datasheet for more information on this feature.

3.2 MAC Register Changes

3.2.1 COE_CR Register (offset: Dh)

The Checksum Offload Engine Control Register (COE_CR), has been added to the LAN9211 at offset Dh. This register controls the transmit and receive checksum offload engines. Please refer to Section 3.6 of the LAN9211 Datasheet for more information on this feature.

- Bits 31:17 - Reserved
- Bit 16 - TX Checksum Offload Engine Enable (TXCOE_EN). TXCOE_EN may only be changed if the TX data path is disabled. If cleared, the TXCOE is bypassed. If set, the TXCOE is enabled.

  Bits 15:2 - Reserved
- Bit 1 - RX Checksum Offload Engine Mode (RXCOE_MODE). This bit indicates whether the RXCOE will check for VLAN tags or a SNAP header prior to beginning its checksum calculation. In its default mode, the calculation will always begin 14 bytes into the frame. RXCOE_MODE may only be changed if the RX data path is disabled. If set, begin checksum calculation after first 14 bytes of Ethernet Frame. If cleared, begin checksum calculation at start of L3 packet by adjusting for VLAN tags and/or SNAP header.
- Bit 0 - RX Checksum Offload Engine Enable (RXCOE_EN). RXCOE_EN may only be changed if the RX data path is disabled. If cleared, the RXCOE is bypassed. If set, the RXCOE is enabled.

4 Additional Features

4.1 Mixed Endian Support

In addition to the Word Swap function supported by both the LAN9217 and the LAN9211, the LAN9211 also provides support for mixed endian data FIFO accesses. The LAN9211 provides the ability to select data FIFO endianess separately for accesses through the data FIFO ports (addresses 00h-3Ch) or using the FIFO_SEL input signal. This is accomplished via the FPORTEND and FSELEND bits of the

HW_CFG—Hardware Configuration Register, respectively. Please refer to Section 3.8 of the LAN9211 Datasheet for more information.

Note: CSR and status FIFO accesses are not affected by the FPORTEND and FSELEND endianess select bits.

4.2 Checksum Offload Engine (COE)

The LAN9211 contains two checksum offload engines, which offload the calculation of the 16-bit checksum for transmitted and received Ethernet frames. Please refer to Section 3.6 of the LAN9211 Datasheet for detailed information on the use of the COE's. Please note that currently only the Linux driver supports checksum offloading.

4.2.1 Receive Checksum Offload Engine (RXCOE)

The receive checksum offload engine provides assistance to the CPU by calculating a 16-bit checksum for a received Ethernet frame. The RXCOE readily supports the following IEEE 802.3 frame formats:

- Type II Ethernet frames
- SNAP encapsulated frames
- Support for up to 2, 802.1q VLAN tags

4.2.2 Transmit Checksum Offload Engine (TXCOE)

The transmit checksum offload engine provides assistance to the CPU by calculating a 16-bit checksum, typically for TCP, for a transmit Ethernet frame. The TXCOE calculates the checksum and inserts the results back into the data stream as it is transferred to the MAC.

5 Driver Support

Table 5.1 below shows the version of drivers needed to support the LAN9211.

Table 5.1 Driver Support

DRIVER	REVISION
WinCE 5.0 - XScale (PXA270)	1.10 or later
Linux - XScale (PXA270)	1.52 or later

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123