UG0641
User Guide
Alpha Blending

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 5.0

All the sections were updated in revision 5.0 of this document.

1.2 Revision 4.0

In revision 4.0 of this document, the Resource Utilization section and the Resource Utilization Report table were updated. For more information, see Resource Utilization, page 4.

1.3 Revision 3.0

In revision 3.0 of this document, the Testbench section was updated with the Steps to simulate the core using test bench.

1.4 Revision 2.0

In revision 2.0 of this document, the SAR 76066 was updated.

1.5 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Alpha Blending

Alpha blending is the process of combining an image with a background to create the appearance of partial or full transparency. It is used to render multiple images into a single background image in separate passes and make one final image.

For example, an 8-bit alpha input can represent 256 levels of transparency with a value of 0 denoting that the image is completely transparent and a value of 255 denoting that the image is completely opaque. Alpha blending defines the transparency of individual images when blended with the background image.

The following are the equation for pixel-wise alpha blending:

$$R_{out} = R_{in1} \times (1 - \alpha_{in}) + R_{in2} \times \alpha_{in}$$

$$G_{out} = G_{in1} \times (1 - \alpha_{in}) + G_{in2} \times \alpha_{in}$$

$$B_{out} = B_{in1} \times (1 - \alpha_{in}) + B_{in2} \times \alpha_{in}$$

Where,

R_{in1}, G_{in1}, and B_{in1} represent the red, blue, and green values of image1

R_{in2}, G_{in2}, and B_{in2} represent the red, blue, and green values of image2

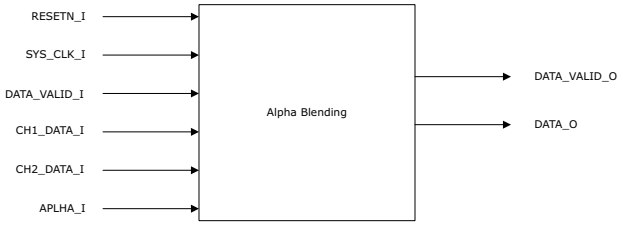
R_{out}, G_{out}, and B_{out} represent the red, blue, and green values of the output image

α_{in} is the input alpha value

2.1 Hardware Implementation

The following figure shows the hardware implementation of alpha blending.

Figure 1 • **Block Diagram of Alpha Blending IP**



When the DATA_VALID_I signal goes high, the R, G, and B values of the output is computed according to the preceding equation.

DATA_O is valid when DATA_VALID_O (which is equivalent to DATA_VALID_I with two clock cycle delay) goes high.

2.2 Inputs and Outputs

The following table lists the description of input and output ports.

Table 1 • **Inputs and Outputs of Alpha Blending IP**

Signal Name	Direction	Width	Description
RESETN_I	Input	1-bit	The active-low asynchronous reset signal to design
SYS_CLK_I	Input	1-bit	System clock
DATA_VALID_I	Input	1-bit	Input data valid

Table 1 • **Inputs and Outputs of Alpha Blending IP *(continued)***

Signal Name	Direction	Width	Description
CH1_DATA_I	Input	3 × G_PIXEL_WIDTH	Channel1 input data CH1_DATA_I [3 × g_PIXEL_WIDTH-1] to CH1_DATA_I [2 × g_PIXEL_WIDTH] represents R value of input1 CH1_DATA_I [2 × g_PIXEL_WIDTH-1] to CH1_DATA_I [g_PIXEL_WIDTH] represents G value of input1 CH1_DATA_I [g_PIXEL_WIDTH-1] to CH1_DATA_I [0] represents B value of input1
CH2_DATA_I	Input	3 × G_PIXEL_WIDTH	Channel2 input data CH2_DATA_I [3 × g_PIXEL_WIDTH-1] to CH2_DATA_I [2 × g_PIXEL_WIDTH] represents R value of input2 CH2_DATA_I [2 × g_PIXEL_WIDTH-1] to CH2_DATA_I [g_PIXEL_WIDTH] represents G value of input2 CH2_DATA_I [g_PIXEL_WIDTH-1] to CH2_DATA_I [0] represents B value of input2
ALPHA_I	Input	8-bit	Alpha input
DATA_VALID_O	Output	1-bit	Asserted when output data is valid
DATA_O	Output	3 × G_PIXEL_WIDTH	Output data DATA_O [3 × g_PIXEL_WIDTH-1] to DATA_O [2 × g_PIXEL_WIDTH] represents R output DATA_O [2 × g_PIXEL_WIDTH-1] to DATA_O [g_PIXEL_WIDTH] represents G output DATA_O [g_PIXEL_WIDTH-1] to DATA_O [0] represents B output

2.3 Configuration Parameters

The following table lists the description of the configuration parameters used in the hardware implementation of the Alpha Blending IP. They are the generic parameters and can vary based on the application requirements.

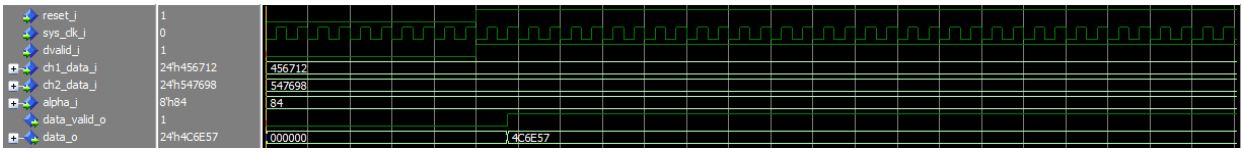
Table 2 • **Configuration Parameters**

Name	Description
G_PIXEL_WIDTH	Bit width of each pixel

2.4 Timing Diagrams

The following figure shows the timing diagram of alpha blending IP.

Figure 2 • **Timing Diagram of Alpha Blending IP**



2.5 Resource Utilization

The alpha blending IP is implemented on SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device (M2S150T-1152 FC package) and PolarFire® FPGA (MPF300TS -1FCG1152E package).

Table 3 • **Resource Utilization of PolarFire[1]**

Resource	Usage
DFFs	242
4-Input LUTs	273
MACC	6
RAM1Kx18	0
RAM64x18	0

1. When G_PIXEL_WIDTH = 8

Table 4 • **Resource Utilization of SmartFusion2[1]**

Resource	Usage
DFFs	242
4-Input LUTs	273
MACC	6
RAM1Kx18	0
RAM64x18	0

1. When G_PIXEL_WIDTH = 8