MicroNote 070

1 Thermal Management for Discrete Semiconductors

By Kent Walters

Thermal management of discrete semiconductors is vital if they are to operate within their ratings and obtain the desired performance. If device temperatures are not well controlled, excessive heat can result in poor semiconductor operating features including high leakage current, longer reverse recovery times for rectifiers, degraded gain in transistors, poor voltage regulation for Zeners, mechanical stresses, shorter life expectancy, or thermal runaway. Acceleration of time-to-failure is based on thermal activation energies and the Arrhenius equation for semiconductor failure mechanisms. The acceleration factor (A_T) from changes in temperature can be described as: $A_T = \exp[(E_{aa}/k)(1/T_1 - 1/T_2)]$, where E_{aa} is the apparent activation energy (eV), k is Boltzmann's constant (8.62×10^{-5} eV/K), T_1 is the absolute temperature of test 1 (K), and T_2 is the absolute temperature of test 2 (K). This can be further reviewed in JEDEC publication JEP122H.

1.1 Junction Temperature

The most important temperature for semiconductor devices is the p-n junction temperature (T_J) inside the package. It is also the source of heat with applied power and energy over time. The T_J becomes excessive if applied power exceeds specified ratings, inadequate heat sinking exists, ambient temperatures are poorly controlled, or any combination of these for overall thermal management. Regardless of specific origins, the same performance degradation or damage to the semiconductor device may occur over time. We shall review many of the design features, mounting considerations, and test methods that are needed for thermal management and optimum semiconductor performance.

1.2 Thermal Resistance

The primary method used in characterizing heat flow from a semiconductor device is with thermal resistance in units of °C/W. The device p-n junction temperature is calculated as:

Equation 1:

$T_J = P \times R_{\theta JA} + T_A$

where P is the applied power in Watts, $R_{\theta JA}$ is the thermal resistance junction to ambient in °C/Watt, and T_A is the ambient temperature in °C. With that description, the thermal resistance path to ambient is very important to understand.

One of the challenges in thermal management is $R_{\theta JA}$ is not typically specified by component manufacturers since it is influenced by mounting methods separate from the device.

This may include printed circuit boards (PCBs) with different copper pad sizes and thickness including various substrate materials or other mounting methods depending on package designs and power requirements. A commonly used PCB substrate material is FR4 with glass-reinforced epoxy laminate material, where "FR" stands for flame retardant.

Industry definitions for $R_{\theta JA}$ from JEDEC (JESD88F) describe it as 'The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a natural convection [still air] environment surrounding the device.' This definition does not include any mounting methods to conduct heat out of the device where heat dissipation is only by radiation or natural convection in still air. For other mounting environments, JEDEC also defines the term $R_{\theta JX}$ for 'The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a defined nonstandard environment surrounding the device.' This term is more applicable for many possible variations in mounting methods to better conduct heat out of the device. It would also require further specific mounting information to quantify in units of °C/W with reference to the surrounding ambient temperature.

Semiconductor component manufacturers do specify the maximum thermal resistance from junction to an external reference point ($R_{\theta JR}$) on various device package configurations. That value is significantly less than $R_{\theta JA}$ where there is no mounting to conduct heat out of the device. This can also be shown as:

Equation 2:
$R_{\theta JA} = R_{\theta JR} + R_{\theta RA}$
where $R_{\theta RA}$ is the thermal resistance from the device reference point to ambient. See $R_{\theta JR}$ examples below after Equation 4 on various package examples.

For representing variations in mounting methods with $R_{\theta JX}$ above, this can be shown as:

Equation 3:
$R_{\theta JX} = R_{\theta JR} + R_{\theta RX}$
where $R_{\theta RX}$ is the thermal resistance from the device reference point to ambient as influenced by specific mounting methods for better heat conduction out of the device. The value of $R_{\theta JX}$ is less than $R_{\theta JA}$ in Equation 2 and greater than $R_{\theta JR}$ as determined by the mounting and heat conduction efficiency out of the device. As a result, $R_{\theta JX}$ also becomes very important for design engineers in overall thermal management. Some of the performance specifications in MIL-PRF-19500 also now specify a maximum $R_{\theta JX}$ value for mounting or heat sinking to ensure the device power or forward current ratings (I_O) can be achieved without exceeding the maximum rated T_J. We will use $R_{\theta JX}$ with the JEDEC definition in Equation 3 rather than a specific maximum in military performance specifications. From Equations 1 and 2, we can then describe the following for T_J:

Equation 4:
$T_J = P \times (R_{\theta JX}) + T_A$.

The specified $R_{\theta JR}$ in Equations 2 and 3 will also have various acronyms depending on device design and applicable reference points on the package such as case, lead, end-cap, or solder pad with corresponding values of $R_{\theta JC}$, $R_{\theta JL}$, $R_{\theta JEC}$, or $R_{\theta JSP}$. In the example for $R_{\theta JL}$, it is also defined for a specific lead length from the body (typically 0.375 inch or 1 mm). These values of thermal resistance from the junction to an external reference point on the component has also been identified as R_{thJR} in JEDEC specifications. (JEDEC originally was for "Joint Electron Device Engineering Council" but is now known as the JEDEC Solid State Technology Association.) The corresponding temperatures at the external reference points (T_R) on the component also become important when measuring thermal resistance as defined in military or JEDEC specifications. These are in terms of the lead temperature (T_L), case temperature (T_C), end-cap temperature (T_{EC}), or solder point temperature (T_{SP}) for various discrete semiconductor packages where applicable.
It is also important to recognize that power (or current) derating curves in data sheets are most often shown only with respect to the defined reference point temperature on the package for semiconductor devices. The power derating curve versus the component reference temperature also often use the inverse slope of device thermal resistance ($R_{\theta JR}$) in Watts/°C. Power derates to zero at the maximum rated T_J. This is frequently 175°C for hermetic discrete silicon p-n junction diodes or lower values for Schottky rectifiers depending on barrier metal design to avoid thermal runaway when operated near their maximum reverse voltage ratings. Plastic packages that are sensitive to glass transition temperatures may dictate maximum operating temperature of 150°C. Integrated circuits are also often rated lower such as 70°C to 125°C with close-proximity spacing of many microelements in circuit design. By comparison, maximum junction ratings can be significantly higher for SiC materials including Schottkys.

1.3 Heating Power

In Equations 1 and 4, the power (P) across various diodes for dc operation and heating considerations can be expressed as follows:

Equation 5:
$P = V_Z \times I_Z$
as applicable for Zeners, or:

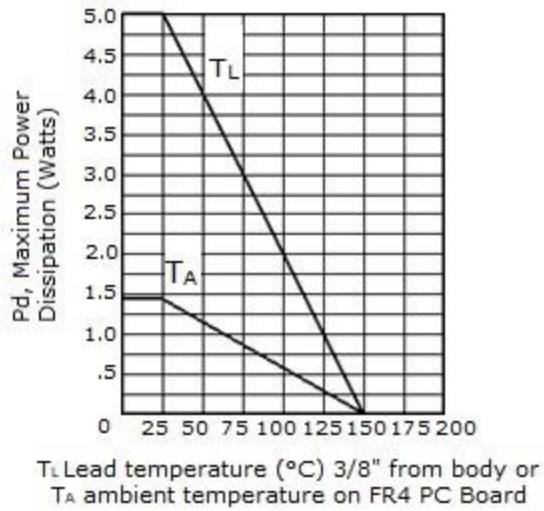
Equation 6:
$P = I_F \times V_F$
for rectifiers. In rectifier ac operation with half-sine-wave conducting and half-sine wave blocking, the RMS heating power is calculated as:

Equation 7:
$P = I_O(0.107 + 0.785\ V_{FM})$
where V_{FM} is the peak forward voltage during a half-sine wave operation and I_O is the rated average rectified output current as also identified in MIL-STD-750, TM3100, par 6.4.1b for ACOL burn-in.
In Equation 7, the peak forward current in each half-sine wave is 3.14 x I_O. This and many other considerations for rectifier waveforms are shown in JEDEC specification JESD282B.01 (section 6.6). Rectifiers are typically rated with I_O rather than power. Sometimes the power versus I_O is also graphically displayed in data sheets or military performance specs. Equations 6 and 7 do not include any heating power considerations in the reverse blocking state where leakage currents are often negligible. However, that cannot always be assumed particularly for silicon Schottky rectifiers that may have significant reverse leakage currents at higher reverse voltages and temperatures where they can also be vulnerable to thermal runaway. For dc operation on rectifiers, the forward current may approximate power in watts if the forward voltage (V_F) is very near one volt ($P = I_F \times V_F$). Silicon Schottky rectifiers will typically produce lower power with their lower V_F. For silicon carbide (SiC) Schottkys, the V_F is typically higher and reverse leakage currents lower by comparison to silicon for overall power considerations.

1.4 Ambient Temperature

As shown in Equations 1 and 4, the surrounding ambient temperature (T_A) is an important consideration in overall thermal management. The reference point temperature on the device will be higher in temperature with applied power as shown in Equation 3 with $R_{\theta RX}$.
The $R_{\theta JA}$ in Equation 1 is not often specified on a semiconductor device data sheet per JEDEC definitions. In examples where $R_{\theta JA}$ is specified, it needs to be carefully reviewed by the design engineer as to how it is defined compared to the actual mounting for the intended application as better recognized with $R_{\theta JX}$. As previously described in Equation 3, $R_{\theta JX}$ includes further mounting variables to better conduct heat out of the device whereas $R_{\theta JA}$ does not. In those examples for $R_{\theta JA}$, heat flow by conduction out the external terminals is very limited implying heat dissipation only by radiation or convection to the surrounding ambient (usually considered still air). This results in much higher thermal resistance from the device internal p-n junction to ambient for $R_{\theta JA}$. The heat dissipated directly into the surrounding air or space is relatively small for most discrete semiconductor devices compared to the heat conduction paths from package terminals to a substrate or heat dissipator. In addition to specifying $R_{\theta JR}$ for devices, some military performance specs for rectifiers also specify what the maximum $R_{\theta JX}$ can be with defined mounting conditions that will still meet the maximum rated I_O current without exceeding the maximum rated T_J at a specified ambient temperature such as 55°C. When the maximum $R_{\theta JX}$ is exceeded with inadequate mounting or heat sinking methods, the rated current (or power) would need to be reduced to avoid exceeding the maximum rated T_J.
Other data sheets may show power derating with T_A compared to T_L temperatures on the horizontal axis. An example is shown in Figure 1 for a 5 Watt rated axial-leaded plastic body Zener where T_A is identified with PCB mounting such as FR4. This example for T_A is insufficient for the Zener to operate at 5 Watts compared to an ideal heat sink where T_L is much better controlled. It also suggests why PCB mounting methods using FR4 are not recommended for higher power devices particularly with high density circuit designs and small mounting pads as further described in Figure 2. Other 5 Watt Zener examples are provided for mounting comparison in Figure 4 as it affects thermal impedance.

Figure 1: Power Derating Curve vs Temperature



In applications where semiconductor devices are mounted on a PCB, the device T_J can be determined from the specified $R_{\theta JR}$ on the component data sheet and measuring the reference point temperature (T_R) such as case, lead, end-cap, or solder point using a small thermocouple after thermal equilibrium is achieved with applied power to the device. The T_R measurement also becomes useful for calculating $R_{\theta RA}$ in °C/W shown in Equation 2 or $R_{\theta RX}$ in Equation 3 using the temperature difference between T_R and T_A after thermal equilibrium is achieved with the applied power such that:

Equation 8:

$R_{\theta RA} = (T_R - T_A)/P$

as influenced by the overall variables in mounting method of the component.

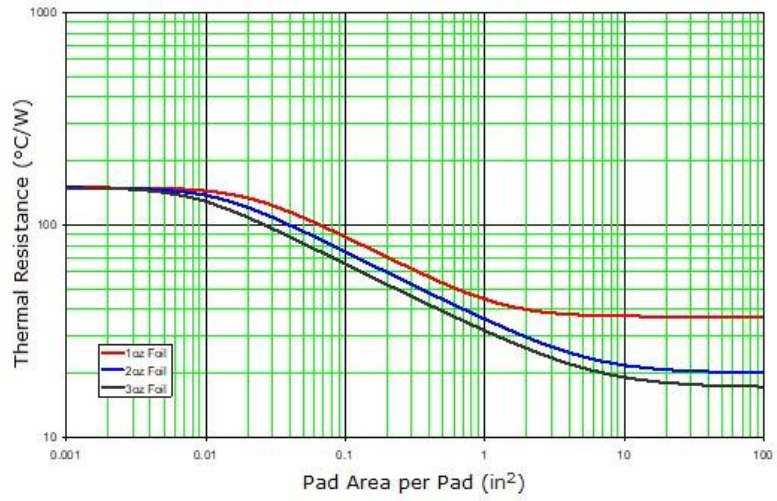
1.5 Reference Temperature

Any increase in the device mounting point reference temperature (T_R) above the surrounding ambient is a result of thermal resistance from the component reference point to ambient as described by $R_{\theta RA}$ or $R_{\theta RX}$. It also becomes a significant added factor in controlling semiconductor device junction temperatures particularly for components with higher power ratings. In worst-case mounting examples, the device package may have lower thermal resistance from junction to its external reference point compared to the added thermal resistance from that same reference point to ambient of a PCB or other heat dissipator they are mounted on. For high power devices with case mounting configurations requiring good contact for heat transfer, thermal grease may also be important as well as surface flatness between device and heatsink. As indicated earlier, the important temperature in semiconductor components for overall thermal management is T_J in Equations 1 and 4.

With this added insight, the important $R_{\theta JX}$ value and how it may be significantly influenced has also been illustrated in military diode performance specs with PCB mounting methods and variations in copper pad sizes. This may include a single layer FR4 and defined copper pads using 1 oz, 2 oz, and 3 oz copper thickness (Cu weight per square foot) that equate to copper thicknesses of 34.1 µm, 68.2 µm, and 102.3 µm respectively. These mounting variables for specific devices can also be graphically illustrated in how $R_{\theta JX}$ is affected over a significant range of copper mounting pad sizes as shown in Figure 2. This example is for 5 W rated military Zener diodes in found in MIL-PRF-19500/356 for hermetically sealed glass body devices. The effects on $R_{\theta JX}$ are significant for the range of copper pad sizes shown with a single layer PCB of FR4. There are other PCB materials beyond the scope of this application note with significantly lower values of thermal resistance such as metal core printed circuit boards (MCPCBs) as well as multiple layer boards with thermovias or combination of microvias and buried vias. Other PCB materials that are also thermally efficient include aluminum silicon carbide (AlSiC) metal matrix composites.

The illustration below shows $R_{\theta JX}$ for a 5 W rated Zener diodes in MIL-PRF-19500/356.

Figure 2: Thermal resistance versus FR4 pad area in still air



PCB horizontal (each pad) with 1 oz copper (top curve), 2 oz copper (middle curve), and 3 oz copper (bottom curve).

For small copper pad areas found in high density applications, it is not unusual for a PCB using FR4 material to add 100°C/W of unwanted thermal resistance from the device reference point to ambient in still air. Such applications also result in higher reference point temperatures at the mounting location for the component case, lead, end-cap, or solder pad (T_C, T_L, T_{EC}, or T_{SP}) despite having comparatively low thermal resistance for the component itself. When this effect is compared to the device maximum ratings for T_J, it may also require significant derating in power or current of the semiconductor component to avoid excessive p-n junction temperatures as shown in Figure 1. This also becomes important for Schottky diodes to avoid thermal runaway when operating at or near rated reverse voltages (V_{RWM}).

If there is little or no heat sinking with very small PCB copper pad sizes, the $R_{\theta JX}$ on the far-left side of Figure 2 will be much higher approaching the $R_{\theta JA}$ value per JEDEC definitions where the semiconductor device can only dissipate heat by radiation and convection into surrounding “still air”. The corresponding high values of thermal resistance in terms of $R_{\theta JA}$ are not often specified in data sheets for the component itself.

On the far-right side of Figure 2 with very large copper mounting pads and good heat sinking, the $R_{\theta JX}$ values start approaching lower values of $R_{\theta JR}$ for the device itself as typically shown in data sheets. The same applies for power devices where separate heat sink mounting methods are required instead of PCBs.

The thermal resistance junction to ambient on a specific PCB substrate material and copper pad size is also sometimes identified as $R_{\theta JA(PCB)}$ in military performance specification ratings. To avoid misleading design engineers, the value of $R_{\theta JA}$ should not be specified with a very good heat sink or large copper mounting pad sizes.

The thermal resistance junction to ambient can also be reduced with moving air resulting in improved convection effects for heat dissipation. When devices are operated in still air or a vacuum, heat removal is primarily by conduction through component terminals to the adjoining PCB substrate or other heat dissipator. When there is poor heat sink mounting, the effects of radiation and convection can be improved with moving air on axial-leaded or through-hole devices by exposing longer lead lengths between the device and mounting points. That also provides a further heat path by radiation and convection out of the device to reduce $R_{\theta JA}$ or $R_{\theta JX}$. For high density board applications, axial-leaded diode devices with generous lead lengths are also sometimes mounted vertically with the exposed upper lead bent 180 degrees back toward the PCB for solder connection that provides further added cooling in moving air.

1.6 Test Methods and Thermal Impedance

There are industry standard methods for measuring thermal resistance of semiconductor components for junction to the device reference point ($R_{\theta JR}$). Examples for diodes include JEDEC Standard JESD282B.01 section 5.7, JESD531, JESD211, as well as MIL-STD-750, Method 4081. There is presently no standardized test method for $R_{\theta JA}$. These test methods use a temperature sensitive parameter (TSP) such as the forward biased p-n junction with a known temperature coefficient to measure the T_J increase after power is applied in comparison to an external reference point temperature (T_R) on the device package. For transistors, the TSP would typically involve the emitter-base junction.

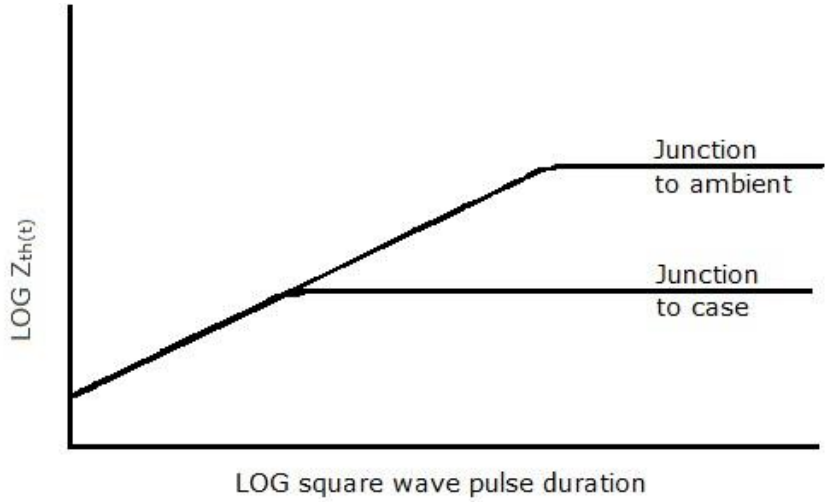
There are also similar test methods for thermal impedance or "transient thermal resistance" to measure short-term thermal transfer characteristics in the immediate vicinity of the p-n junction and die. Examples include MIL-STD-750, Method 3101 (Diodes) and Method 3131 (Transistors), as well the JEDEC specifications above. Thermal impedance ($Z_{\theta JX}$ or $Z_{th(t)}$) testing at short heating times can be efficiently performed with automatic test equipment to ensure good die bonding and/or internal contacts within the device for good heat transfer. This also permits efficient 100% screening of product. External heat sinking has no significant influence on thermal impedance at short heating times (such as 10 ms) on most semiconductor components where heat generated at the p-n junction has not yet propagated to external package regions or mounting terminals before the transient heating event has concluded.

Overall thermal impedance test characterization may include a broad spectrum of heating times from very short (< 1 ms) to very long (> 20 seconds) when thermal equilibrium is achieved for thermal resistance. Thermal impedance versus heating time graphs are often shown in data sheets including many of the military performance specs or slash sheets in MIL-PRF-19500.

The thermal impedance for semiconductors with short heating times will be lower in value than the overall package thermal resistance at thermal equilibrium. In these examples, heat from the p-n junction has not yet propagated to the outer extremities of the package or terminals. Heat flow distance versus elapsed time plot is also shown in MIL-STD-750, Method 3101 in the Appendix.

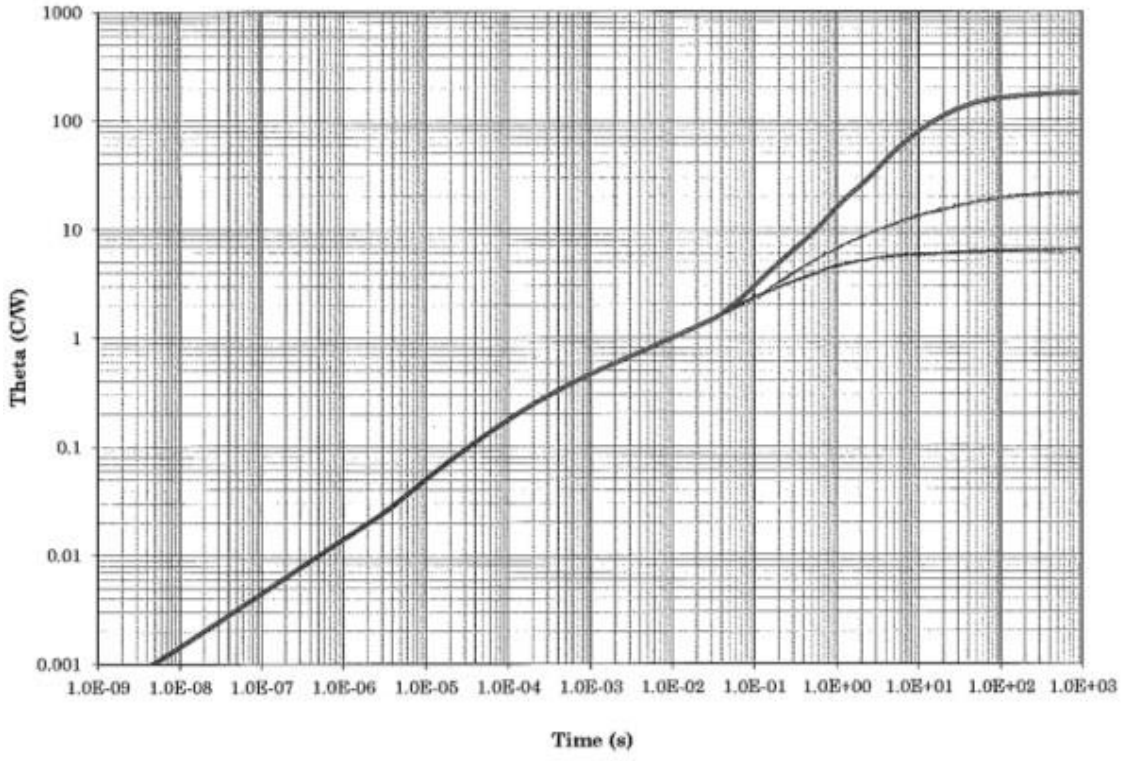
The important internal design features that influence thermal impedance at short heating times are determined by the area of the active p-n junction inside the package and the adjacent material it is bonded to (or in intimate contact with). A simplified log-log plot presentation of thermal impedance ($Z_{th(t)}$) versus heating pulse duration (square wave) is shown in Figure 3 where extended pulse durations approach thermal resistance values such as $R_{\theta JC}$ and $R_{\theta JA}$ in the flat portion of each graph at thermal equilibrium. As shown, the heating time for $R_{\theta JA}$ is longer depending on the mounting method compared to $R_{\theta JC}$ or other examples of $R_{\theta JR}$ for various package designs and their reference points. Thermal impedance in JEDEC and military specifications such as MIL-PRF-19500 and related slash sheets or performance specs is identified as $Z_{\theta JX}$, Z_{θ}, $Z_{th(t)}$, or simply "theta" to avoid subscripts.

Figure 3: Thermal Impedance vs. Heating Pulse Duration (Square Wave)



It should be noted the log-log plot in Figure 3 can deviate in linearity for rise in thermal impedance ($Z_{th(t)}$) versus pulse time for various package designs and their heat path out of the device as the pulse duration of heating increases. As an example, thermal impedance curves for 5 Watt Zeners are again shown in Figure 4. The lower curve is for surface mount devices on an infinite heat sink where the maximum rated thermal resistance is 7°C/W for $R_{\theta JEC}$ at long heating times (thermal equilibrium). The middle curve is for axial-leaded devices (through-hole mounting) on an infinite heat sink where the maximum rated $R_{\theta JL}$ is 22°C/W at a reference point 3/8 inch from the body. The upper curve is for mounting on a PCB with small FR4 pad sizes (worst-case) where thermal impedance is approaching 150°C/W for $R_{\theta JA(PCB)}$ at long heating times (see Figure 2). These values for $R_{\theta JEC}$, $R_{\theta JL}$, and $R_{\theta JA(PCB)}$ correspond to the 5 Watt Zener ratings in MIL-PRF-19500/356 for the 1N4954 thru 1N4996 series. The surface mount devices are identified with a "US" suffix that have square end caps instead of axial leads.
It is apparent significant thermal resistance is being added from the device reference point to ambient for the PCB example. If mounted on a very good heat sink, the total effective $R_{\theta JA}$ or "Theta" in Figure 4 approaches the rated $R_{\theta JL}$ in axial-leaded packages or $R_{\theta JEC}$ for surface mount packages with end caps.

Figure 4: Thermal Impedance vs. Heating Time on a 5-Watt Rated Zener

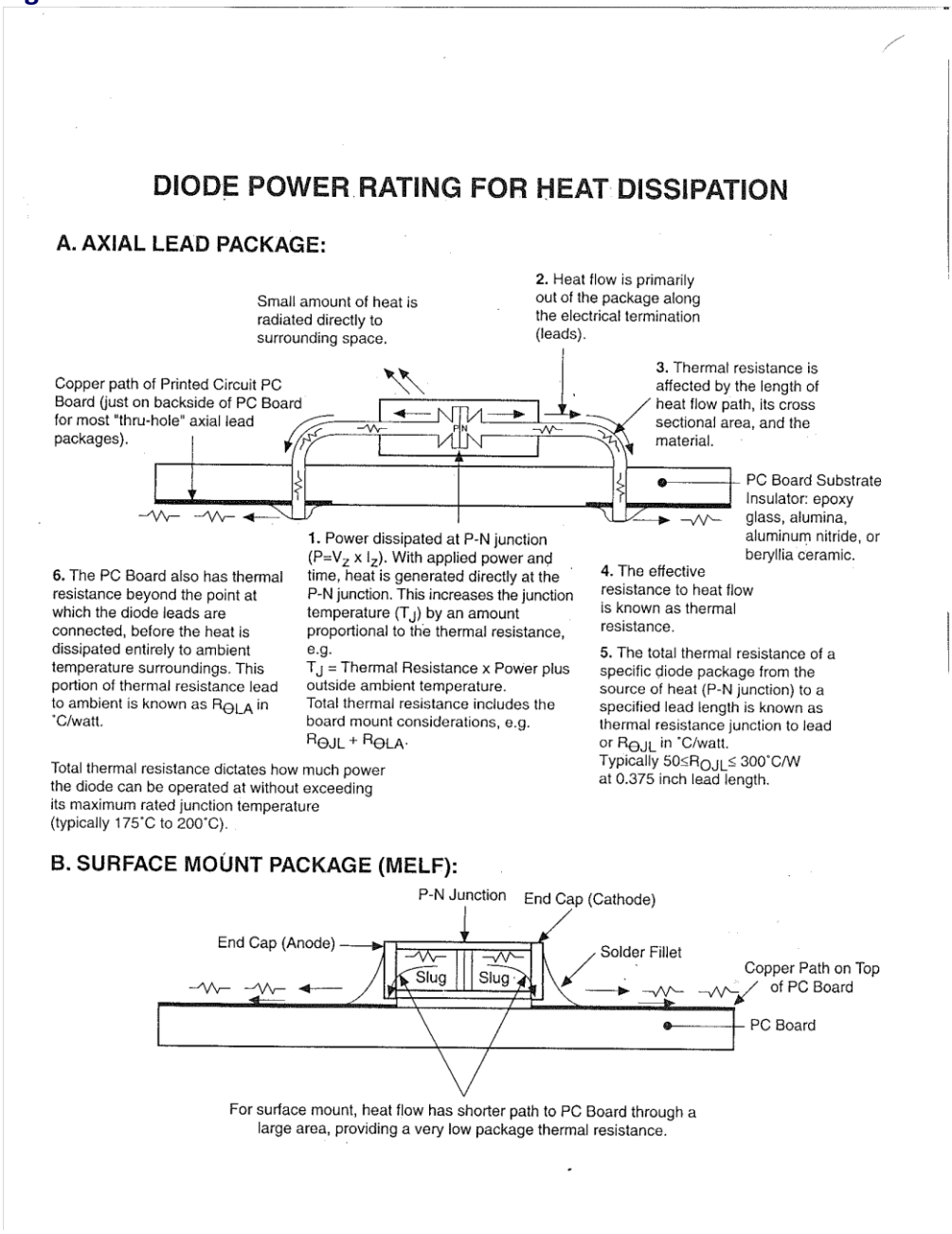


Upper curve is mounted on a PCB with small pad sizes, middle curve for an axial-leaded package on an infinite heat sink, and lower curve for a surface mount package also mounted on an infinite heat sink, and a lower curve for a surface mount package also mounted on an infinite heat sink.

1.7 Surface Mount vs. Through Hole

Surface mount packages have provided efficiencies in thermal management by minimizing parasitic thermal resistance from long lead terminations on "through-hole" components when there is good heat sinking available. Examples such as TO-18 or TO-39 leaded packages for transistors can also be optionally mounted with a heat sink directly on the case (lid) to take advantage of a much lower $R_{\theta JC}$ compared to heat flow out the leads. Other axial-leaded diodes also have higher thermal resistance values compared to their surface mount equivalents as shown in Figure 4. These thermal flow differences are shown in Figure 5 for axial-leaded designs (DO-204) and surface mount diode designs often identified as a Metal Electrode Leadless Face (MELF) packages (DO-213) with end caps for mounting.

Figure 5: Heat Flow for axial-leaded and surface mount diodes



Many surface mount devices (SMDs) using the same active die, package size, and electrical features as their older through-hole counterparts can be operated much cooler in still air for the same applied power and good mounting practices for optimizing thermal management. If a leaded carrier or "interposer" is also used between a larger size SMD and the PCB or other substrate to relieve stresses (such as for TO-276 package outlines), the added parasitic thermal resistance of the carrier must also be considered. Surface mount package designs also minimize other parasitics such as inductance (L) that can improve performance for Transient Voltage Suppressors (TVSs). In those examples, the voltage overshoot from a very fast rising transient (v = -Ldi/dt) are minimized that compromise clamping voltage (V_C) as described in MicroNote 111.

The thermal management or heat sinking for TVSs is not important in most applications where the device is idling with negligible power (and heating) at the rated Working Standoff Voltage (V_{WM}) well below the avalanche breakdown region with very low leakage currents until a short high power transient occurs. Most TVSs are rated at 1 ms or less for Peak Pulse Power (P_{PP}) where the transient event is concluded before heat travels to the external terminals and mounting points. For very long transients or "abnormal voltages" well beyond 1 ms, thermal management again becomes important similar to Zeners that are used for voltage regulation with continuous applied current and power. For combined Zener and TVS applications requiring continuous voltage regulation and transient protection, MicroNote 134 should be reviewed.

1.8 Summary

Overall thermal management is important for discrete semiconductor devices. As reflected in both JEDEC and military test standards, semiconductor devices are primarily characterized for thermal resistance junction to a reference point on the device. However those same devices are also significantly influenced by numerous mounting methods found in typical applications resulting in added thermal resistance from the device reference point to ambient as best described by $R_{\theta JX}$. As a result, it is incumbent on the user to also understand what the additional thermal resistance is from the device reference point to ambient. In examples where thermal resistance junction to ambient ($R_{\theta JA}$) is also specified on a device data sheet or performance spec, it needs to be carefully reviewed by the design engineer as to how it is defined compared to the actual application.

1.9 Support

For additional technical information, please contact Design Support at:
http://www.microsemi.com/designsupport
or
Kent Walters (kwalters@microsemi.com) at 480-302-1144

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com