AN2794

SAM L10/SAM L11 Op Amp as ADC Gain Amplifier

Abstract

The Microchip® SAM L10/SAM L11 includes three on-chip operational amplifiers (op amp). The Operational Amplifier Controller module offers the most common inverting and non-inverting programmable gain and hysteresis configurations. Each op amp is software configurable and can be used as a standalone general purpose operational amplifier. This document introduces the configuration and usage of the op amp module, different built-in modes, and presents an application example. In the application example, one of the operational amplifiers is configured as a non-inverting gain amplifier with output internally connected to the ADC. With this setup, the op amp operates as a gain amplifier stage for ADC sampling.

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1. Introduction

This document introduces the Operational Amplifier Controller (OPAMP) module on the SAM L10/SAM L11. The operational amplifiers can be software configured and combined to many different modes, as described in the product data sheet. Before the OPAMP module is further investigated, a brief introduction to ideal operational amplifiers and the application example is presented.

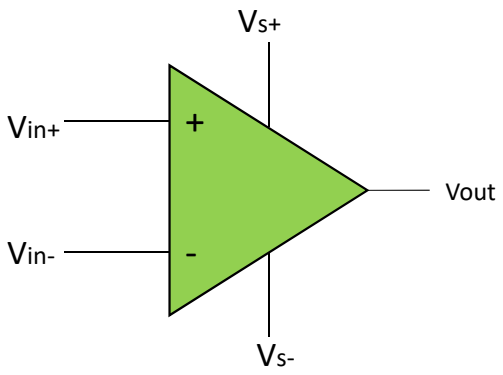
1.1 Operational Amplifiers

An operational amplifier (op amp) is an electronic component designed for voltage gain amplification. Op amps most often include a differential input (Vin±), inputs for a power supply (Vs±), and a single output (Vout). For an ideal op amp, the following two laws will determine its main properties:

1. The op amp will attempt to keep the differential inputs the same (Vin+ =Vin-).
2. No current flows into or out of the differential inputs. For a non-ideal op amp the low leakage current is due to the high impedance input stage composed by the transistor gates.

Using these two laws, many configurations for different purposes can be obtained by creating circuits with op amps and other components, often resistors. The most common configurations are available as built-in modes on the SAM L10/SAM L11 as presented in Built-In Modes.

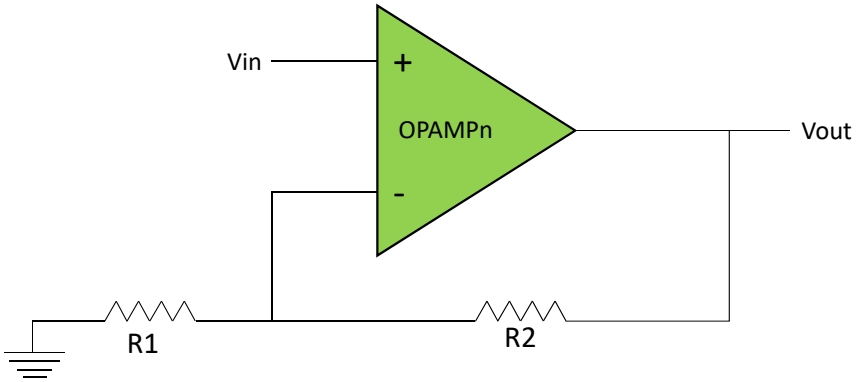
Figure 1-1. Ideal Op Amp



1.2 Introduction to the Application Example

In the code example, one of the op amps is configured as a non-inverting Programmable Gain Amplifier (PGA) with output internally connected to the ADC module for signal sampling. The input reference signal is connected to the non-inverting (positive) input while the inverting (negative) input, and the output is connected in a closed loop with an internal resistor ladder, as shown in Non-Inverting PGA. For a non-inverting PGA, the ideal amplified output is given in the below equation:

Figure 1-2. Non-Inverting PGA



Vout = Vin (1 + R2/R1), which is derived using the two laws of an ideal op-amp.

The example is useful when sampling a low-voltage measurement, and there is a need for gain amplification. Recalling the laws for an ideal op-amp, no current flows into the inputs. This property, known as buffering, is valuable for minimizing the impact of the measurement on the voltage.

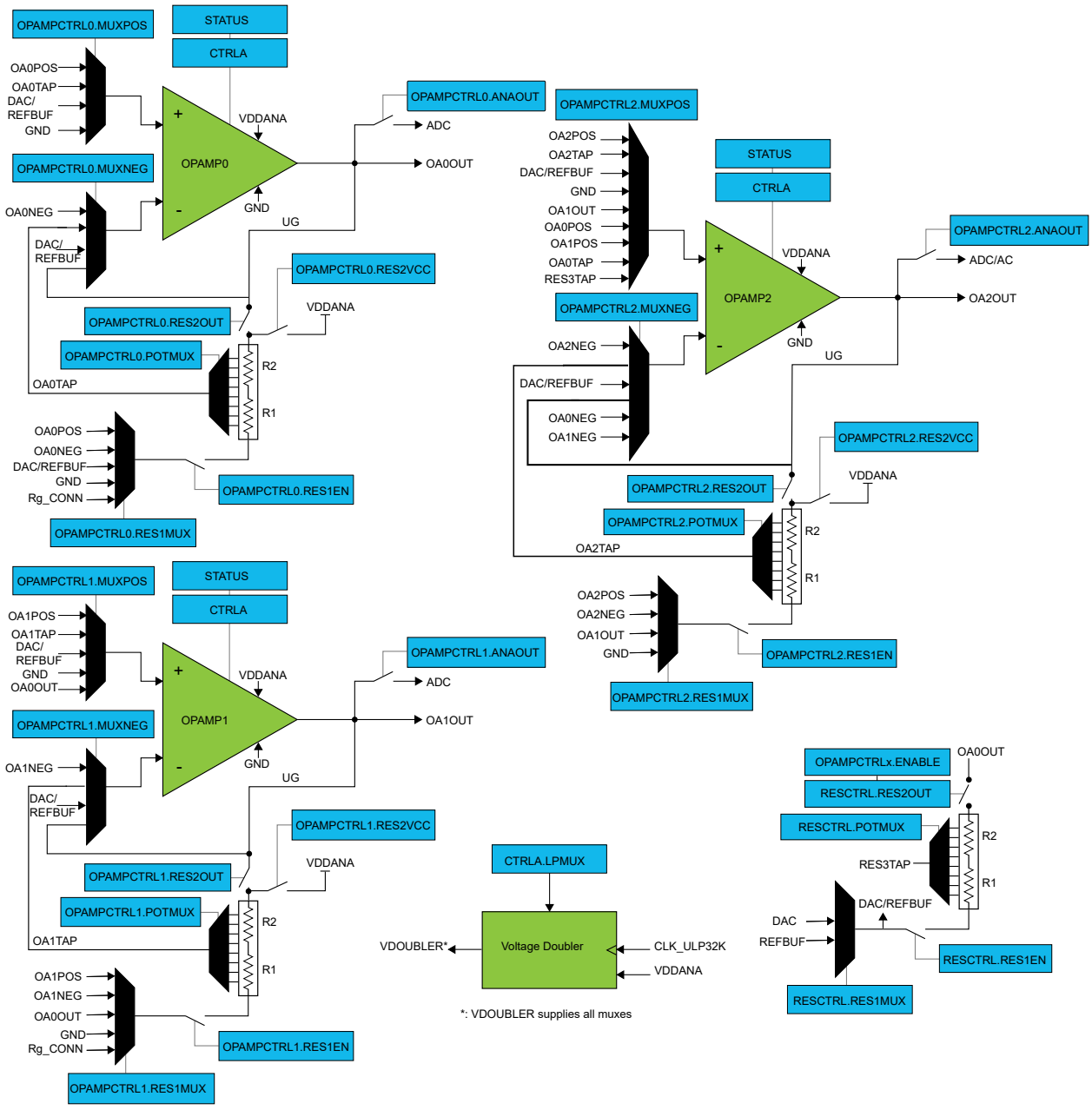
1.2.1 Prerequisites

Running the example, as described in this application note, requires: SAM L10/SAM L11 Xplained Pro Evaluation Kit with USB cable.

2. Module Overview

The block diagram of the op amp module is shown in the below figure. Each individual op amp is configured by its respective Operational Amplifier Control (OPAMPCTRLx) register.

Figure 2-1. OPAMP Block Diagram



2.1 Configuring the Operational Amplifiers

The OPAMP settings must be configured before the amplifier is enabled. The following is a brief description of significant bit fields and groups in the Operational Amplifier Control registers:

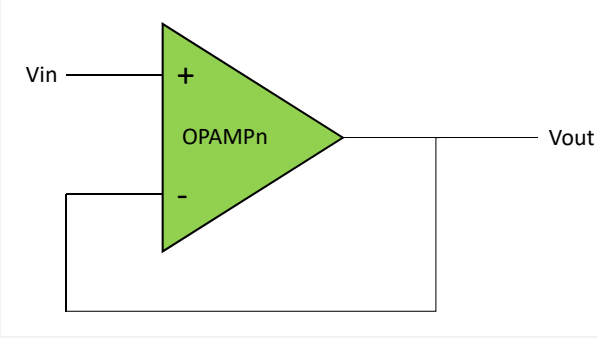
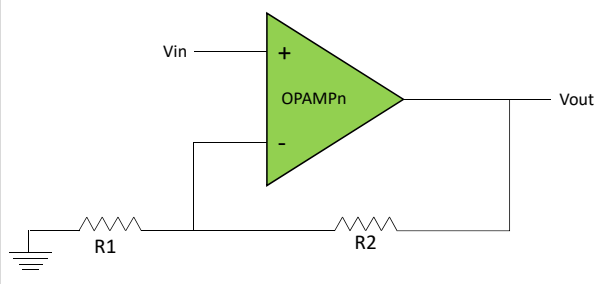
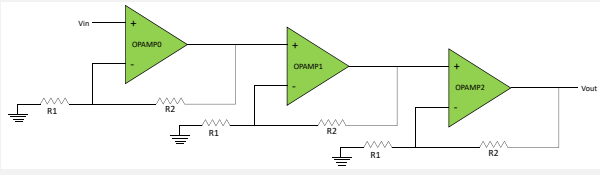
- Select the positive input in OPAMPCTRLx.MUXPOS

- Select the negative input in OPAMPCTRLx.MUXNEG
- Select OPAMPCTRLx.RES1EN if resistor ladder issued
- Select the input for the resistor ladder in OPAMPCTRLx.RES1MUX
- Select the potentiometer selection of the resistor ladder in OPAMPCTRLx.POTMUX
- Select the VCC input for the resistor ladder in OPAMPCTRLx.RES2VCC
- Connect the operational amplifier output to the resistor ladder using OPAMPCTRLx.RES2OUT
- Select the trade-off between speed and energy consumption in OPAMPCTRLx.BIAS

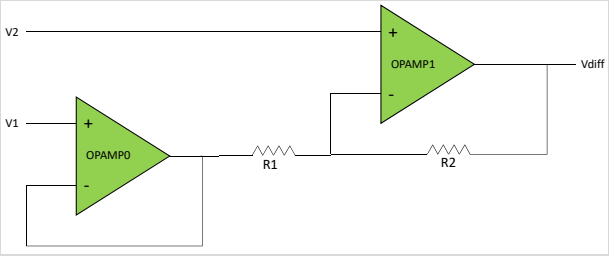
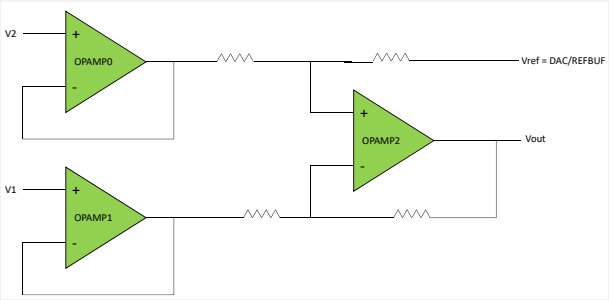
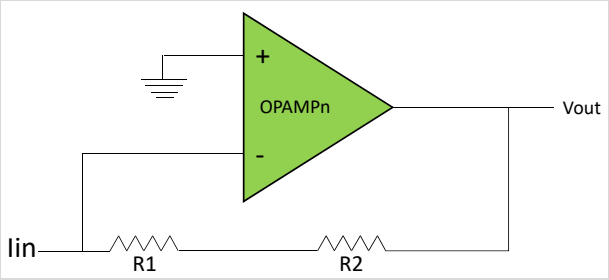
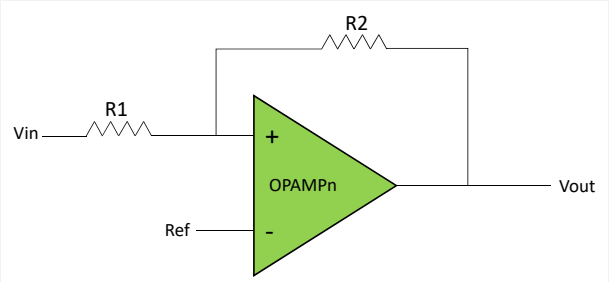
2.2 Built-In Modes

The op amp module includes software configurable internal connections that enables the most common op-amp modes. The different modes are briefly introduced in the following table. For additional information related to implementation of the built-in modes, refer to the product data sheet.

Table 2-1. Built-In Modes

Mode	Figure
Voltage Follower A unity gain amplifier. Vout = Vin	**Figure 2-2. Voltage Follower** 
Inverting/Non-Inverting PGA A software configurable Programmable Gain Amplifier (PGA) using the internal resistor ladder. Vout = Vin (1 + R2/R1)	**Figure 2-3. Non-Inverting PGA** 
Cascaded Inverting/Non-Inverting PGA The OPAMPs can be internally connected in cascade to provide a larger variety of gains. Vout = Vin (1 + R2/R1)(1 + R2/R1)(1 + R2/R1)	**Figure 2-4. Cascaded Non-Inverting PGA** 

.....continued

Mode	Figure
Differential Amplifier A Voltage Follower and a non-inverting PGA connected in cascade. Vdiff = (V2 - V1) R2/R1	**Figure 2-5. Differential Amplifier** 
Instrumentation Amplifier A Differential Amplifier with input buffer amplifiers. Vout = (V2 - V1) Gain + Ref	**Figure 2-6. Instrumentation Amplifier** 
Transimpedance Amplifier For converting current to voltage. Vout = -Iin (R1 + R2)	**Figure 2-7. Transimpedance Amplifier** 
Programmable Hysteresis Inverting or Non-Inverting comparator with programmable hysteresis. Threshold = ±Vcc R2/R1 + Ref	**Figure 2-8. Non-Inverting Comparator with Programmable Hysteresis** 

2.3 Low-Power Mode

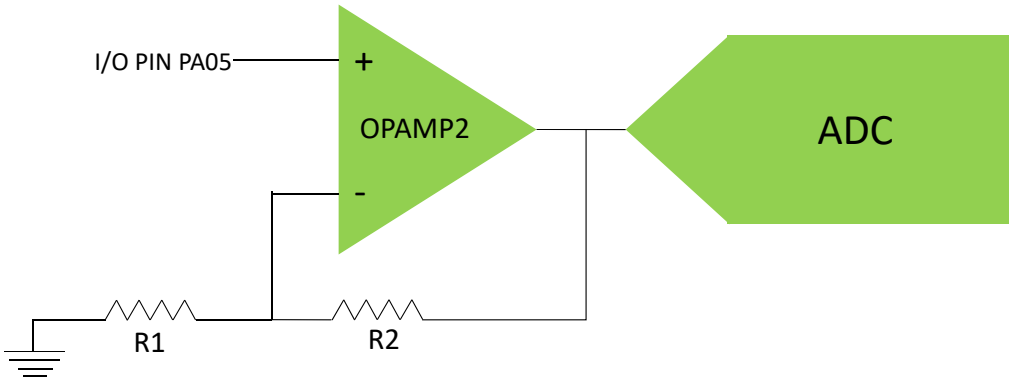
For low-power applications, the op amp module contains settings for power saving. One of them is to trade off speed versus power efficiency to get the lowest power consumption. The speed setting is configured for each amplifier individually by the Bias Control field in the Operational Amplifier x Control

register (OPAMPCTRLx.BIAS). The BIAS bits select the amount of bias current provided to the operational amplifiers. This will also affect the start-up time. Another low-power configuration is to disable the voltage doubler by setting the Low-Power Mux bit in the Control Register (CTRLA.LPMUX), if the supply voltage is guaranteed to be above 2.5V. Disabling the voltage doubler saves power and reduces the start-up time. The Analog-On-Demand feature allows the ADC and the AC analog peripherals to automatically enable the OPAMPx only when it is needed, thereby allowing a reduction in power consumption. When OPAMPCTRLx.ONDEMAND=1, the analog block is powered off for the lowest power consumption if it is not requested.

3. Example Overview

In the application example, the OPAMP2 is configured as a non-inverting PGA. The amplified output is enabled for sampling with the ADC. As mentioned in the product data sheet, the OPAMP2 positive input can be multiplexed to the I/O pin PA05. Therefore, the input signal to be amplified must be connected to this pin. The pin must also be configured as an input. The ADC needs to be configured to use the OPAMP2 output as input.

Figure 3-1. OPAMP2 Configured as Non-Inverting PGA with Output Connected to the ADC Module



In this example OPAMP2 is configured with R2/R1 = 1/3 and the internal connection to the ADC is enabled. When OPAMP2 is configured and enabled in the main loop, the ADC starts converting a predefined number of samples of the amplified signal. The ADC is configured in callback mode, implying that an interrupt occurs when the conversion is complete. The ADC result can be verified as:

ADC result (in Volts) = (1+ R2/R1) x Vin = (1 + 1/3) x Vin

3.1 Application Configuration and Implementation

Oscillator and GCLK Configuration:

- Configure the 16 MHz internal oscillator frequency to 16 MHz by setting OSC16MCTRL.FSEL[1:0] to 0x11. Enable the 16 MHz internal oscillator by setting OSC16MCTRL.ENABLE to 1.
- Configure the GCLK0 clock source to 16 MHz oscillator output by setting GENCTRL0.SRC[4:0] to 0x05 (OSC16M oscillator output). Enable GCLK0 by setting GENCTRL0.GENEN to 1.

Operational Amplifier Controller (OPAMP) Configuration:

The following steps describe the important register settings for configuring OPAMP2 as a non-inverting programmable gain amplifier with a gain of 1+1/3.

1. Select OA2POS as the positive input of OPAMP2 by setting OPAMPCTRL2.MUXPOS[3:0] to 0x00 (OPAMPx Positive Input).
2. PA05 is used as the OPAMP input. Assign the OA2POS peripheral function to PA05 by setting the PMUX2.PMUXO[3:0] to 0x01 (Peripheral Function B Selected).
3. Select Resistor Ladder Taps as the negative input of OPAMP2 by setting OPAMPCTRL2.MUXNEG[3:0] to 0x01 (OPAMPx Resistor Ladder Taps).
4. Enable the Resistor ladder. Set OPAMPCTRL2.RES1EN to 1.
5. Select GND as input to the Resistor ladder by setting OPAMPCTRL2.RES1MUX[2:0] to 0x03.

6. Set the Potentiometer selection for the resistor ladder to 1/3 by setting OPAMPCTRL2.POTMUX[2:0] to 1. This sets R1 to 12R and R2 to 4R.
7. Connect the resistor ladder to the operational amplifier output by setting OPAMPCTRL.REST2OUT to 1.
8. Close the switch that connects the OPAMP2 output to the ADC input by setting OPAMPCTRL2.ANAOUT to 1.

Analog-to-Digital Converter (ADC) Configuration:

The following steps describe the important register settings for configuring ADC to convert the OPAMP input.

1. Select GCLK0 as the clock source to the ADC module by configuring PCHCTRL20.GEN[2:0] to 0x0 (Generic Clock Generator 0).
2. Divide the input clock to the ADC peripheral by 8 by setting CTRLB.PRESCALER[2:0] to 0x02.
3. Assign OA2POS peripheral function to PA05 by setting PMUX2.PMUXO[3:0] to 0x01 (Peripheral Function B Selected).
4. Select OPAMP2 output as the positive input of the ADC by setting INPUTCTRL.MUXPOS[4:0] to 0x1F (OPAMP2 Output).
5. Select GND as the negative input of the ADC by setting INPUTCTRL.MUXNEG[4:0] to 0x18 (Internal ground).
6. Set the ADC reference voltage to ½ VDDANA by setting REFCTRL.REFSEL[3:0] to 0x02.
7. Set the ADC resolution to 12-bit by setting CTRLC.RESSEL[1:0] to 0x0.

Note:

1. The ADC clock prescaler must be set according to the specifications of the ADC module, and the speed of the clock source. The ADC clock speed should not exceed the maximum conversion frequency.
2. The ADC is mostly configured with default settings. The accuracy of the sampling can be increased by applying built-in software selectable features to accumulate and divide samples for averaging and gain and offset correction.

In the application code, enable the ADC Result Ready interrupt (INTENSET.RESRDY = 1) and the ADC module (CTRLA.ENABLE=1). Enable the OPAMP module (CTRLA.ENABLE=1) and wait for the OPAMP module to be ready by polling the STATUS.READYx bit (where x = 2, corresponding to OPAMP2).

Start the first ADC conversion by setting SWTRIG.START to 1. The subsequent ADC conversions are triggered from the ADC interrupt by setting the SWTRIG.START to 1 in the ADC result ready interrupt handler.

Note: The amplified signal voltage can be calculated from the ADC result buffer values according to: adc_result_buffer * V_REF / ADC_MAX_VALUE, where V_REF is the sampling voltage reference (ADC_REFERENCE_INTVCC1) and ADC_MAX_VALUE is 0xFFF for a 12-bit conversion.

3.2 Importing Atmel Start Project into Atmel Studio

The example application corresponding to this document can be downloaded from the following web site: start.atmel.com. Follow these steps to download the example project:

1. Go to start.atmel.com and click **Browse Examples.**
2. Search for the `ADC Gain Amplifier` example.

3. Select the `ADC Gain Amplifier` example, and then click **Download Selected Example** to download the project.
4. Once prompted, select the board to use.

3.3 Summary

The SAM L10/SAM L11 operational amplifiers can be used for many purposes. This document describes how to use the on-chip op amp module as a non-inverting amplifier, and how to configure the op amp and ADC modules, such that the output of the OPAMP2 is sampled by the ADC.

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