

AVR16/32DD14/20 Silicon Errata and Data Sheet Clarification

AVR16/32DD14/20



The AVR32/16DD14/20 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002413), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR32/16DD14/20 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002413) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A1 ⁽¹⁾	Rev. A2	Rev. A3
Device	2.2.1. Multiple High Voltage Pulses in Series can Force Pin PF7 to Remain in UPDI Configuration	X	X	X
	2.2.2. The CLKSEL Fuse can Force PF7 to Remain in UPDI Configuration	X	-	-
	2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X	X
NVMCTRL	2.3.1. Flash Multi-Page Erase Can Erase Write Protected Section	X	X	X
TCD	2.4.1. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X	X
USART	2.5.1. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

2.2 Device

2.2.1 Multiple High Voltage Pulses in Series can Force Pin PF7 to Remain in UPDI Configuration

If applying multiple high voltage pulses to the Reset pin within a 100 ms timeframe, pin PF7 will remain as a UPDI pin even if no UPDI key is given. If PF7 is configured as GPIO pin (UPDIPINCFG is '0' in FUSE.SYSCFG0), it will only return to GPIO mode after a Reset is issued by either POR or BOD.

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. A2	Rev. A3
X	X	X

2.2.2 The CLKSEL Fuse can Force PF7 to Remain in UPDI Configuration

When the CLKSEL fuse is configured to OSC32K and a high voltage pulse is applied to the Reset pin, pin PF7 will remain as a UPDI pin even if no UPDI key is given. If PF7 is configured to GPIO pin (UPDIPINCFG is '0' in FUSE.SYSCFG0), it will only return to GPIO mode after a Reset is issued by POR.

Work Around

Do not configure the PF7 pin to the GPIO mode if the CLKSEL fuse is configured to OSC32K.

Affected Silicon Revisions

Rev. A1	Rev. A2	Rev. A3
X	-	-

2.2.3 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by an ST/STD instruction to address < 64 or SLPCTRL.CTRLA will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64 , or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA

Affected Silicon Revisions

Rev. A1	Rev. A2	Rev. A3
X	X	X

2.3 NVMCTRL - Nonvolatile Memory Controller

2.3.1 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. A2	Rev. A3
X	X	X

2.4 TCD - 12-Bit Timer/Counter Type D

2.4.1 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A1	Rev. A2	Rev. A3
X	X	X

2.5 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.5.1 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A1	Rev. A2	Rev. A3
X	X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002413).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	09/2023	Added new silicon revision (Rev. A3)
C	08/2022	Added new silicon revision (Rev. A2)
B	06/2022	Changed the revision of the initial release of the silicon
A	05/2022	Initial document release

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