# PolarFire FPGA Packaging and Pin Descriptions User Guide

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## Introduction (Ask a Question)

This user guide provides pin and packaging information, such as bank assignments and mechanical information for PolarFire® FPGAs.

PolarFire FPGAs feature a flexible I/O structure that supports a range of mixed voltages (1.1V, 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V) through bank selection. High Speed Input/Output (HSIO) and General Purpose Input/Output (GPIO) are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide.

The AXI4 Lite, AXI4 Stream, and AXI4 protocol standard uses the terminology **Master** and **Slave**. The equivalent Microchip terminology used in this document is **Initiator** and **Target** respectively.


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# 1. Packaging Overview (Ask a Question)

PolarFire FPGAs are available in multiple packages. Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. The HSIO and GPIO banks have a maximum supply voltage of 1.8V and 3.3V, respectively.

The following table lists the PolarFire FPGA variants, with user I/O and XCVR lanes, in Pb-free packages.

**Table 1-1.** PolarFire FPGA Product Family[1]

| Features | | MPF050T | MPF100T | MPF200T | MPF300T | MPF500T |
|---|---|---|---|---|---|---|
| FPGA Fabric | Logic Elements (4 LUT + DFF) | 48 | 109 | 192 | 300 | 481 |
| | Math Blocks (18 × 18 MACC) | 150 | 336 | 588 | 924 | 1480 |
| | LSRAM Blocks (20 kbit) | 160 | 352 | 616 | 952 | 1520 |
| | µSRAM Blocks (64 × 12) | 450 | 1008 | 1764 | 2772 | 4440 |
| | Total RAM (Mbits) | 3.6 | 7.6 | 13.3 | 20.6 | 33 |
| | µPROM (Kbits 9-bit bus) | 216 | 297 | 297 | 459 | 513 |
| | User DLLs/PLLs | 8 | 8 | 8 | 8 | 8 |
| High-Speed I/O | 250 Mbps to 10.3125 Gbps Transceiver Lanes | 4 | 8 | 16 | 16 | 24 |
| | PCIe® Gen2 End Points/Root Ports | 2 | 2 | 2 | 2 | 2 |
| Total I/Os | Total User I/Os | 176 | 284 | 368 | 512 | 584 |
| Packaging | Type/Size/Pitch | — | Total User I/O (HSIO/GPIO)/Transceivers | | | |
| | FCSG325 (11 mm × 11 mm, 11 mm × 14.5 mm, 0.5 mm) | 168(84/80)/4 | 170(84/86)/4 | 170(84/86)/4 | — | — |
| | FCSG536 (16 mm × 16 mm, 0.5 mm) | — | — | 300(120/180)/4 | 300(120/180)/4 | — |
| | FCVG484 (19 mm × 19 mm, 0.8 mm) | 188(96/92)/4 | 284(120/164)/4 | 284(120/164)/4 | 284(120/164)/4 | — |
| | FCG484 (23 mm × 23 mm, 1.0 mm) | — | 244(96/148)/8 | 244(96/148)/8 | 244(96/148)/8 | — |
| | FCG784 (29 mm × 29 mm, 1.0 mm) | — | — | 364(132/232)/16 | 388(156/232)/16 | 388(156/232)/16 |
| | FCG1152 (35 mm × 35 mm, 1.0 mm) | — | — | — | 512(276/236)/16 | 584(324/260)/24 |

**Important:**

1. Devices in the same package are pin compatible. For more information about multiple speed grades, temperatures, and package combinations, see the Ordering Information section in PolarFire FPGA Product Overview.


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# 2. Bank Locations (Ask a Question)

PolarFire FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/Os with compatible standards are assigned to the same I/O voltage bank.

The following figures show the bank locations for the MPF050T, MPF100T, MPF200T, MPF300T, and MPF500T devices with available package combinations.

**Figure 2-1.** PolarFire MPF500T-FCG1152 I/O Bank Locations

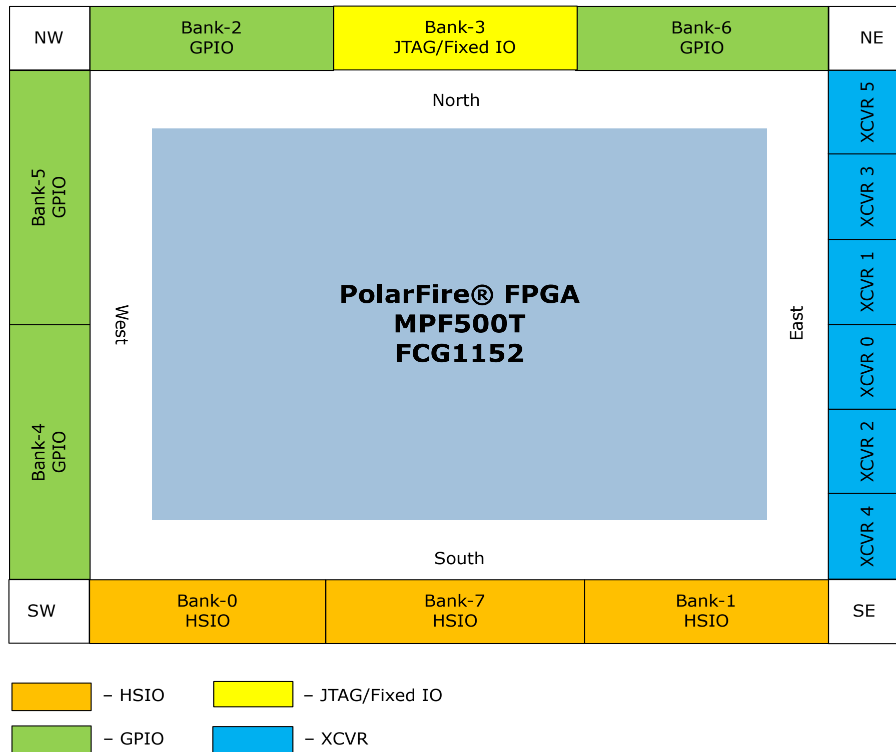



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**Figure 2-2.** PolarFire MPF300T-FCG1152 I/O Bank Locations

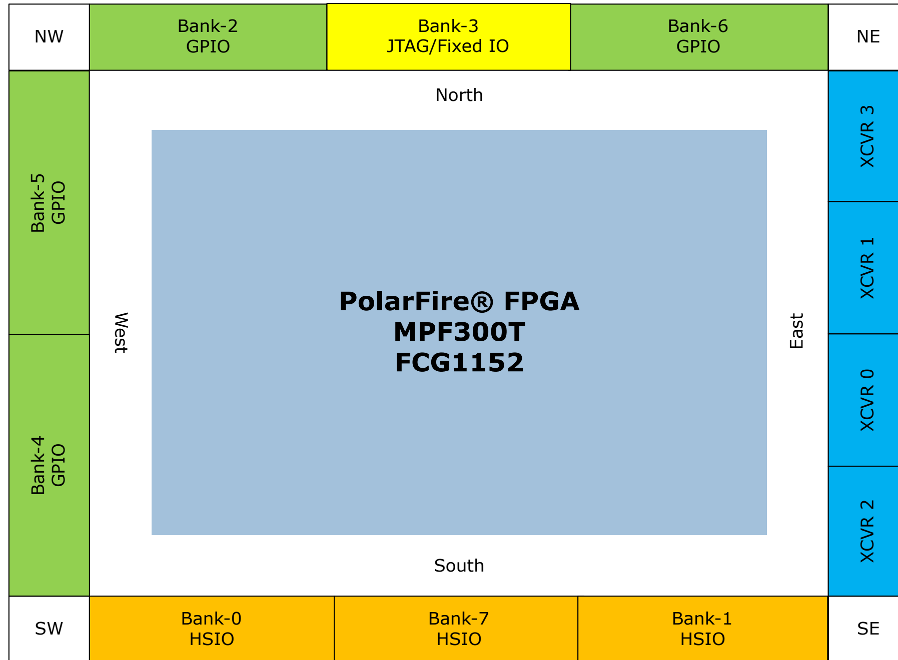


**Figure 2-3.** PolarFire MPF500T/MPF300T-FCG784 I/O Bank Locations

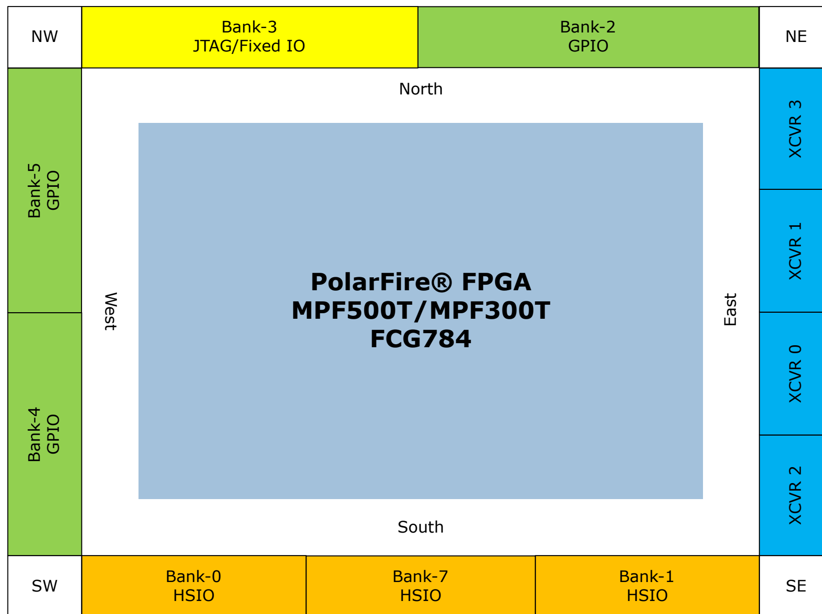



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**Figure 2-4.** PolarFire MPF200T-FCG784 I/O Bank Locations

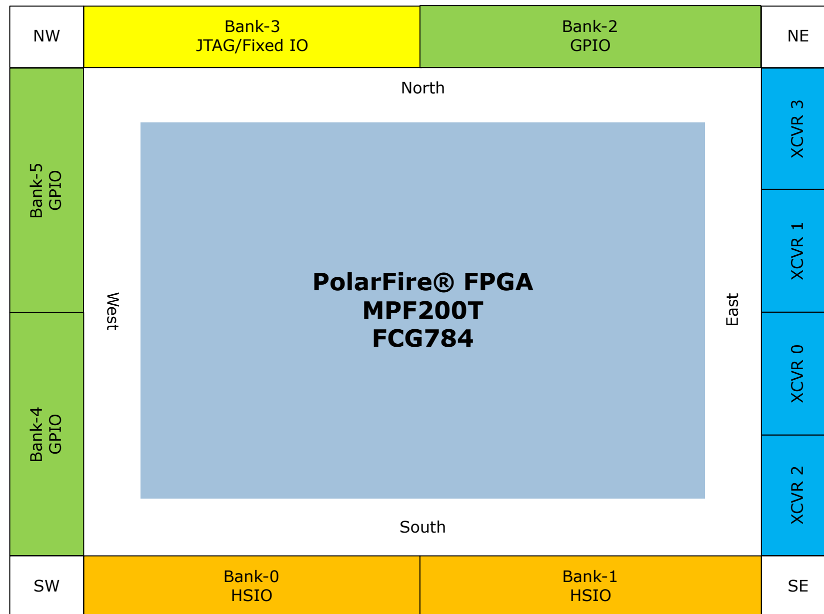
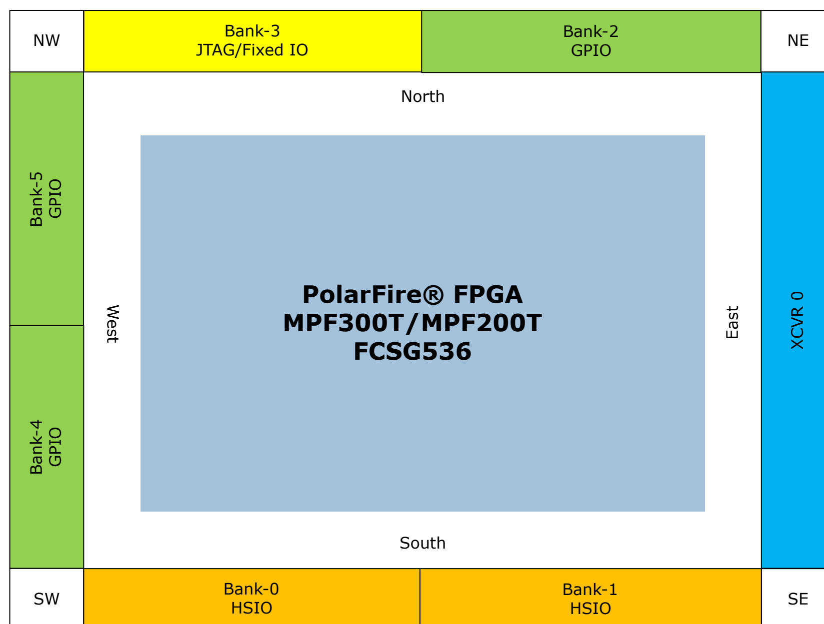



**Figure 2-5.** PolarFire MPF300T/MPF200T-FCSG536 I/O Bank Locations




**Important:** Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively within the package substrate for pin migration compatibility.


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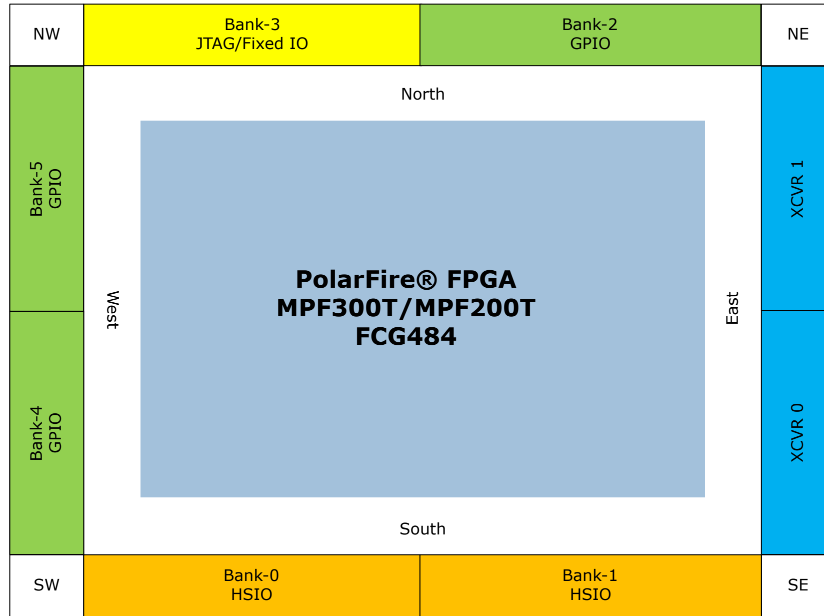
**Figure 2-6.** PolarFire MPF300T/MPF200T-FCG484 I/O Bank Locations




**Important:** In MPF300T and MPF200T devices, Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively, within the package substrate for pin migration compatibility.

**Figure 2-7.** PolarFire MPF100T-FCG484 I/O Bank Locations

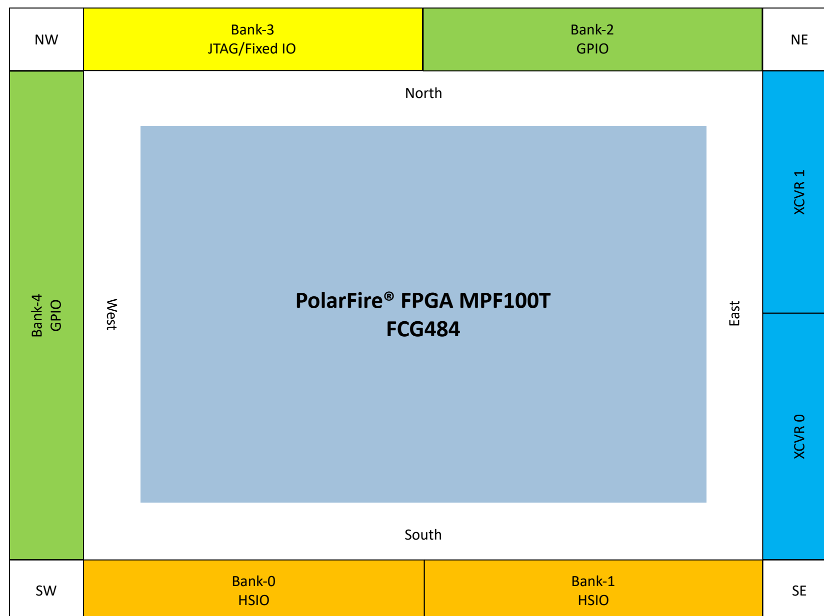




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**Figure 2-8.** PolarFire MPF300T/MPF200T/MPF100T/MPF050T-FCVG484 I/O Bank Locations

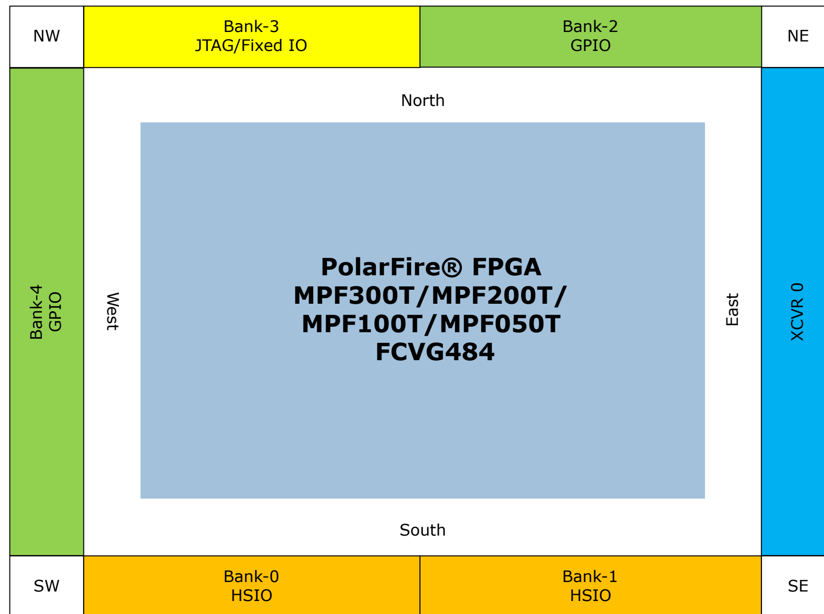
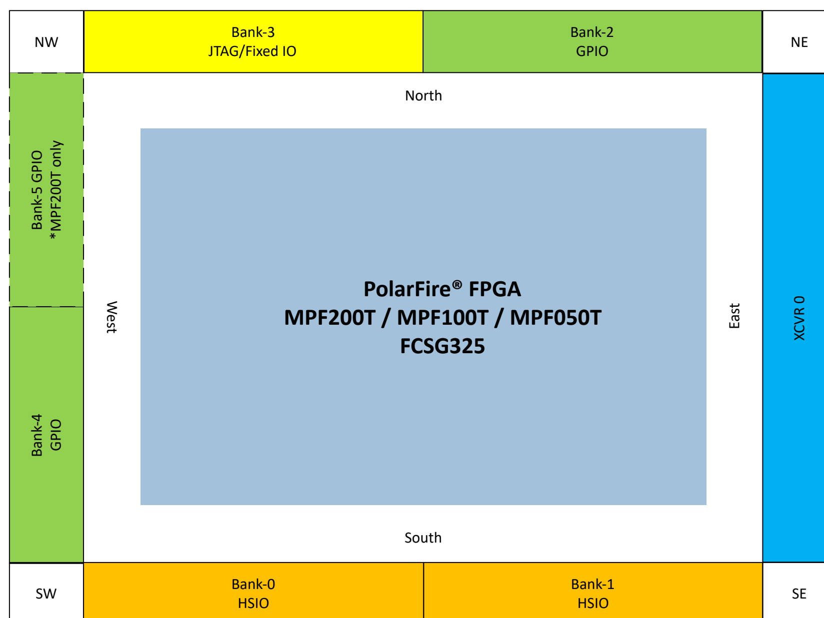



**Figure 2-9.** PolarFire MPF200T/MPF100T/MPF050T-FCSG325 I/O Bank Locations




**Important:** In MPF200T devices, Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively, within the package substrate for pin migration compatibility.

The following table lists the organization of the I/O banks in PolarFire FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe® is supported only in XCVR0.


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**Table 2-1.** Organization of I/O Banks

| Bank Number | FCG1152 | | FCG784 | | FCSG536 | FCG484 | | FCVG484 | FCSG325 |
|---|---|---|---|---|---|---|---|---|---|
| | MPF500T | MPF300T | MPF500T **MPF300T** | MPF200T | MPF300T **MPF200T** | MPF300T **MPF200T** | MPF100T | MPF300T **MPF200T** **MPF100T** MPF050T | MPF200T **MPF100T** MPF050T |
| Bank 0 | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO |
| Bank 1 | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO | HSIO |
| Bank 2 | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| Bank 3 | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O | JTAG/ FIXED I/O |
| Bank 4 | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| Bank 5 | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | — | — | — |
| Bank 6 | HSIO | HSIO | — | — | — | — | — | — | — |
| Bank 7 | HSIO | HSIO | HSIO | — | — | — | — | — | — |
| XCVR 0 | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| XCVR 1 | Yes | Yes | Yes | Yes | — | Yes | Yes | — | — |
| XCVR 2 | Yes | Yes | Yes | Yes | — | — | — | — | — |
| XCVR 3 | Yes | Yes | Yes | Yes | — | — | — | — | — |
| XCVR 4 | Yes | — | — | — | — | — | — | — | — |
| XCVR 5 | Yes | — | — | — | — | — | — | — | — |

Each I/O bank supports multiple DDR lanes. If the CDR/SGMII interface is connected to the I/O bank, then Tx and Rx signals must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane.

For more information about DDR lanes for each package in Package Pin Assignment Tables (PPATs), see www.microchip.com/en-us/products/fpgas-and-plds/fpgas/polarfire-fpgas/polarfire-mid-range-fpgas#overview.

The following table lists the XCVR channels for a PolarFire device/package.

**Table 2-2.** Serial Transceiver Channels

| Device | FCG1152 | FCG784 | FCG484 | FCVG484 | FCSG536 | FCSG325 |
|---|---|---|---|---|---|---|
| MPF500T | 24 | 16 | — | — | — | — |
| MPF300T | 16 | 16 | 8 | 4 | 4 | — |
| MPF200T | — | 16 | 8 | 4 | 4 | 4 |
| MPF100T | — | — | 8 | 4 | — | 4 |
| MPF050T | — | — | — | 4 | — | 4 |


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# 3. Packaging Pin Assignment (Ask a Question)

The Packaging Pin Assignment Table (PPAT) information is available in the Packing section, for more information, see the PolarFire FPGAs Documentation Web Page. PPAT contains information about recommended DDR pin-outs, PCI Express capability for XCVR0, DDR Lane information for I/O CDR, and generic IOD interface pin placement.


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# 4. IOD Interfaces (Ask a Question)

PolarFire pinouts can migrate between device densities in the same packages with regard to compatible PCB footprints. This is generally true for power, ground, general purpose pin usage, and XCVR lanes. However, upward and downward pin migration of different PolarFire logic densities in the same package can vary when using high-speed IOD interfaces, such as memory interfaces or generic DDR interfaces.

Microchip recommends initially targeting the intended lowest density device to achieve the full I/O migration with IOD interfaces before committing a final footprint to a PCB design.

Using Libero® SoC to verify the pinout in the same package with the lowest density allows footprint compatibility for smoother density migration with the IOD interfaces. This approach allows designs to initially use a larger density while providing the path to reduce to lower density.

**Table 4-1.** IOD Interfaces

| Device | Operating Condition | Speed Grade | Core Voltage |
|---|---|---|---|
| MPF050T/TL | EXT | STD | 1.0V/1.05V |
| MPF050T/TL/TS/TLS | IND | STD | 1.0V/1.05V |
| MPF050T | EXT | –1 | 1.0V/1.05V |
| MPF050T/TS | IND | –1 | 1.0V/1.05V |

**Important:** You must use the DDR interface for migrating upwards and downwards for the MPF050T/TL/TS/TLS device.


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# 5. Pin Descriptions (Ask a Question)

PolarFire device has user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

## 5.1. User I/O (Ask a Question)

PolarFire FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see PolarFire Family Memory Controller User Guide.

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1V and 1.8V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards, and operating supplies ranging from 1.2V to 3.3V. GPIO supports multiple standards, including 3.3V with an integrated Clock Data Recovery (CDR) to high-speed serial interfaces such as 1 GbE.

Each PolarFire FPGA user I/O uses a IOxyBz naming convention, where:

- IO: The type of I/O
- x: The I/O pair number in bank z
- y: P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/Os —P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- B: Bank (see note in Supported I/O Features)
- z: Bank number

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

### 5.1.1. Supported I/O Features (Ask a Question)

The following table lists the I/O features supported on HSIO and GPIO.

**Table 5-1.** Supported I/O Features

| I/O Feature | HSIO | GPIO | Additional Information |
|---|---|---|---|
| Programmable on/off clamp | — | Yes | — |
| Hot-plug | — | Yes | — |
| Cold sparing | Yes[1] | Yes | — |
| True differential output driver | — | Yes | — |
| Programmable on/off 100Ω differential termination | — | Yes | — |
| PVT-compensated output drive | Yes | Yes | — |
| Programmable slew control | — | Yes | — |
| PVT compensated slew control | Yes | — | — |
| Programmable input hysteresis | Yes | Yes | — |
| Mobile industry processor interface (MIPI) (input) | — | Yes | High-speed and low-power |
| MIPI (output) | — | Yes | High-speed |

**Important:**
1. HSIO is a pseudo-cold spare, that is, it requires the spare device to have its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes.


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## 5.2. Supply Pins (Ask a Question)

The following table lists multiple power supply pins required for proper device operation. For information about unused conditions and power sequence, see UG0726: PolarFire FPGA Board Design User Guide.

**Table 5-2.** Supply Pins

| Name | Description | Operating Voltage |
|---|---|---|
| XCVR_VREF[1] | Voltage reference for transceiver | 0.9V/1.25V |
| VDD_XCVR_CLK | Provides common power to all transceiver reference clock buffers | 2.5V/3.3V |
| VDDA25 | Transceiver PLL power | 2.5V |
| VDDA | Power for transceiver Tx and Rx lanes 0, 1, 2, and 3 | 1.0V/1.05V |
| VSS | Core digital ground | — |
| VDD | Device core digital supply | 1.0V/1.05V |
| VDDIx (JTAG Bank) | Supply for I/O circuits in a bank | 1.8V/2.5V/3.3V |
| VDDIx (GPIO Banks) | Supply for I/O circuits in a bank | 1.2V/1.5V/ 1.8V/2.5V/ 3.3V |
| VDDIx (HSIO Banks) | Supply for I/O circuits in a bank | 1.2V/1.5V/ 1.8V |
| VDD25 | Power for corner PLLs and PNVM | 2.5V |
| VDD18 | Power for programming and HSIO receiver. HSIO auxiliary power supply | 1.8V |
| VDDAUXx | Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5V or 3.3V and must be always equal to or higher than VDDIx of GPIO banks | Greater than or equal to VDDI |

**Important:**

1. SSTL25 (Stub Series Terminated Logic) I/O standard for 1.25V VREF, SSTL18 I/O standard for 0.9V, and HSUL18 I/O standard for 0.9V.

### 5.2.1. Packaging Decoupling Capacitors (Ask a Question)

PolarFire 0.8 mm and 1.0 mm pitch packages contain decoupling capacitors to support high-speed I/O operation.

Small, low-profile CSP packages (0.5 mm ball pitch, 16 mm × 16 mm and smaller) do not have package decoupling capacitors.

The following table lists the packaging decoupling capacitors contained in non-CSP packages.

**Table 5-3.** Packaging Decoupling Capacitors

| Power Supply | 0.8 mm Pitch | | 1 mm Pitch | |
|---|---|---|---|---|
| — | Number of Capacitors | Value | Caps available | Value |
| VDDI0 | — | — | 1 | 1 µF |
| VDDI1 | — | — | 1 | 1 µF |
| VDDI2 | — | — | 1 | 1 µF |
| VDDI4 | — | — | 1 | 1 µF |
| VDDI5 | — | — | 1 | 1 µF |
| VDDI6[1] | — | — | 1 | 1 µF |
| VDDI7[1] | — | — | 1 | 1 µF |
| VDD | — | — | 1 | 2.2 µF |
| VDD18 | — | — | 2 | 1 µF |


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**Table 5-3.** Packaging Decoupling Capacitors (continued)

| Power Supply | 0.8 mm Pitch | | 1 mm Pitch | |
|---|---|---|---|---|
| VDDA | 2 | 4.7 nF<br>1.0 nF | 4 | 4.7 nF<br>2.2 nF<br>1.5 nF<br>1.0 nF |

**Important:**

1. 0.8 mm pitch PolarFire packages do not support VDDI6 and VDDI7.

**Table 5-4.** Package De-Capacitor Part Number and ESR Values

| Capacitance Value | Part Numbers | Package | ESR (Ω) |
|---|---|---|---|
| 4.7 nF | GRM033R70J472KA01 | 0201 | 0.09724812 |
| 2.2 nF | GRM033R70J222KA01 | 0201 | 0.16111 |
| 1.5 nF | GRM033R70J152KA01 | 0201 | 0.194915396 |
| 1 nF | CGA1A2X7R1C102K030BA | 0201 | 0.2444 |
| 1 uF | LL185C70J105ME14K (GPIO) | 0306 | 0.005475757 |
| 1 uF | LL185C70G105ME01L (HSIO and HSIO_AUX) | 0306 | 0.005009904 |
| 2.2 uF | W2L14C225MAT1A | 0508 | 0.003964 |

## 5.3. Memory Interface (Ask a Question)

Valid locations for DDR memory interfaces are shown in PPATs, see www.microchip.com/en-us/products/fpgas-and-plds/fpgas/polarfire-fpgas/polarfire-mid-range-fpgas#packaging. By using the Libero SoC PolarFire configurator, all individual DDR interface pins are identified from the macro. For more information on the memory interface, see PolarFire Family Memory Controller User Guide.

The following table lists the reference receiver modes of I/O standards.

**Table 5-5.** Reference Receiver Modes

| I/O Standard | VDDIx | VREF | On-Die Termination (ODT) (in Ω) | Bank Type | Speed (Mbps) | Application |
|---|---|---|---|---|---|---|
| SSTL18 | 1.8V | 0.9V | 40/50/60/80/120/240 | GPIO, HSIO | 800<br>1066 | RLDRAM2 |
| SSTL15 | 1.5V | 0.75V | 40/50/60/80/120/240 | GPIO, HSIO | 1066<br>1333 | DDR3 |
| SSTL135 | 1.35V | 0.68V | 20/30/40/60/120 | HSIO | 1333 | DDR3L |
| HSTL15 | 1.5V | 0.75V | 40/50/60/80/120/240 | GPIO, HSIO | 900<br>1100 | QDRII+ |
| HSTL135 | 1.35V | 0.68V | 20/30/40/60/120 | HSIO | 1066 | RLDRAM3 |
| HSUL12 | 1.2V | 0.6V | 60/120/40 | HSIO | 1066<br>1333 | LPDDR3 |
| HSTL12 | 1.2V | 0.6V | 60/120/240 | HSIO | 1266 | QDRII+ |
| POD12 | 1.2V | 0.6V | 20/30/40/60/120 | HSIO | 1600 | DDR4 |

## 5.4. DDR Interface (Ask a Question)

The DDR subsystems are the hardened ASIC blocks for interfacing the LPDDR3, DDR3, and DDR4 memories. It supports 16-bit, 32-bit, and 64-bit data bus width modes with ECC support. DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC PolarFire software for the selected I/O standards. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information on DDR signals, see PolarFire Family Memory Controller User Guide


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## 5.5. Clocking Pins (Ask a Question)

CCC blocks, located at each corner of the PolarFire FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, CCC located in the northeast corner is labeled as CCC_NE. For more information on clocking pins, see PolarFire Family Clocking Resources User Guide. Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, 12 on the north side, and either 12 or 16 inputs on the south side, depending on the package.

The following table lists the clocking pin names and descriptions. See Table 5-2 for more information on CCC pin voltage.

**Table 5-6.** Clocking Pins[1]

| Name | Description | When Unused |
|---|---|---|
| CCC_NW_PLL0_OUT[0:1]<br>CCC_NW_PLL1_OUT[0:1]<br>CCC_NE_PLL0_OUT[0:1]<br>CCC_NE_PLL1_OUT[0:1]<br>CCC_SE_PLL0_OUT[0:1]<br>CCC_SE_PLL1_OUT[0:1]<br>CCC_SW_PLL0_OUT[0:1]<br>CCC_SW_PLL1_OUT[0:1] | Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of PolarFire® device to route the clocks to and from the PLLs and DLLs. | Do Not Connect (DNC) |
| CCC_SE_CLKIN_S_[8:15]<br>CCC_SW_CLKIN_S_[0:3]<br>CCC_SW_CLKIN_W_[0:3]<br>CCC_NW_CLKIN_W_[4:7]<br>CCC_NW_CLKIN_N_[0:3]<br>CCC_NE_CLKIN_N_[8:11] | Preferred clock inputs that connect external clock signals to CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs, and fabric logic. | DNC |
| CLKIN_S_[4:7]<br>CLKIN_N_[4:7] | Preferred clock inputs directly routed to internal global buffers through MUXes. | DNC |

**Important:**

1. Some of the preferred clock inputs have connections to feedback clock input of the PLL/DLL present in the CCC. It is required to choose a preferred clock input which has connection to the PLL reference clock input for clock frequency synthesis. See PolarFire Family Clocking Resources User Guide for preferred clock inputs connectivity to PLLs/DLLs and global clock network. For example, the package pin T9 of MPF300T-FCG1152 device has pin name as follows: GPIO219PB4, CLKIN_W_3, and CCC_SW_CLKIN_W_3. The T9 pin can be used as a preferred clock input which can connect to global clock network or CCC_SW. Inside the CCC_SW, the T9 pin is connected to feedback clock inputs of PLLs and reference clock inputs of DLLs.

## 5.6. Dedicated I/O Bank Pins (Ask a Question)

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/Os are, however, dynamically switched over to be used by the fabric when the PolarFire controller does not use them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the PolarFire controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and


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descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up. For information about unused conditions, see PolarFire FPGA Board Design User Guide.

The JTAG bank voltages can be set to operate at 1.8V, 2.5V, or 3.3V. The following table lists the JTAG pins.

**Table 5-7.** JTAG Pins

| Pin Names | Direction | Weak Pull-Up/Unused Condition | Description |
|---|---|---|---|
| TMS | Input | Yes/DNC | JTAG test mode select |
| TRSTB | Input | Yes | JTAG test reset<br>Must be held low during device operation |
| TDI | Input | Yes/DNC | JTAG test data in<br>In ATPG or test mode, when using a 4-bit tdi bus, this I/O is used as tdi[0] |
| TCK | Input | No | JTAG test clock |
| TDO | Output | No/DNC | JTAG test data out |

**Important:**

1. If TRSTB is unused and in the avionics mode, either an external 1 kΩ pull-down resistor must be connected to it, to override the weak internal pull-up or it must be driven low from the external source.
2. In unused condition, must be connected to VSS through 10 kΩ resistor.

**Table 5-8.** Device Reset Pins

| Name | Direction | Weak Pull-up | Description |
|---|---|---|---|
| DEVRST_N | Input | 22 KΩ | Device reset (asserted low) |

**Table 5-9.** SPI Interface Pins

| Name | Direction | Description |
|---|---|---|
| SCK | Bi-directional | SPI clock |
| SS | Bi-directional | SPI target select |
| SDI | Input | SDI input for the shared SPI interface |
| SDO | Output | SDO output for the shared SPI interface |
| SPI_EN | Input | Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O |
| IO_CFG_INTF | Input | Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a initiator or a target.<br>• 0: SPI target interface<br>• 1: SPI initiator interface |

**Table 5-10.** Special Pins

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| NC | — | No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device. | — |
| DNC | — | Do not connect pin. DNC pins must not be connected to any signals on PCB, and they must be left unconnected. | — |


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**Table 5-10.** Special Pins (continued)

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| LPRB_A | Output | Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following: • Live probe • User I/O (GPIO) | Libero-Defined DNC |
| LPRB_B | Output | | Libero-Defined DNC |
| FF_EXIT_N | Input | RESERVED | — |
| Shield Signal | Output | Shield signal is required for each group of DDR data byte signals. It must be routed with a thick trace to DDR RAM along with Data byte signal to provide grounding between DDR byte lanes. The Shield signal must be tied to ground at the FPGA and at the DDR RAM. **Note:** Each DDR_Byte signal has one shield pin (Ground signal) in PolarFire® FPGA, and it must be routed with a thick trace to SDRAM along with Data byte signal, so that it improves the Noise from other data signal. | Only when DDR controller is in use |

## 5.7. XCVR Interface (Ask a Question)

**Important:** PolarFire -CORE devices do not include transceiver functionality. Users must refer to the Unused Pin Recommendations provided in the Packaging Pin Assignment Table (PPAT) for information on transceiver-related pins and power supplies.

The transceiver I/O available in the PolarFire device is dedicated for high-speed serial communication protocols. Libero-Defined DNC pins are pulled up internally when not used in the Libero design.

The following table lists the XCVR interface pins.

**Table 5-11.** XCVR Interface Pins

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| XCVR_xy_REFCLK_P<br>XCVR_xy_REFCLK_N | Input | Differential serial reference clock<br>• xy: Location<br>• x: Transceiver number (0, 1, 2 and 3)<br>• y: Lane number (A, B and C) | DNC, Libero-Defined, add on-board connect to VSS through resistor (100 KΩ) for higher noise immunity, CLAMP = OFF |
| XCVR_x_TXy_P<br>XCVR_x_TXy_N | Output | Differential serial transmit pins<br>• x: Transceiver number (0, 1, 2 and 3)<br>• y: Lane number (0, 1, 2 and 3) | DNC, Libero-Defined |
| XCVR_x_RXy_P<br>XCVR_x_RXy_N | Input | Differential serial receive pins<br>• x: Transceiver number (0, 1, 2 and 3)<br>• y: Lane number (0, 1, 2 and 3) | DNC, Libero-Defined, add on-board connect to VSS through resistor (100 KΩ) for higher noise immunity, see PolarFire Family Transceiver User Guide |


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# 6. Package Pin-Outs (Ask a Question)

The following table lists packaging pin-outs of PolarFire device. Detailed PPATs are available for download and they contain revision history, device specification, power supplies, pin-outs, and BGA graphic. For more information about PPATs, see www.microchip.com/en-us/products/fpgas-and-plds/fpgas/polarfire-fpgas/polarfire-mid-range-fpgas#packaging.

**Table 6-1.** Package Pin-Outs

| Device | Packages | | | | | |
|---|---|---|---|---|---|---|
| | FCG1152 | FCG784 | FCG484 | FCVG484 | FCSG536 | FCSG325 |
| MPF500T | Yes | Yes | — | — | — | — |
| MPF300T | Yes | Yes | Yes | Yes | Yes | — |
| MPF200T | — | Yes | Yes | Yes | Yes | Yes |
| MPF100T | — | — | Yes | Yes | — | Yes |
| MPF050T | — | — | — | Yes | — | Yes |

## 6.1. Pin Compatibility Between Devices (Ask a Question)

The following table lists the pin compatible packages of PolarFire device.

**Table 6-2.** Pin Compatible Packages

| Package | Devices |
|---|---|
| FCG1152 | MPF500T/300T |
| FCG784 | MPF500T/300T/200T |
| FCG484 | MPF300T/200T/100T |
| FCVG484 | MPF300T/200T/100T/050T |
| FCSG536 | MPF300T/200T |
| FCSG325 | MPF200T/100T/050T |


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# 7. Mechanical Drawings (Ask a Question)

The following figures show the top, bottom, and side views and dimensions of PolarFire FPGAs.

**Figure 7-1.** MPF500TS-FC1152M Package Top-View and Side-View

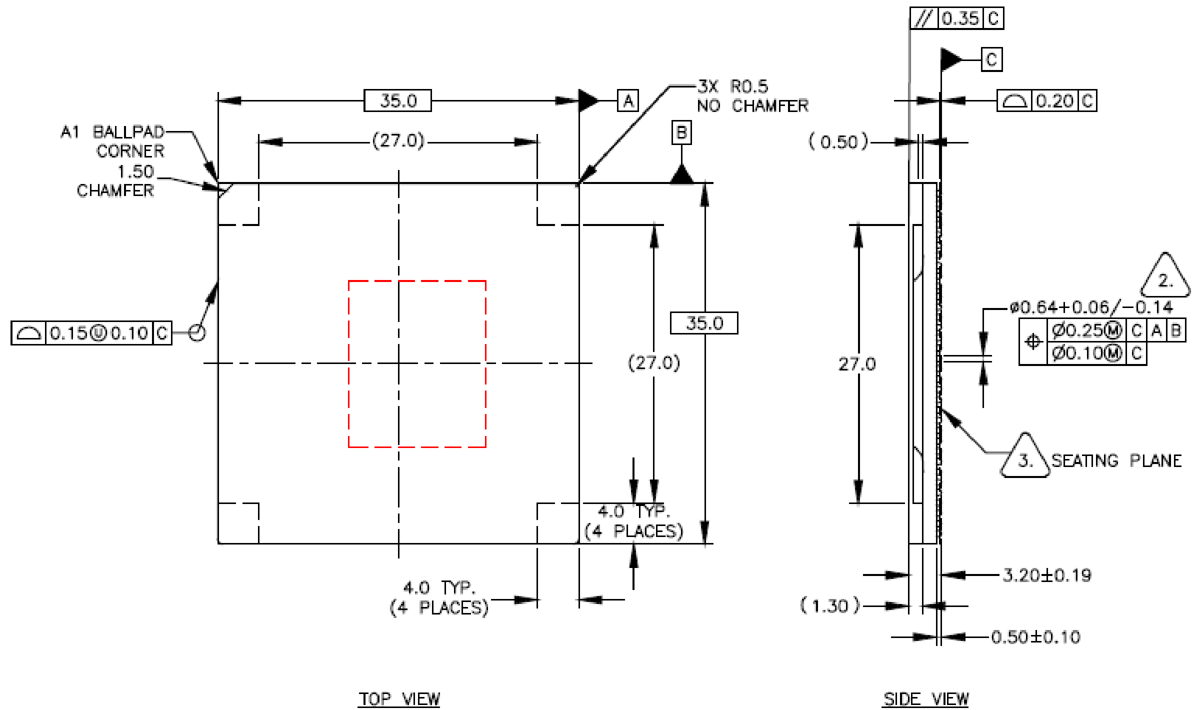



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**Figure 7-2.** MPF500TS-FC1152M Package Bottom-View

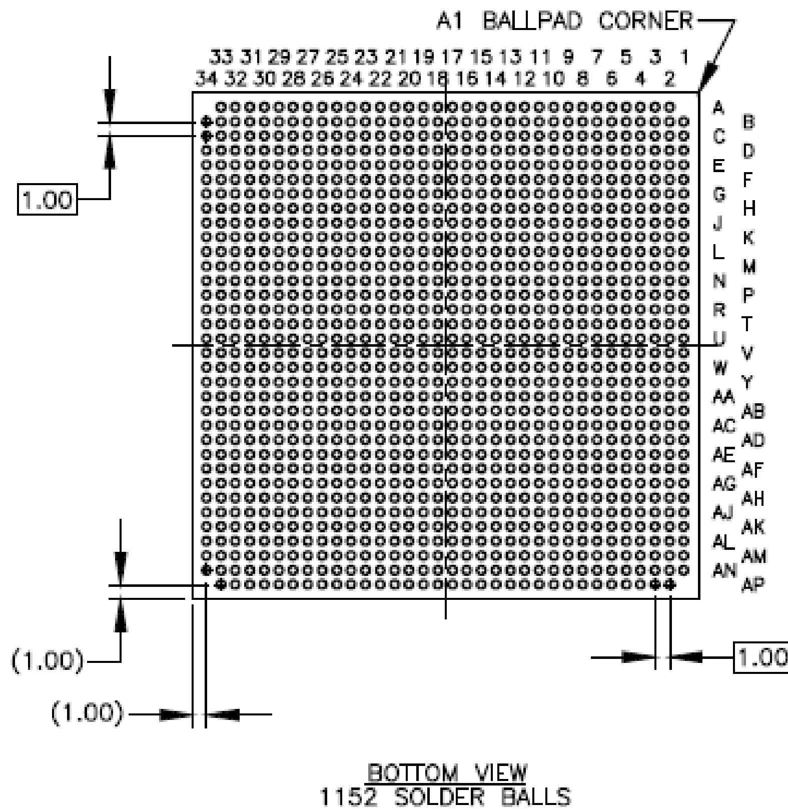


**Figure 7-3.** MPF500T/MPF300T-FCG1152 Package Top-View and Side-View

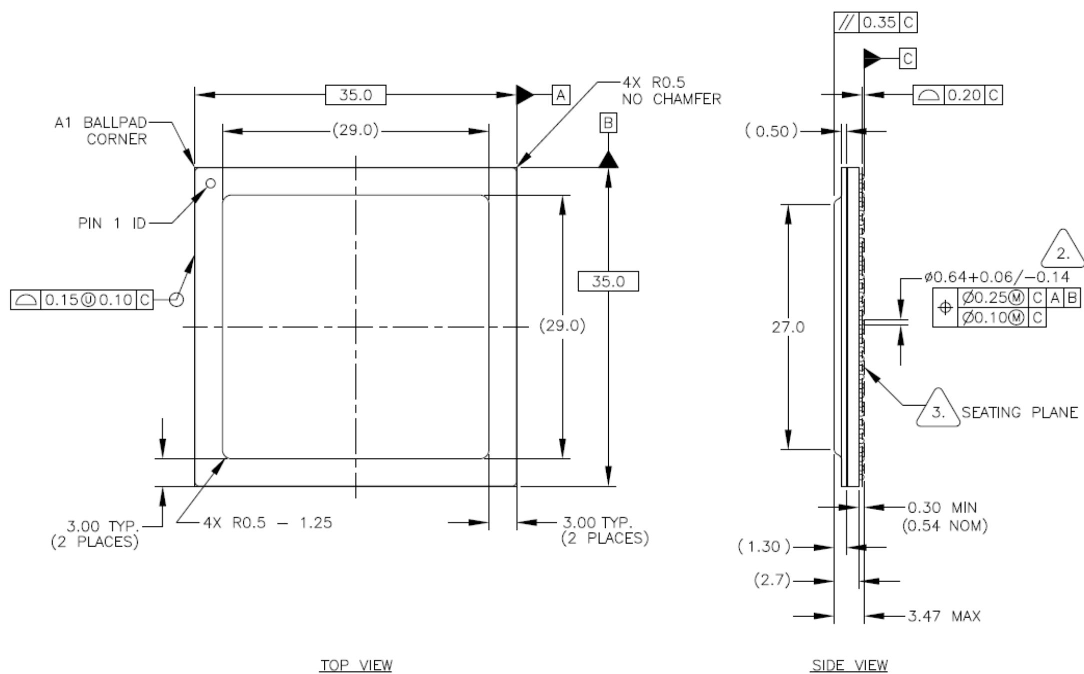



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**Figure 7-4.** MPF500T/MPF300T-FCG1152 Package Bottom-View

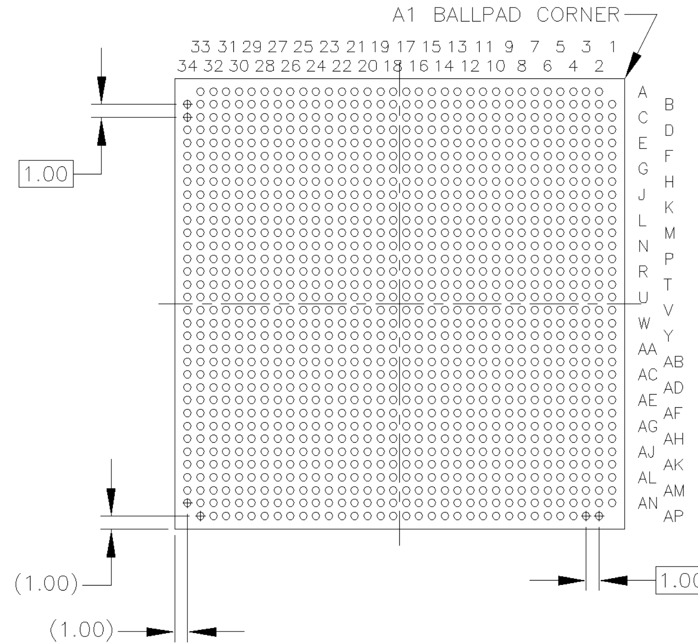


**Figure 7-5.** MPF500T/TS/MPF300T/TS/MPF200T-FCG784/FC784M Package Top-View and Side-View

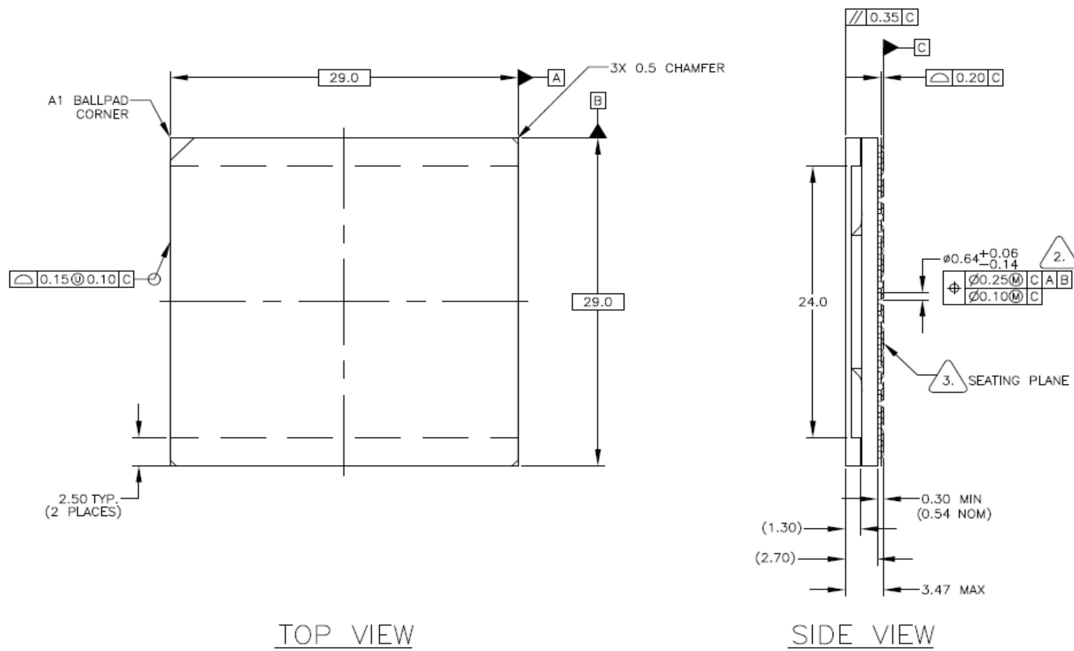



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**Figure 7-6.** MPF500T/TS/MPF300T/TS/MPF200T-FCG784M Package Bottom-View

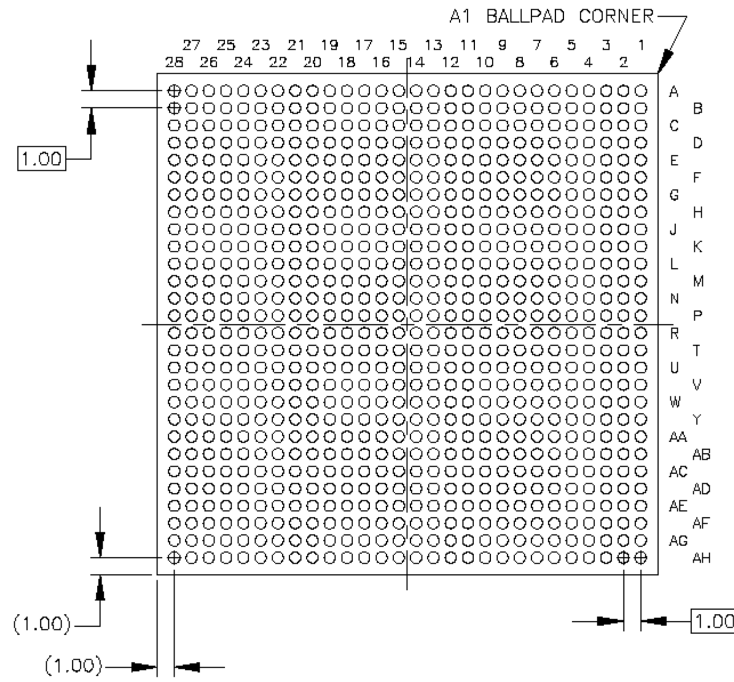


**Figure 7-7.** MPF300T-FCG784N Package Top-View and Side-View

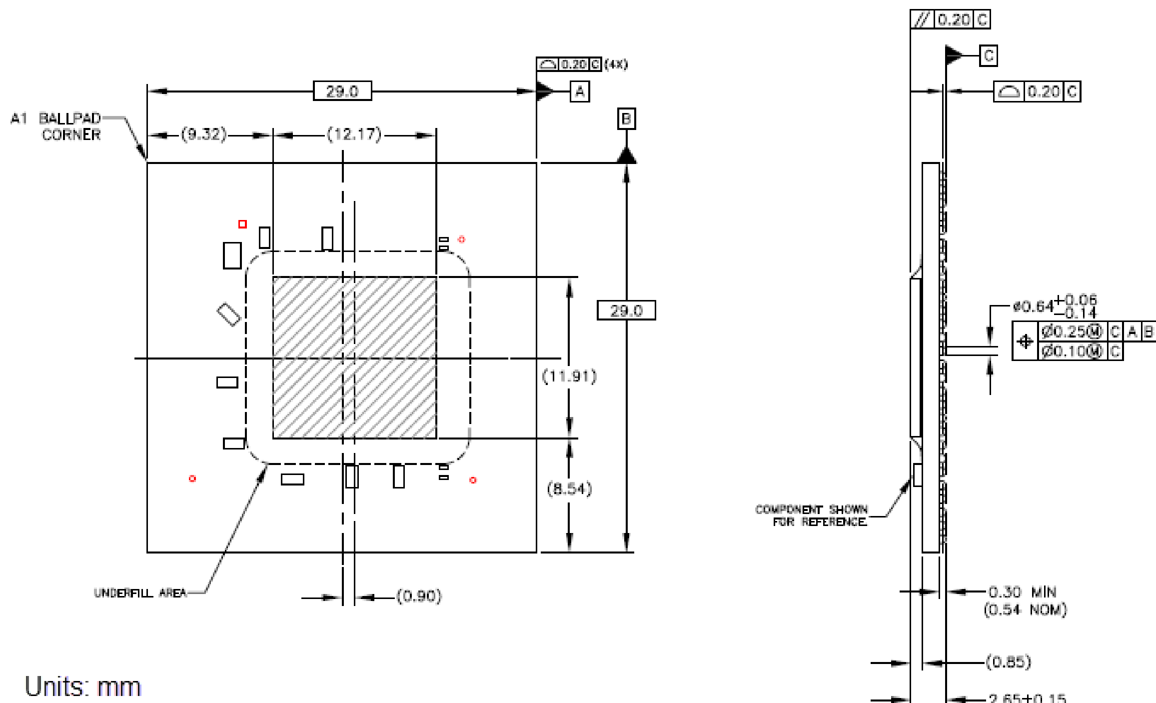



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**Figure 7-8.** MPF300T-FCG784N Package Bottom-View

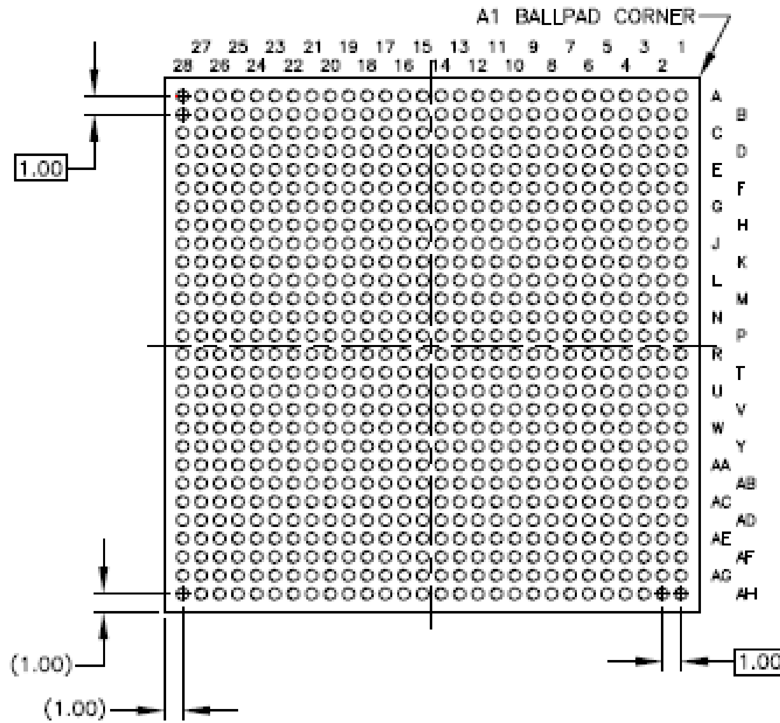


**Figure 7-9.** MPF300T-FCG784N Decoupling Capacitor Locations

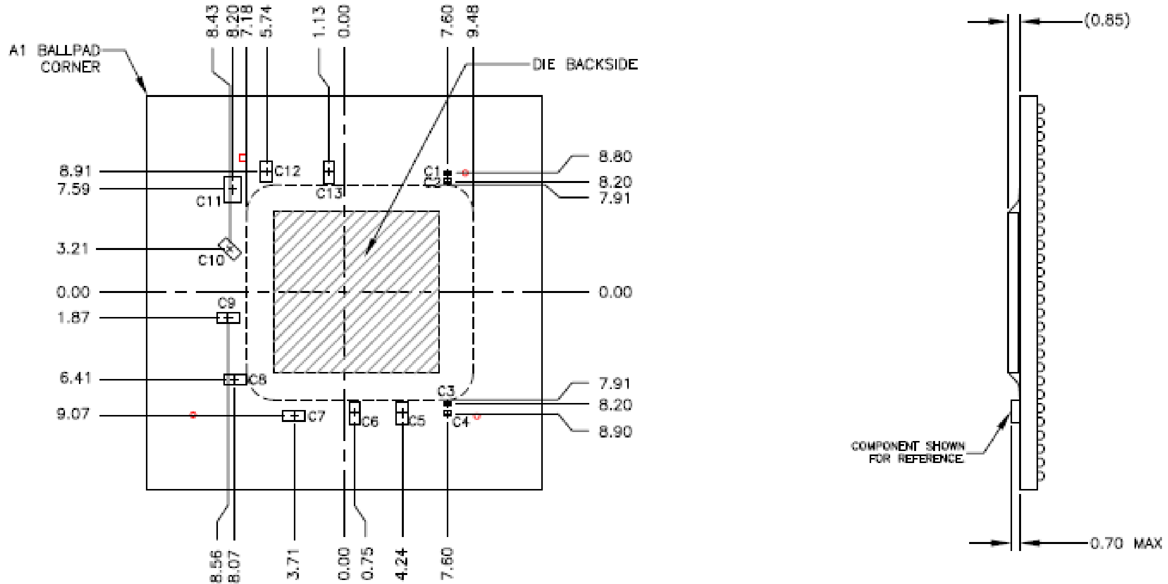



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**Figure 7-10.** MPF300T-FCG484 Package Top-View and Side-View

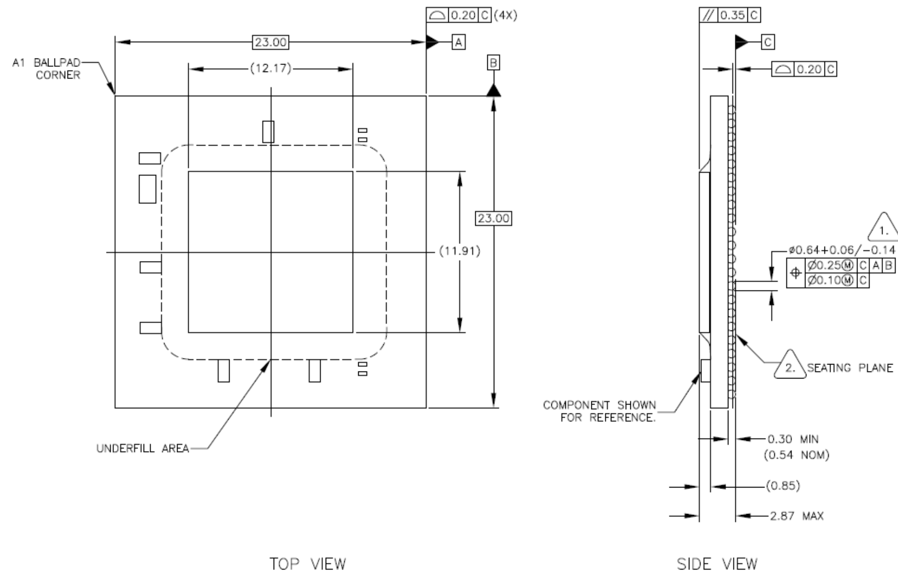


**Figure 7-11.** MPF300T-FCG484 Package Bottom-View

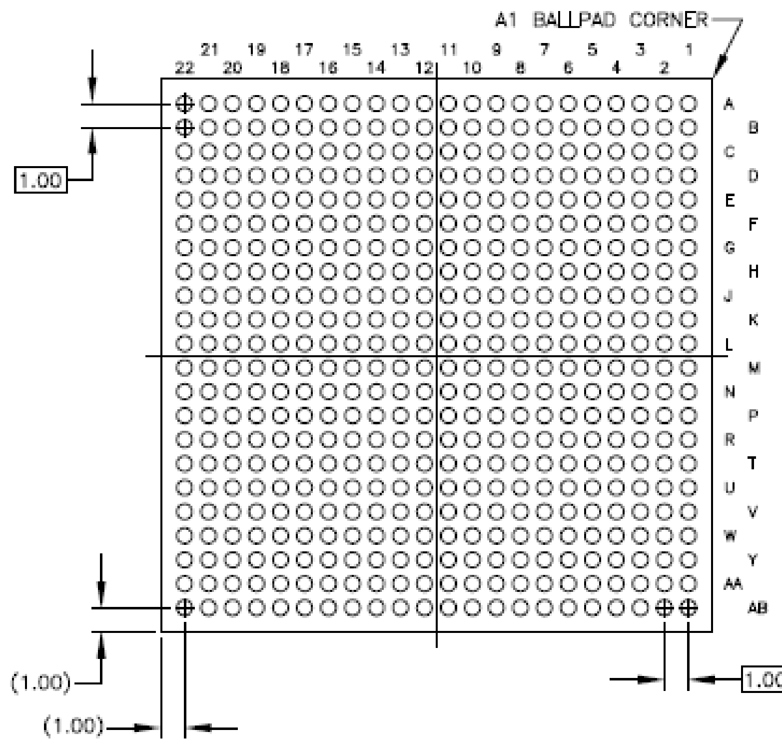



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**Figure 7-12.** MPF300T-FCG484-Decoupling Capacitor Locations

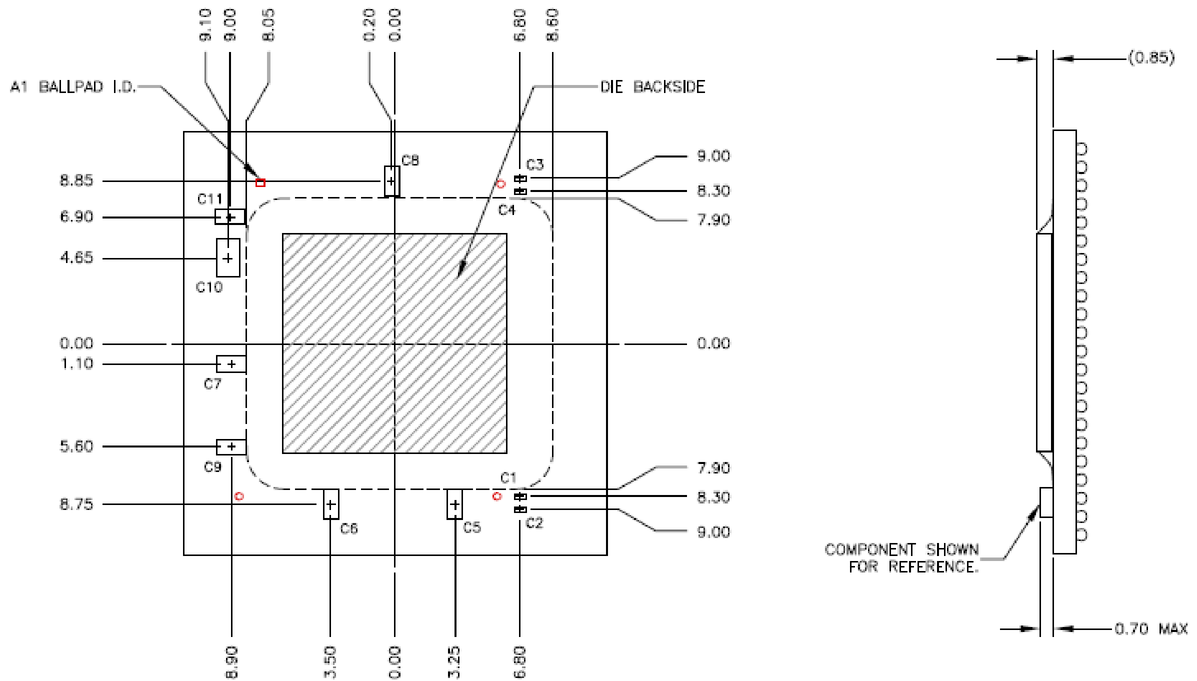


**Figure 7-13.** MPF300T/TS-FC484M, MPF100T/MPF200T-FCG484T2 Package Top-View and Side-View

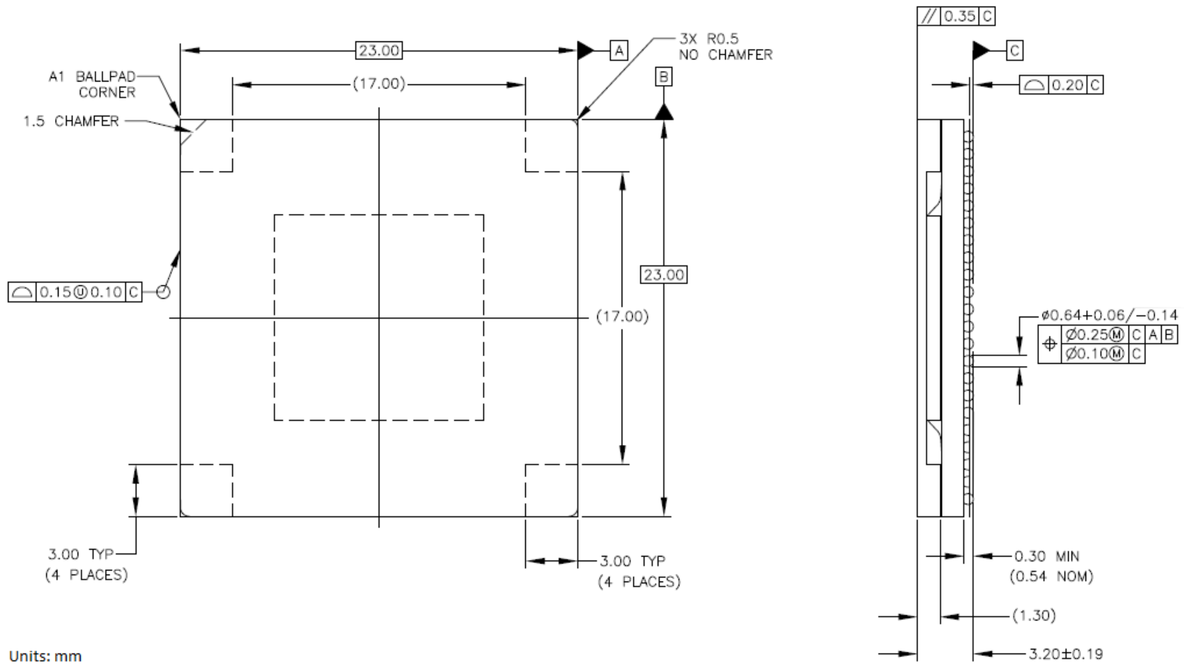



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**Figure 7-14.** MPF300T/TS-FC484M, MPF100T/MPF200T-FCG484T2 Package Bottom-View

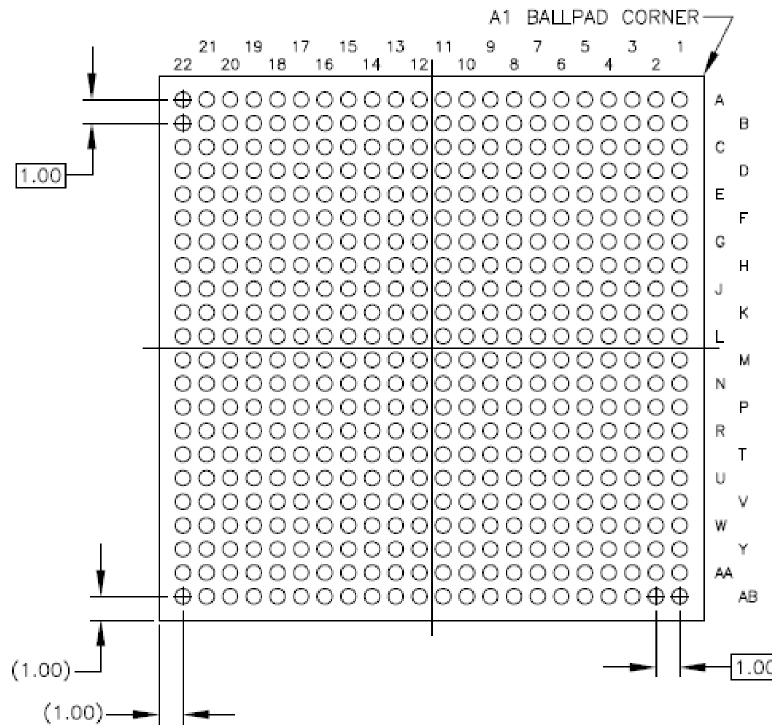
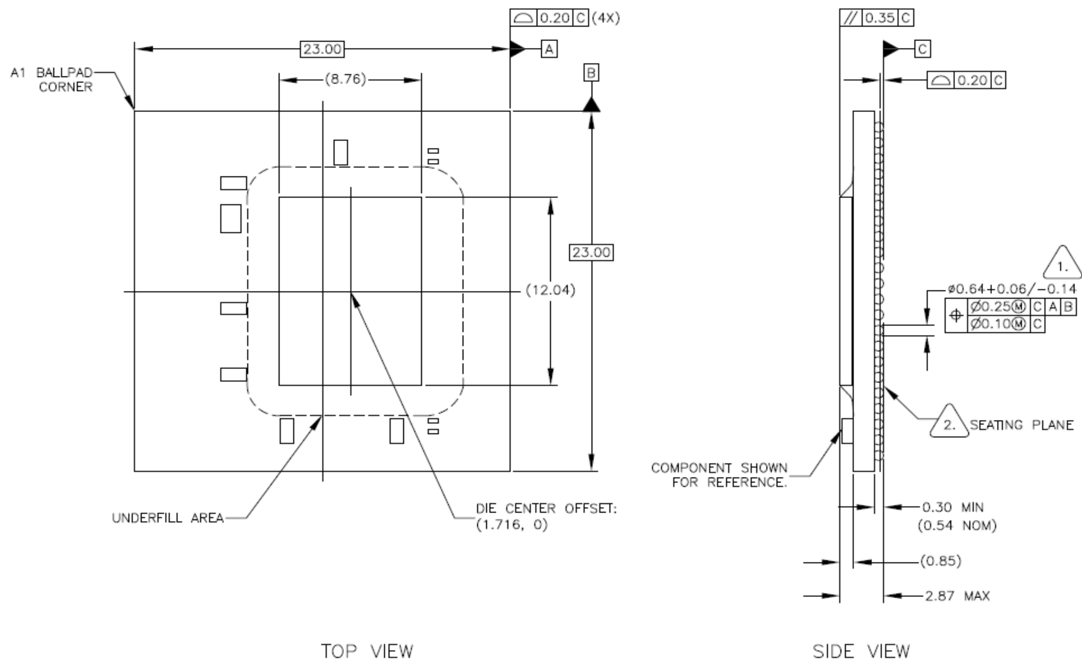



**Figure 7-15.** MPF200T-FCG484 Package Top-View and Side-View





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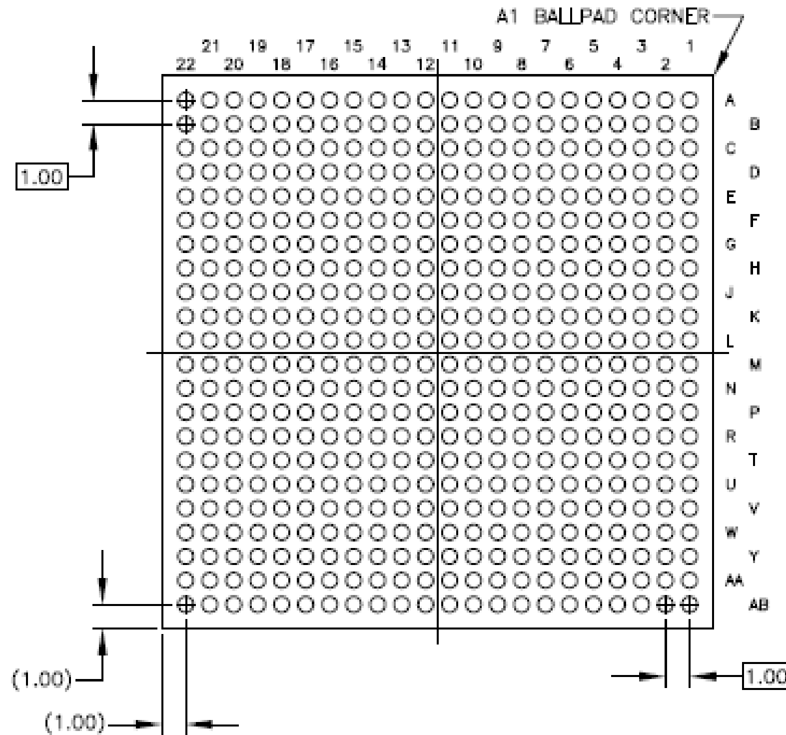


**Figure 7-16.** MPF200T-FCG484 Package Bottom-View

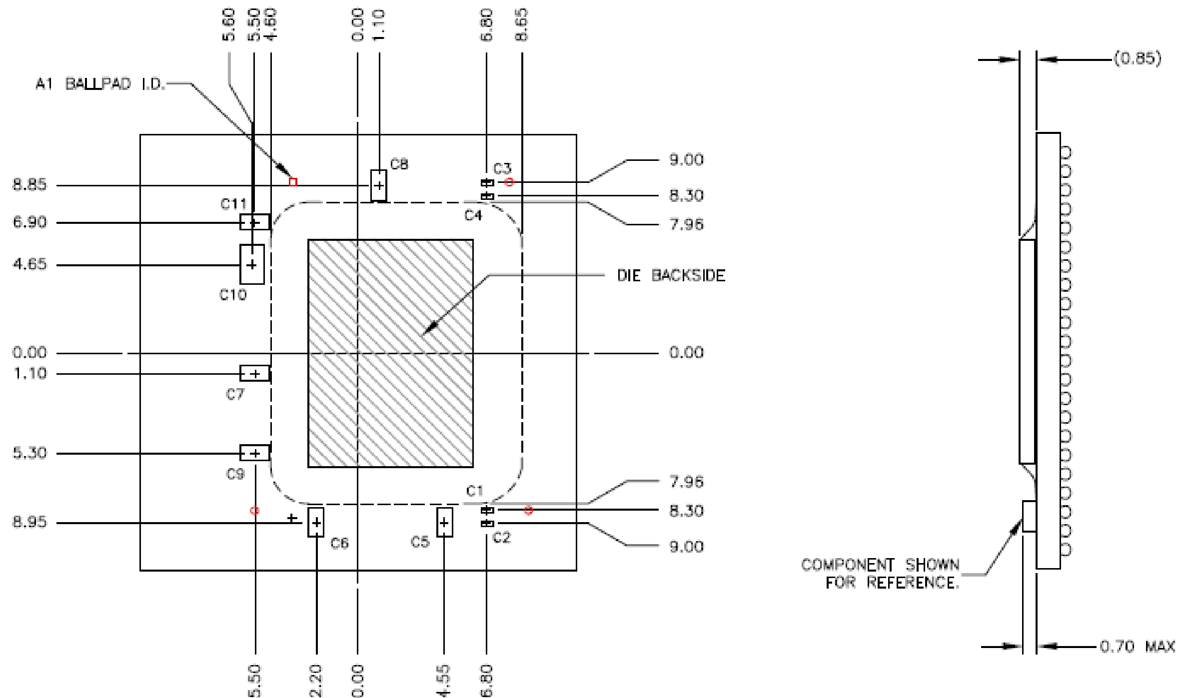


**Figure 7-17.** MPF200T-FCG484 Decoupling Capacitor Locations

**Note:** The ball pinout and spacing are the same on both the packages (that is, MPF100 and MPF200), which allow you to use one PCB footprint.


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**Figure 7-18.** MPF100T-FCG484 Package Top-View and Side-View

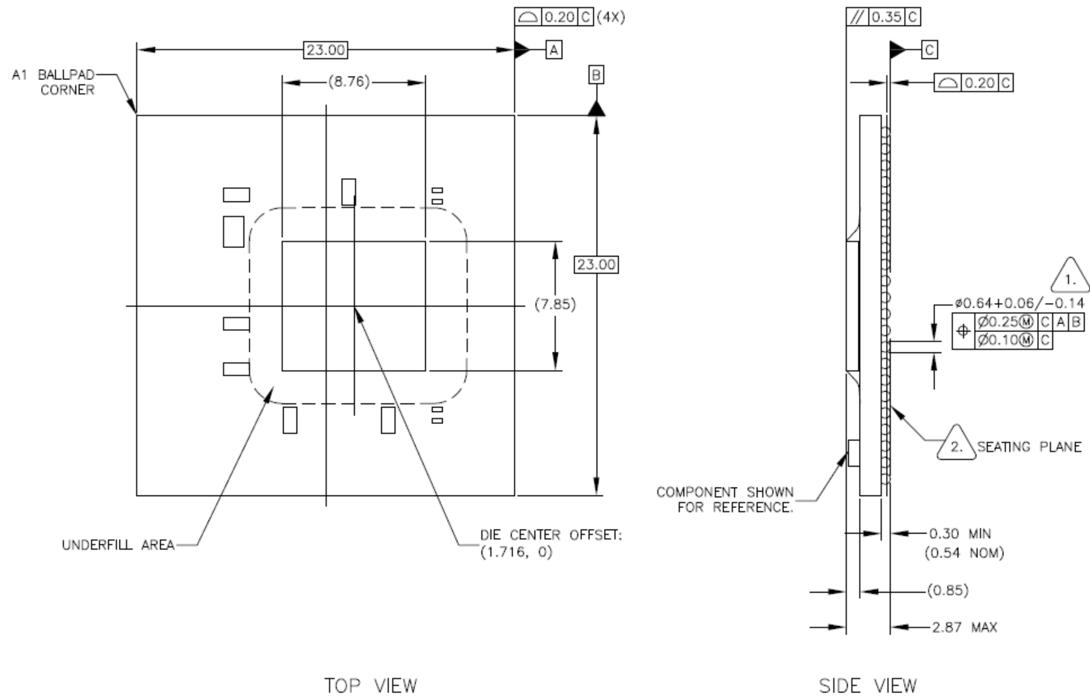


**Figure 7-19.** MPF100T-FCG484 Package Bottom-View

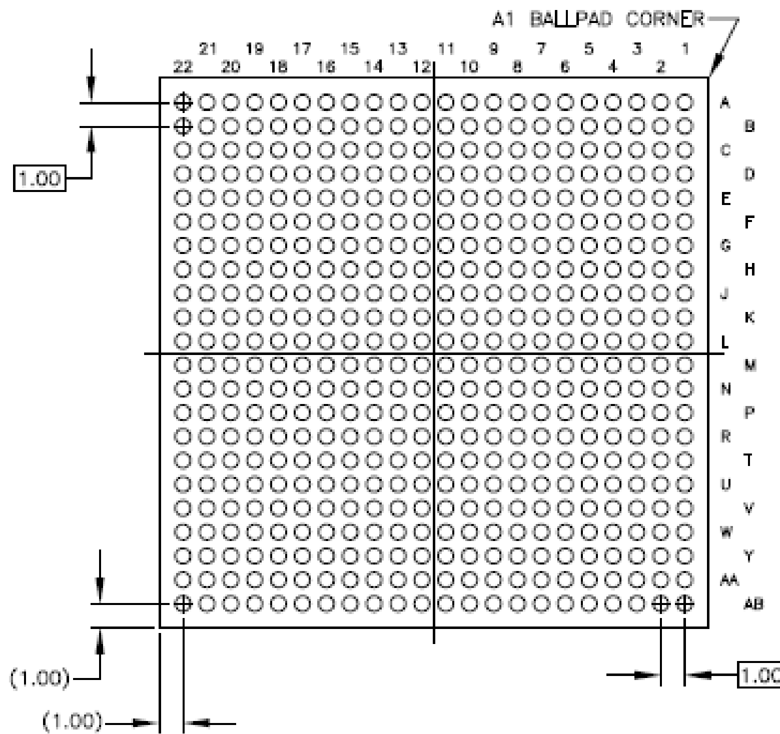



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**Figure 7-20.** MPF100T-FCG484 Decoupling Capacitor Locations

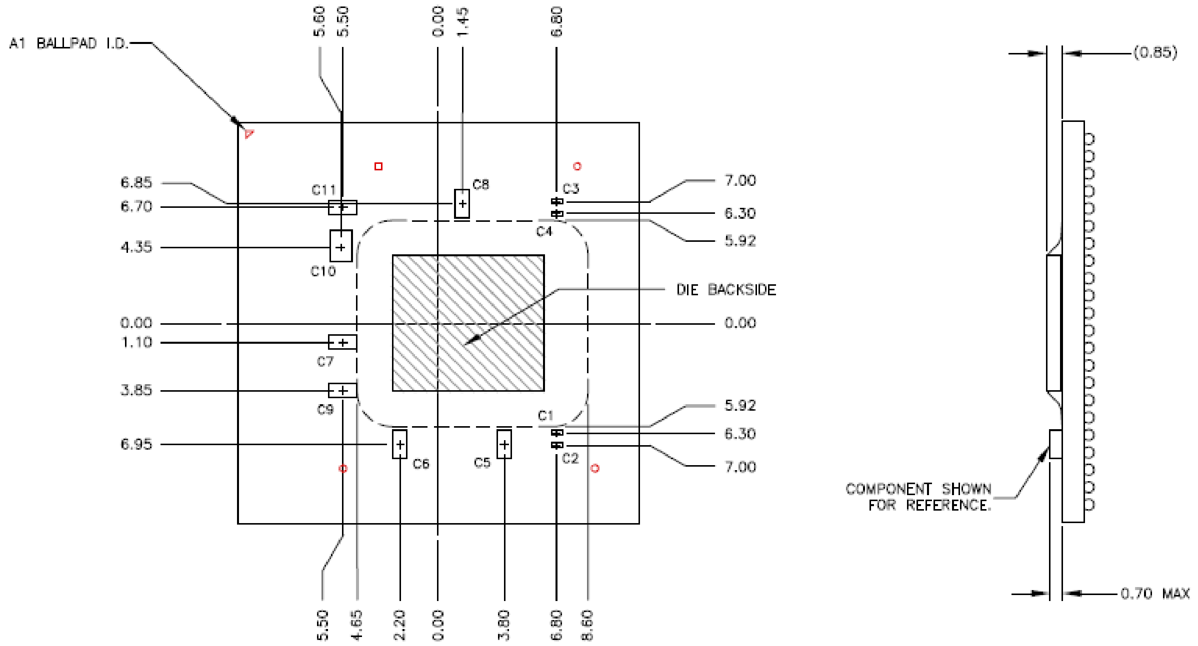


**Figure 7-21.** MPF300T/TS-FCV484M, MPF300T/MPF200T/MPF100T-FCVG484/FCVG484T2, MPF050T-FCVG484 Package Top-View and Side-View

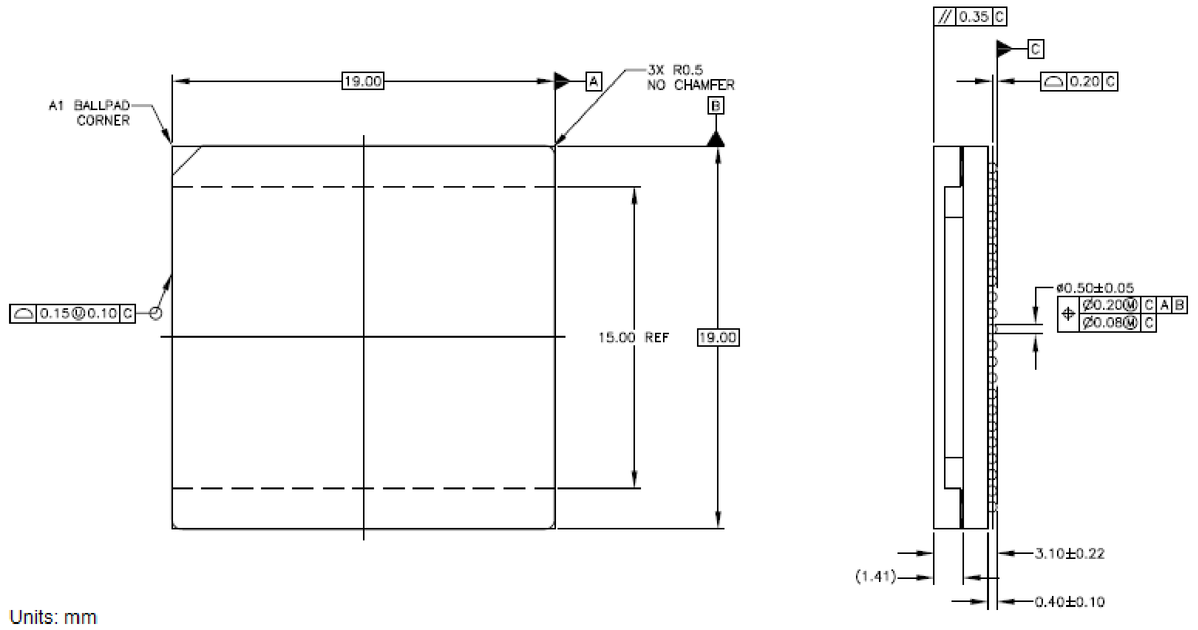



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**Figure 7-22.** MPF300T/TS-FCV484M, MPF300T/MPF200T/MPF100T-FCVG484/FCVG484T2, MPF050T-FCVG484 Package Bottom-View

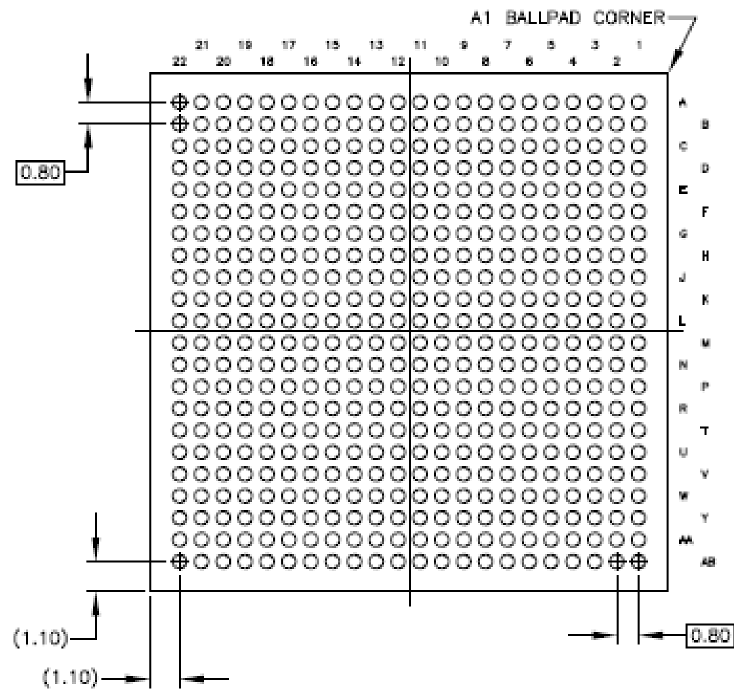


**Figure 7-23.** MPF300T/TS-FCS536M, MPF300T/MPF200T-FCSG536/FCSG536T2 Package Top-View and Side-View

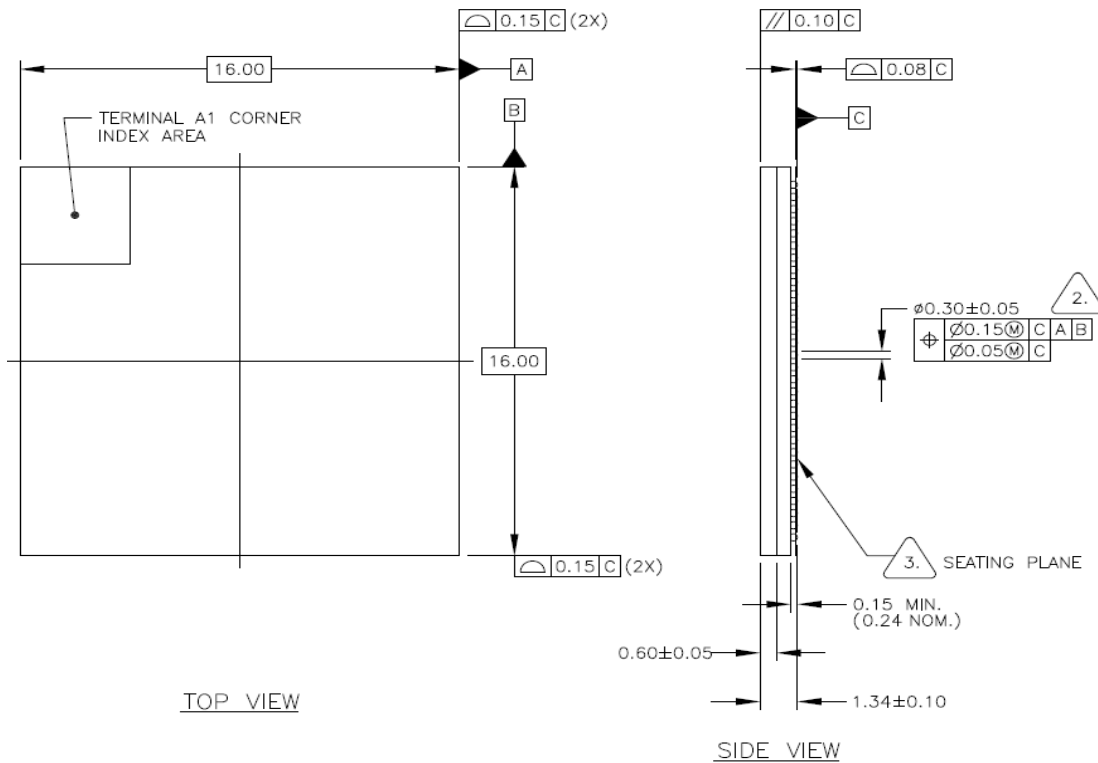



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**Figure 7-24.** MPF300T/TS-FCS536M, MPF300T/MPF200T-FCSG536/FCSG536T2 Package Bottom-View

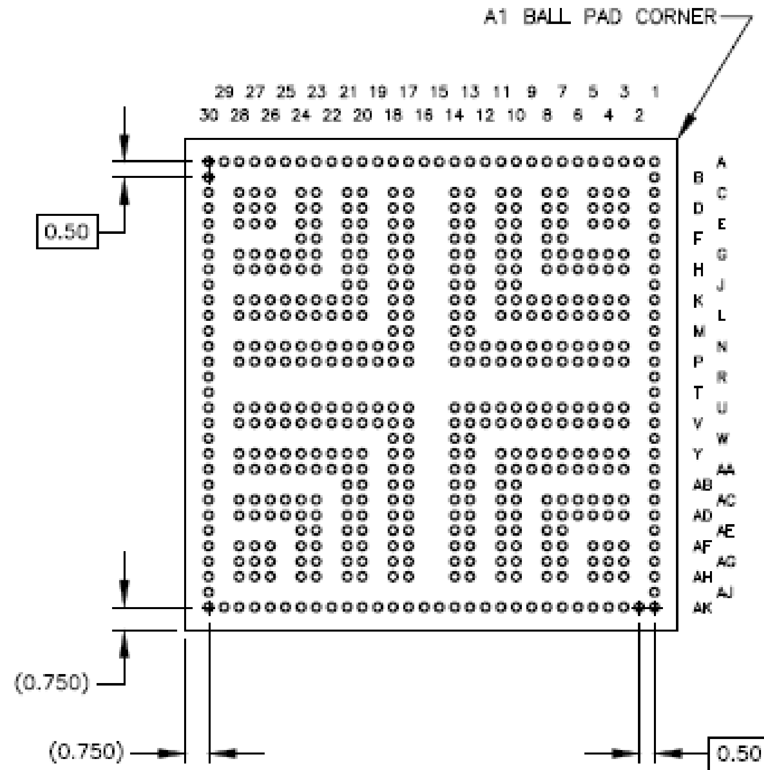



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**Figure 7-25.** MPF200T/TS-FCS325M, MPF200T-FCSG325/FCSG325T2 Package Top-View and Side-View

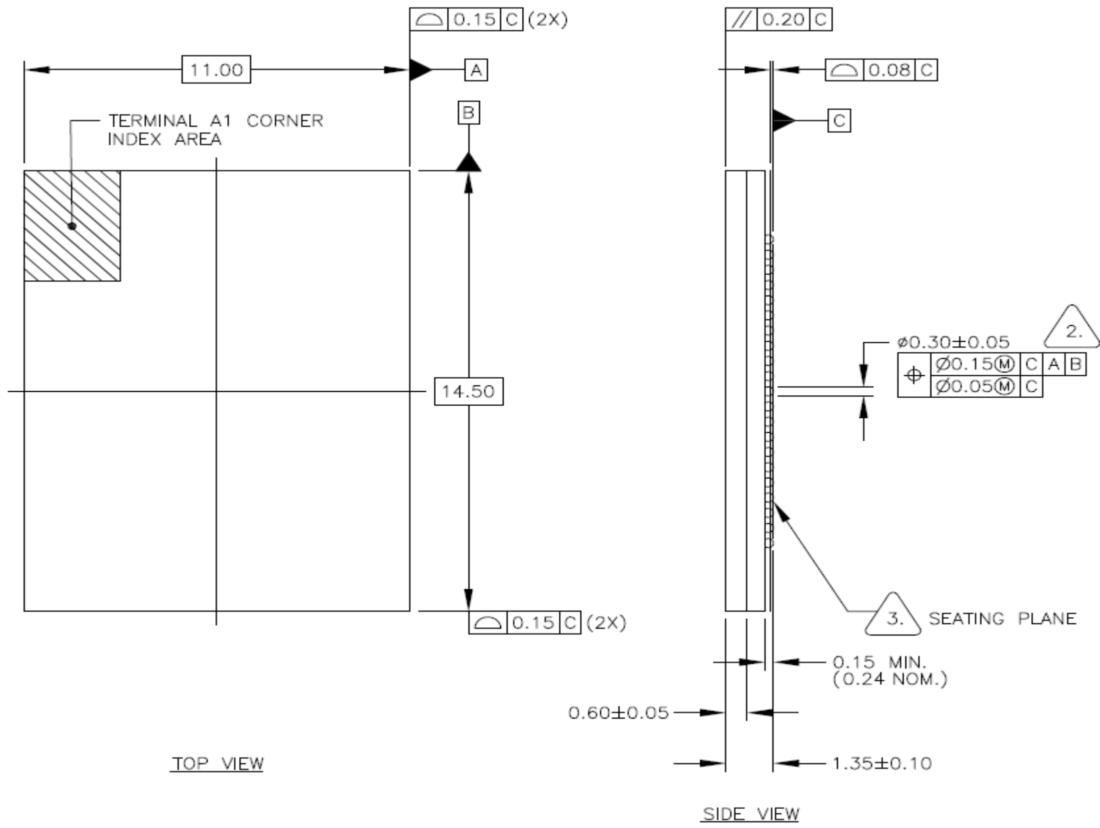



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**Figure 7-26.** MPF200T/TS-FCS325M, MPF200T-FCSG325/FCSG325T2 Package Bottom-View

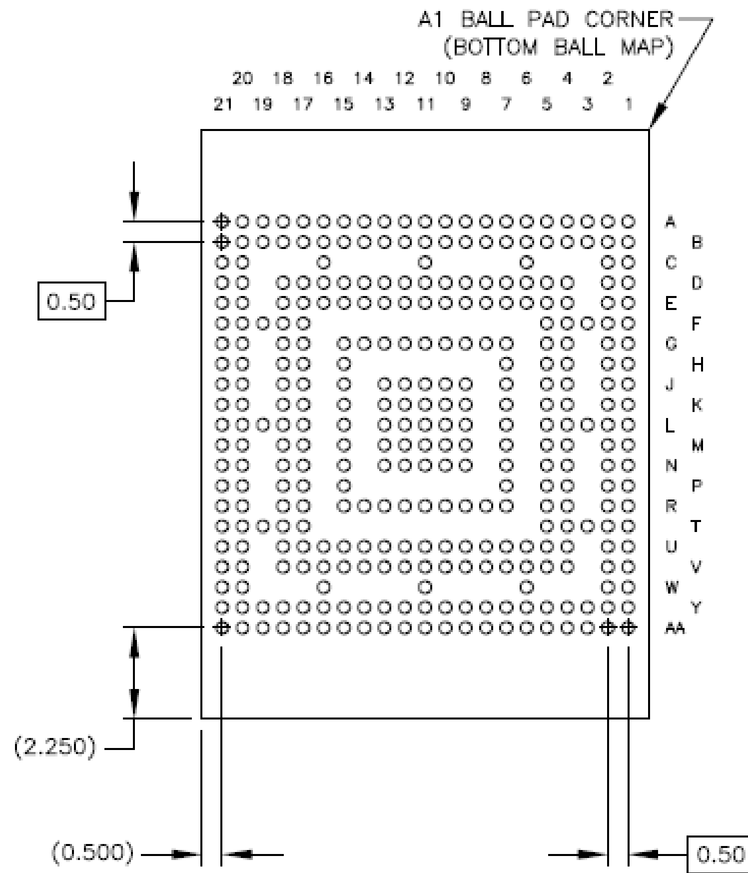



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**Figure 7-27.** MPF100T/MPF050T-FCSG325, MPF100T/MPF050T-FCSG325T2 Package Top-View and Side-View

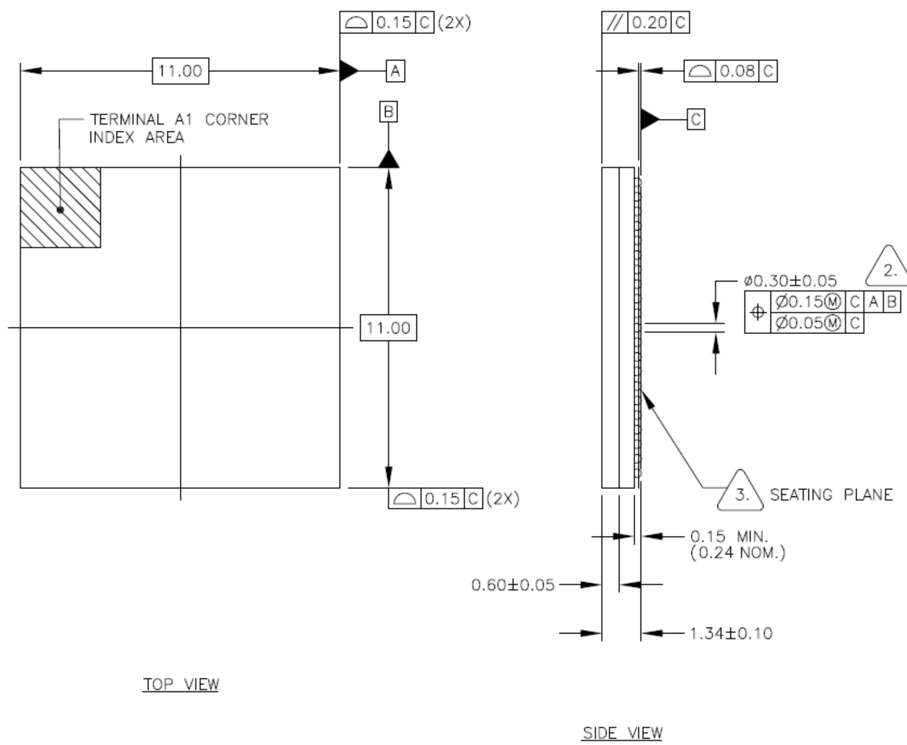



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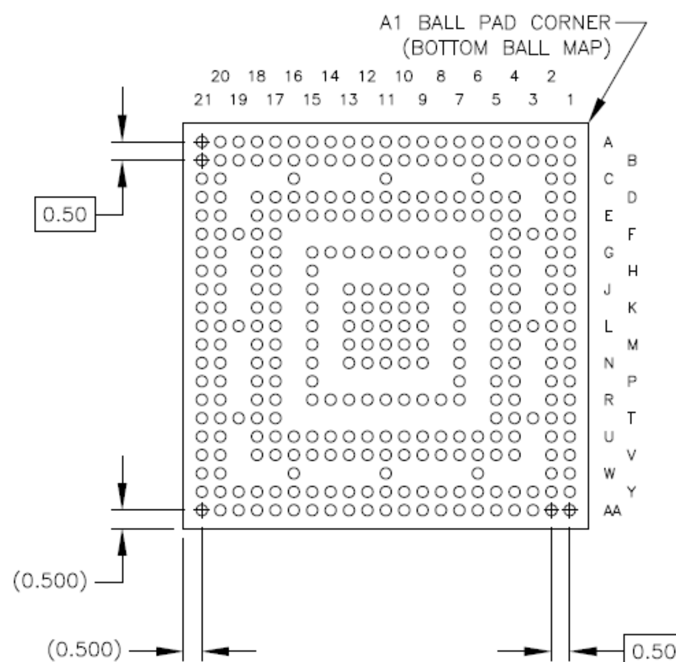
**Figure 7-28.** MPF100T/MPF050T-FCSG325, MPF100T/MPF050T-FCSG325T2 Package Bottom-View




The following table lists the PolarFire FPGAs package description and specifications.

**Table 7-1.** PolarFire FPGAs Package Information

| Package | Description | Package Specifications | | | |
|---|---|---|---|---|---|
| | | Package Type | Pitch (mm) | Size (mm) | Maximum I/Os |
| FCG1152 | Flip-Chip with lid | BGA | 1 | 35 × 35 | 512 |
| FCG784 | Flip-Chip with lid | BGA | 1 | 29 × 29 | 388 |
| FCG784N | Flip-Chip | BGA | 1 | 29 × 29 | 388 |
| FCG484 | Flip-Chip | BGA | 1 | 23 × 23 | 244 |
| FCVG484 | Flip-Chip with lid | BGA | 0.8 | 19 × 19 | 284 |
| FCSG536 | Flip-Chip (molded) | CSP | 0.5 | 16 × 16 | 300 |
| FCSG325 | Flip-Chip (molded) | CSP | 0.5 | 11 × 11, 11 × 14.5 | 170 |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# 8. Package Material Information (Ask a Question)

The following table lists the PolarFire ball grid array RoHS packages.

**Table 8-1.** PolarFire RoHS Packages

| Package Balls | FCG1152 | FCG784/ FCG784N | FCG484 | FCVG484 | FCSG536 | FCSG325 |
|---|---|---|---|---|---|---|
| Package Pitch | 1 mm | 1 mm | 1 mm | 0.8 mm | 0.5 mm | 0.5 mm |
| Substrate Material | Epoxy Glass | Epoxy Glass | Epoxy Glass | Epoxy Glass | BT Resin | BT Resin |
| Solder Ball Composition RoHS | SAC305 | SAC305 | SAC305 | SAC305 | SAC305 | SAC105 |
| Wafer Bump Material | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 | Cu Pillar + Solder Cap | Cu Pillar + Solder Cap |

The following table lists the PolarFire ball grid array mil temp packages.

**Table 8-2.** PolarFire Mil Temp Packages

| Package Balls | FC1152M | FC784M | FC484M | FCV484M | FCS536M | FCS325M |
|---|---|---|---|---|---|---|
| Package Pitch | 1 mm | 1 mm | 1 mm | 0.8 mm | 0.5 mm | 0.5 mm |
| Substrate Material | Epoxy Glass | Epoxy Glass | Epoxy Glass | Epoxy Glass | BT Resin | BT Resin |
| Solder Ball Composition RoHS | Sn63/Pb37 | Sn63/Pb37 | Sn63/Pb37 | Sn63/Pb37 | Sn63/Pb37 | Sn63/Pb37 |
| Wafer Bump Material | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 | Cu Pillar + Solder Cap | Cu Pillar + Solder Cap |

All FCBGA packages—FCG1152, FCG784, and FCVG484—are vented. FCG484 is a bare die package.

The following table lists the PolarFire ball grid array for RoHS and Leaded packages.

**Table 8-3.** PolarFire Ball Grid Array for RoHS and Leaded Packages

| Flip-Chip Packages | Ball Pad Diameter (mm) | Ball Pad Opening (mm) | Vent Dimension (mm) | Vented Package |
|---|---|---|---|---|
| MPF500T - FCG1152 (with heat spreader) | 0.60 | 0.50 | 1.0 ± 0.25 | Yes (Vent hole diameter at Pin1 location) |
| MPF500T - FC1152M (with heat spreader) | 0.60 | 0.50 | 1.0 ± 0.25 | Yes (north, south, east, and west) |
| MPF300T - FCG1152 (with heat spreader) | 0.60 | 0.50 | 1.0 ± 0.25 | Yes (Vent hole diameter at Pin1 location) |
| MPF500T - FCG784 (with heat spreader) | 0.60 | 0.50 | 24 × 0.9 | Yes (east and west side) |
| MPF500T - FC784M (with heat spreader) | 0.60 | 0.50 | 24 × 0.9 | Yes (east and west side) |
| MPF300T - FCG784 (with heat spreader) | 0.60 | 0.50 | 24 × 0.9 | Yes (east and west side) |
| MPF300T-FCG784N Bare Die | 0.60 | 0.50 | — | Bare Die |
| MPF200T - FCG784 (with heat spreader) | 0.60 | 0.50 | 24 × 0.9 | Yes (east and west side) |
| MPF300T - FCG484 (Bare Die) | 0.60 | 0.50 | — | Bare Die |
| MPF300T - FC484M (with heat spreader) | 0.60 | 0.50 | 17 × 0.9 | Yes (north, south, east, and west) |


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**Table 8-3.** PolarFire Ball Grid Array for RoHS and Leaded Packages (continued)

| Flip-Chip Packages | Ball Pad Diameter (mm) | Ball Pad Opening (mm) | Vent Dimension (mm) | Vented Package |
|---|---|---|---|---|
| MPF300T - FCV484M (with heat spreader) | 0.50 | 0.40 | 15 × 0.9 | Yes (east and west side) |
| MPF200T - FCG484 (Bare Die) | 0.60 | 0.50 | — | Bare Die |
| MPF100T - FCG484 (Bare Die) | 0.60 | 0.50 | — | Bare Die |
| MPF300T - FCVG484 (with heat spreader) | 0.50 | 0.40 | 15 × 0.9 | Yes (east and west side) |
| MPF200T - FCVG484 (with heat spreader) | 0.50 | 0.40 | 15 × 0.9 | Yes (east and west side) |
| MPF100T - FCVG484 (with heat spreader) | 0.50 | 0.40 | 15 × 0.9 | Yes (east and west side) |
| MPF300T - FCSG536 Over-mold | 0.35 | 0.275 | — | No (molded) |
| MPF300T - FCS536M Over-mold | 0.35 | 0.275 | — | No (molded) |
| MPF200T - FCSG325 Over-mold | 0.35 | 0.275 | — | No (molded) |


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# 9. Thermal Specifications (Ask a Question)

The following table lists the thermal resistances of PolarFire FPGA package device.

**Table 9-1.** PolarFire Package Thermal Resistance

| Package | Environment | Theta-JA | Psi-JB | Psi-JT | Theta-JB | Theta-JC | Unit |
|---|---|---|---|---|---|---|---|
| MPF500T-FCG1152/MPF500T-FC1152M | Still Air | 7.75 | 1.71 | 0.182 | 1.87 | 0.293 | C/W |
| | 1.0 m/s | 5.80 | 2.68 | 0.184 | | | |
| | 2.5 m/s | 4.98 | 2.56 | 0.187 | | | |
| MPF300T-FCG1152 | Still Air | 8.00 | 1.95 | 0.290 | 2.09 | 0.429 | C/W |
| | 1.0 m/s | 6.03 | 2.91 | 0.288 | | | |
| | 2.5 m/s | 5.20 | 2.79 | 0.290 | | | |
| MPF500T-FCG784/MPF500T-FC784M | Still Air | 9.31 | 2.23 | 0.080 | 2.72 | 0.198 | C/W |
| | 1.0 m/s | 7.18 | 2.23 | 0.095 | | | |
| | 2.5 m/s | 6.34 | 2.17 | 0.100 | | | |
| MPF300T-FCG784/MPF300T-FC784M | Still Air | 9.50 | 2.46 | 0.114 | 2.94 | 0.253 | C/W |
| | 1.0 m/s | 7.35 | 2.43 | 0.125 | | | |
| | 2.5 m/s | 6.51 | 2.37 | 0.132 | | | |
| MPF300T-FCG784N (bare die) | Still Air | 11.21 | 3.36 | 0.009 | 3.52 | 0.045 | C/W |
| | 1.0 m/s | 9.22 | 3.54 | 0.011 | | | |
| | 2.5 m/s | 8.51 | 3.59 | 0.011 | | | |
| MPF200T-FCG784 | Still Air | 9.68 | 2.65 | 0.155 | 3.10 | 0.345 | C/W |
| | 1.0 m/s | 7.50 | 2.57 | 0.171 | | | |
| | 2.5 m/s | 6.65 | 2.51 | 0.180 | | | |
| MPF300T-FC484M | Still Air | 11.74 | 3.68 | 0.170 | 4.69 | 0.475 | C/W |
| | 1.0 m/s | 8.92 | 4.85 | 0.191 | | | |
| | 2.5 m/s | 7.55 | 4.43 | 0.206 | | | |
| MPF200T-FCG484T2 | Still Air | 11.95 | 3.92 | 0.229 | 4.98 | 0.619 | C/W |
| | 1.0 m/s | 9.13 | 5.05 | 0.250 | | | |
| | 2.5 m/s | 7.70 | 4.59 | 0.271 | | | |
| MPF100T-FCG484T2 | Still Air | 12.36 | 4.35 | 0.384 | 5.48 | 0.958 | C/W |
| | 1.0 m/s | 0.42 | 1.39 | 9.593 | | | |
| | 2.5 m/s | 0.45 | 1.24 | 8.055 | | | |
| MPF300T-FCG484 (bare die) | Still Air | 12.40 | 4.15 | 0.010 | 5.08 | 0.046 | C/W |
| | 1.0 m/s | 9.88 | 5.64 | 0.015 | | | |
| | 2.5 m/s | 8.69 | 5.32 | 0.016 | | | |
| MPF200T-FCG484 (bare die) | Still Air | 12.80 | 4.57 | 0.013 | 5.56 | 0.622 | C/W |
| | 1.0 m/s | 10.29 | 6.04 | 0.018 | | | |
| | 2.5 m/s | 9.11 | 5.73 | 0.019 | | | |
| MPF100T-FCG484 (bare die) | Still Air | 13.52 | 5.30 | 0.020 | 6.37 | 0.979 | C/W |
| | 1.0 m/s | 11.02 | 6.76 | 0.022 | | | |
| | 2.5 m/s | 9.85 | 6.45 | 0.023 | | | |
| MPF300T-FCVG484/MPF300T-FCV484M | Still Air | 12.10 | 2.71 | 0.036 | 4.51 | 0.220 | C/W |
| | 1.0 m/s | 11.07 | 3.95 | 0.109 | | | |
| | 2.5 m/s | 9.85 | 3.80 | 0.116 | | | |


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**Table 9-1.** PolarFire Package Thermal Resistance (continued)

| Package | Environment | Theta-JA | Psi-JB | Psi-JT | Theta-JB | Theta-JC | Unit |
|---|---|---|---|---|---|---|---|
| MPF200T-FCVG484 | Still Air | 12.13 | 2.73 | 0.048 | 4.75 | 0.255 | C/W |
| | 1.0 m/s | 11.27 | 4.17 | 0.157 | | | |
| | 2.5 m/s | 10.04 | 4.01 | 0.166 | | | |
| MPF100T-FCVG484 | Still Air | 12.18 | 2.79 | 0.074 | 5.01 | 0.390 | C/W |
| | 1.0 m/s | 11.55 | 4.44 | 0.264 | | | |
| | 2.5 m/s | 10.32 | 4.28 | 0.274 | | | |
| MPF050T-FCVG484 | Still Air | 12.34 | 2.91 | 0.138 | 3.18 | 0.536 | C/W |
| | 1.0 m/s | 11.96 | 4.88 | 0.467 | | | |
| | 2.5 m/s | 10.73 | 4.72 | 0.484 | | | |
| MPF300T-FCSG536/MPF300T-FCS536M | Still Air | 14.17 | 3.57 | 0.053 | 3.46 | 1.749 | C/W |
| | 1.0 m/s | 11.49 | 6.73 | 0.112 | | | |
| | 2.5 m/s | 10.40 | 6.47 | 0.158 | | | |
| MPF200T-FCSG536 | Still Air | 14.90 | 4.10 | 0.058 | 4.44 | 2.123 | C/W |
| | 1.0 m/s | 12.32 | 7.52 | 0.118 | | | |
| | 2.5 m/s | 11.19 | 7.23 | 0.186 | | | |
| MPF200T-FCSG325/MPF200T-FCS325M (11 X 14.5) | Still Air | 20.57 | 6.72 | 0.066 | 6.16 | 2.538 | C/W |
| | 1.0 m/s | 17.31 | 11.75 | 0.166 | | | |
| | 2.5 m/s | 15.64 | 11.20 | 0.267 | | | |
| MPF100T-FCSG325 (11 X 11) | Still Air | 21.18 | 5.83 | 0.074 | 6.87 | 3.570 | C/W |
| | 1.0 m/s | 17.78 | 11.93 | 0.173 | | | |
| | 2.5 m/s | 16.28 | 11.51 | 0.285 | | | |
| MPF050T-FCSG325 | Still Air | 21.28 | 6.83 | 0.099 | 7.71 | 4.602 | C/W |
| | 1.0 m/s | 18.50 | 12.82 | 0.203 | | | |
| | 2.5 m/s | 17.13 | 12.41 | 0.322 | | | |


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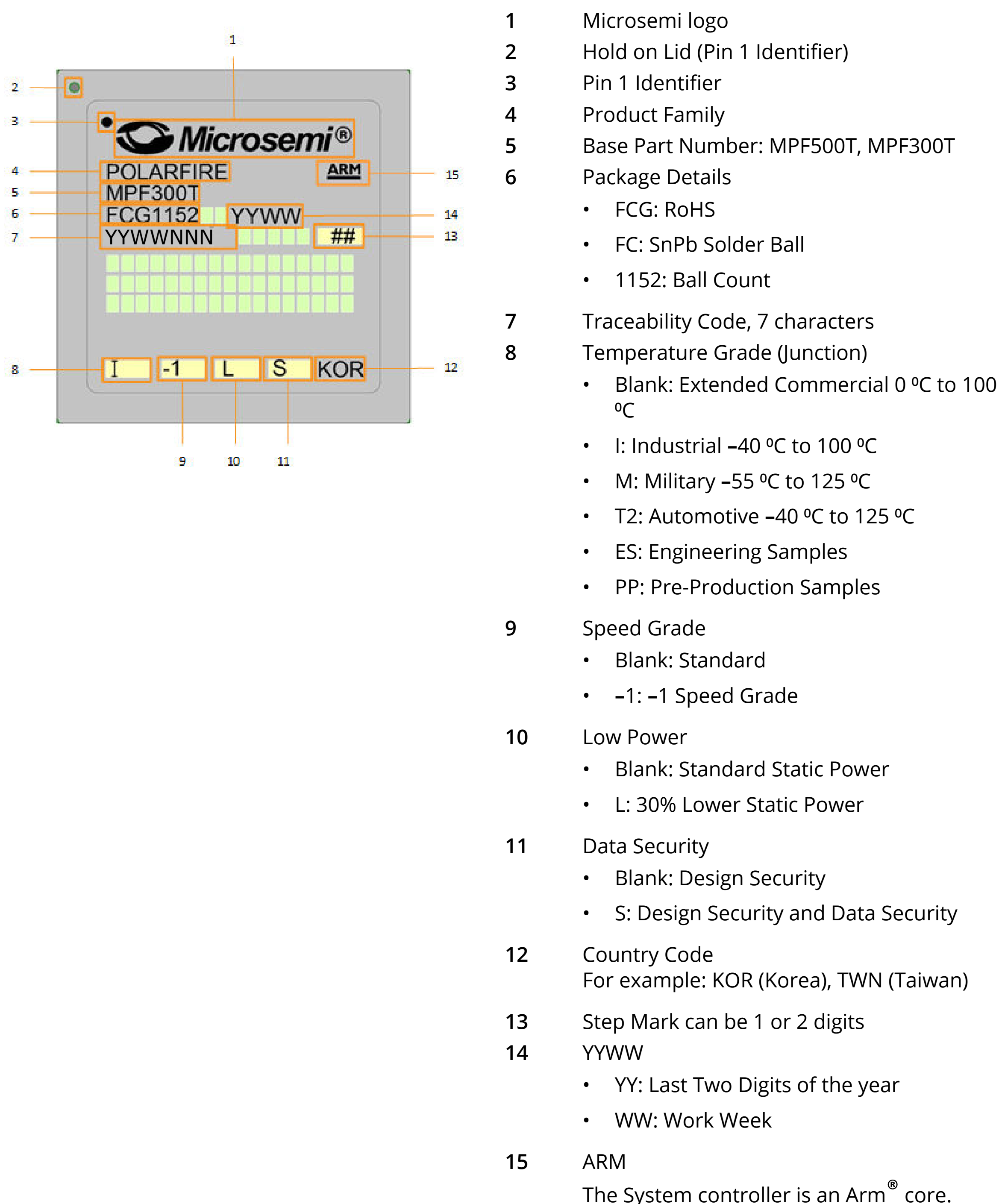
# 10. Package Marking (Ask a Question)

In general, Microchip marks the full ordering part number on the top of each device. The following figure provides details for each character code present on Microchip's PolarFire FPGA device.

**Figure 10-1.** Detailed Marking for Each Character Code




1 Microsemi logo

2 Hold on Lid (Pin 1 Identifier)

3 Pin 1 Identifier

4 Product Family

5 Base Part Number: MPF500T, MPF300T

6 Package Details
- FCG: RoHS
- FC: SnPb Solder Ball
- 1152: Ball Count

7 Traceability Code, 7 characters

8 Temperature Grade (Junction)
- Blank: Extended Commercial 0 ºC to 100 ºC
- I: Industrial –40 ºC to 100 ºC
- M: Military –55 ºC to 125 ºC
- T2: Automotive –40 ºC to 125 ºC
- ES: Engineering Samples
- PP: Pre-Production Samples

9 Speed Grade
- Blank: Standard
- –1: –1 Speed Grade

10 Low Power
- Blank: Standard Static Power
- L: 30% Lower Static Power

11 Data Security
- Blank: Design Security
- S: Design Security and Data Security

12 Country Code
For example: KOR (Korea), TWN (Taiwan)

13 Step Mark can be 1 or 2 digits

14 YYWW
- YY: Last Two Digits of the year
- WW: Work Week

15 ARM
The System controller is an Arm® core.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# 11. Packing and Shipping (Ask a Question)

The PolarFire series device is packed in trays, which are used to pack most of the Microchip surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

The following table lists the standard device counts per tray and carton.

**Table 11-1.** Standard Device Counts per Tray and Carton

| Package | Maximum Number of Devices Per Tray | Maximum Number Trays Per Stack | Maximum Number of Units per Inner Carton |
|---|---|---|---|
| FCG1152 | 24 | 5 | 120 |
| FCG484 | 60 | 5 | 300 |
| FCVG484 | 84 | 5 | 420 |
| FCSG536 | 90 | 5 | 450 |
| FCSG325 | 176 | 5 | 880 |


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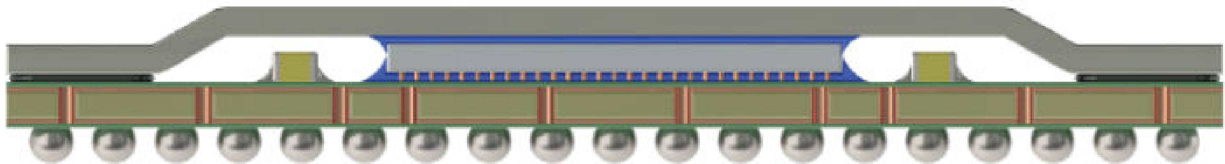
# 12. Thermal Management (Ask a Question)

Microchip PolarFire FPGAs are offered in lidded Flip-Chip BGA (FCBGA) format. Lidded FCBGA features a controlled bond-line Thermal Interface Material (TIM) thickness that reduces the thermal resistance (Theta-JC) between the junction and the externally applied thermal solution. The lid or heat spreader also spreads the heat away from the die to the package perimeter and to the PCB.

Optimized package electrical performance with multiple power and ground planes to take care of signal return paths, and dense core via under the die to improve power delivery adds benefit in dissipating heat through the bottom of the package and to the board.

PolarFire FPGAs in FCG484 are also available in bare die FCBGA. Bare die FCBGA produces the lowest possible thermal resistance (Theta-JC) between the junction and any externally applied thermal solution.

**Figure 12-1.** Heat Spreader with Thermal Interface Material



## 12.1. System Level Heat Sink Solutions (Ask a Question)

The use of external heat sinks, component placement in the PCB, and air flow in the system depends on the physical and mechanical limitations of the system. A system level thermal design engineer must understand these limitations and device capabilities to effectively manage the complete thermal strategy.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# 13. Thermal Interface Material (Ask a Question)

When using external heat sinks, a suitable thermal interface material must be considered to effectively transfer the heat from the component to the heat sink, and eventually to the environment.

For bare-die FCBGAs, the surface of the silicon contacts the heat sink. For lidded FCBGAs, the lid contacts the heat sink. The surface size of the bare-die FCBGA and lidded FCBGAs are different. Microchip recommends a different type of thermal material for long-term use with each type of FCBGAs package.

For lidded FCBGAs, the lid contacts the external heat sink while bare die FCBGAs, the surface of the silicon contacts the external heat sink. The surface areas of lidded FCBGAs and bare die FCBGAs are different. The system level thermal design engineer must choose the appropriate TIM to be used.

Thermal interface material is required because the surfaces of both the PolarFire package and heat sinks base are not smooth. The surface roughness reduces the effective contact area between the package and the heat sinks base. The insulating air gaps created by voids between contacting surfaces are too large. The thermal interface materials fills these gaps and allows an effective conductive transfer of heat from the package to the external heat sink.

Selection of the appropriate thermal interface material is critical to ensure the lowest thermal contact resistance. One must consider the thermal conductivity of the TIM—flatness of the surface contact areas, the applied pressure on the thermal interface material and the total thermal contact area. In addition to thermal performance, TIMs are selected based on the ease of use in assembly and long term reliability.

## 13.1. Heat Sink Attachments (Ask a Question)

Seven main methods for heat sink attachment are as follows.

- Thermal tape
- Thermally conductive adhesive
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs
- Thermal compound (also called as thermal gel, thermal grease, thermal paste, heat-sink paste or heat-sink compound)


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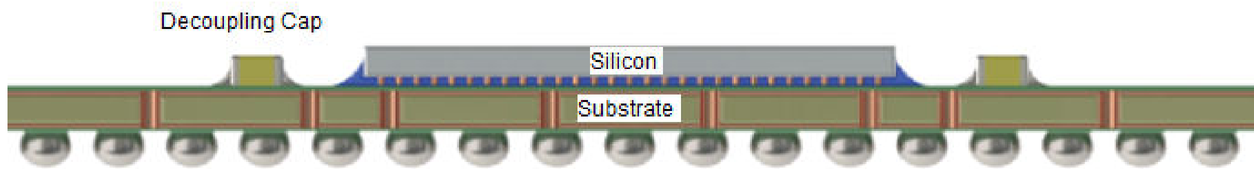
# 14. Heat Sink Guidelines for Bare-Die Flip-Chip Packages (Ask a Question)

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

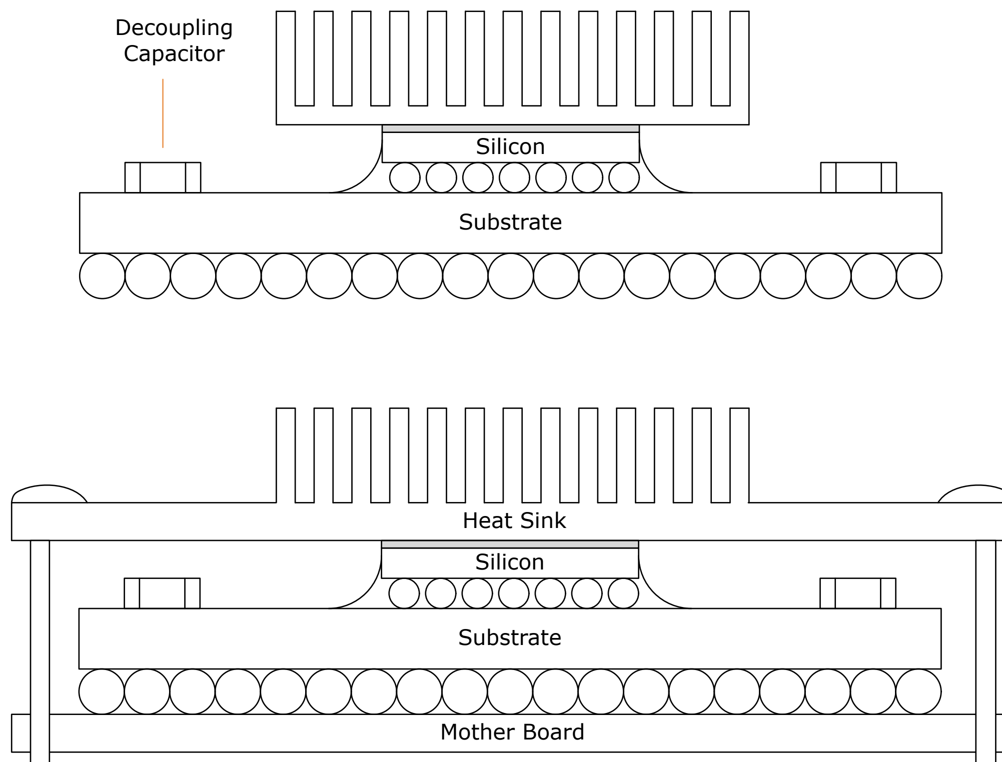
When designing heat sink attachments for bare-die FCBGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered. This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors. When attaching the heat sink to the bare-die FCBGA, ensure that the TIM thickness and the force applied during heat sink placement are even.

**Figure 14-1.** Cross Section of Bare-Die FCBGA




Care must be taken while attaching a heat sink to the bare-die package after the component is placed onto PCBs.

**Figure 14-2.** Recommended Application of Heat Sink





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# 15. Heat Sink Removal Procedure (Ask a Question)

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care must be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut must reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.


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# 16. Recommended PCB Design Rules for BGA Packages (Ask a Question)

Microchip provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and summarized in the following table. For Microchip BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter) and the solder mask opening (diameter) as shown in the following figure.

The space between the NSMD pad and the solder mask; the actual signal trace widths and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

**Figure 16-1.** Ball and Via Dimensions

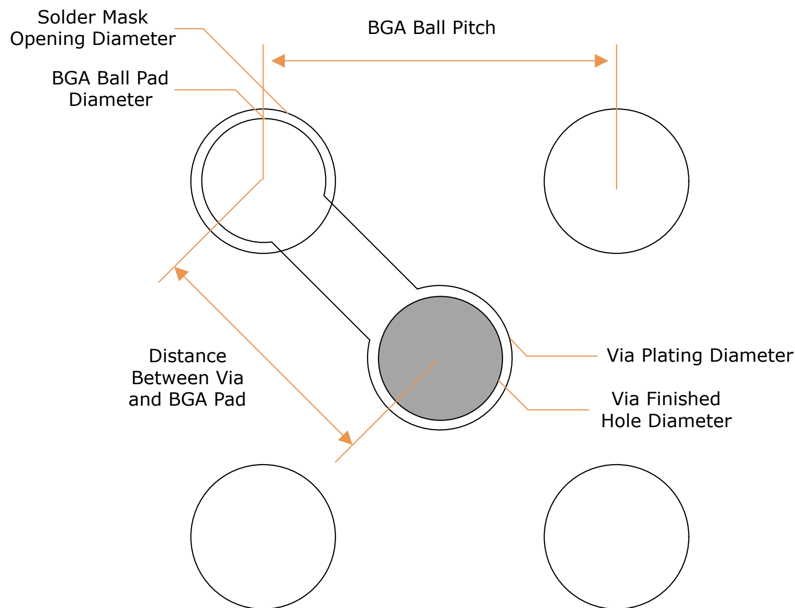


**Table 16-1.** Recommended PCB Design Rules

| Design Rule for Packages | 0.5 mm Pitch | 0.8 mm Pitch | 1.0 mm Pitch |
|---|---|---|---|
| | FCSG | FCVG | FCG |
| BGA ball pad diameter | 0.27 mm | 0.4 mm | 0.51 mm |
| Solder mask opening diameter | 0.3 mm | 0.43 mm | 0.54 mm |
| BGA ball pitch | 0.5 mm (19.7 mils) | 0.8 mm (31.5 mils) | 1.00 mm (39.37 mils) |
| Line width between via and solder land | 0.13 mm | 0.13 mm | 0.15 mm |
| Distance between via and solder land | 0.35 mm | 0.56 mm | 0.7 mm |
| Via finished hole diameter | 0.1 mm | 0.33 mm | 0.33 mm |
| Via plating diameter | 0.25 mm | 0.48 mm | 0.48 mm |

**Important:** For more information about package fanout, see AC462: PolarFire FPGA Package Fanout Application Note.


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# 17. Moisture Sensitive Level (Ask a Question)

The following table lists Microchip PolarFire packages Moisture Sensitive Levels (MSL). For information about solder re-flow guidelines for Sn/Pb and Pb-free, see ww1.microchip.com/downloads/en/Quality_ReliabilityDocs/SolderabilityEvaluation_11_11_21.pdf

**Table 17-1.** Moisture Sensitive Levels

| Package | MSL |
|---|---|
| FCG1152 | 4 |
| FCG784 | 4 |
| FCG484 | 4 |
| FCVG484 | 4 |
| FCSG536 | 3 |
| FCSG325 | 3 |


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# 18. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

**Table 18-1.** Revision History

| Revision | Date | Description |
|---|---|---|
| G | 05/2025 | The following is a summary of the changes made in revision G of this document.<br>• Added a note regarding unused pin recommendations in the XCVR Interface section.<br>• Updated Figure 7-3, Figure 7-5, Figure 7-10, Figure 7-15, Figure 7-18, Figure 7-23 and Figure 7-25 in the Mechanical Drawings section.<br>• Added MPF300T-FCG784N to Table 8-3 in the Package Material Information section. |
| F | 04/2025 | The following is a summary of the changes made in revision F of this document.<br>• Updated all Bank Locations figures in the Bank Locations.<br>• Updated Vented Package information for MPF500T-FC1152M in the Table 8-3 in the Package Material Information. |
| E | 03/2024 | The following is a summary of the changes made in revision E of this document.<br>• Updated Figure 2-9 by adding a note: In MPF200T devices, Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively, within the package substrate for pin migration compatibility.<br>• Updated Figure 10-1 by updating the marking with Traceability Code instead of Wafer Lot. |
| D | 12/2023 | In revision D of the document, updated Figure 10-1. |
| C | 08/2023 | The following is a summary of the changes made in revision C of this document.<br>• Updated Table 9-1 with the missing packages in revision B.<br>– MPF050T-FCVG484<br>– MPF050T-FCSG325<br>– MPF200T-FCVG484<br>– MPF100T-FCVG484<br>– MPF300T-FCSG536/MPF300T-FCS536M<br>– MPF200T-FCSG536<br>– MPF200T-FCSG325/MPF200T-FCS325M<br>– MPF100T-FCSG325 |
| B | 01/2023 | The following is a summary of the changes made in revision B of this document.<br>• Added the serial transceiver channel value for the MPF050T device in Table 2-2.<br>• Updated Figure 10-1. |


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**Table 18-1.** Revision History (continued)

| Revision | Date | Description |
|---|---|---|
| A | 09/2022 | The following is a summary of the changes made in revision A of this document.<br>• Migrated the document from Microsemi template to Microchip's template.<br>• Updated Table 1-1.<br>• Updated LPRB_A/B pins inTable 5-10.<br>• Updated Table 5-11.<br>• Updated Shield signal pins in Table 5-10.<br>• Updated Table 7-1.<br>• Added a note and table for MPF050T device in IOD Interfaces.<br>• Updated Figure 7 to include MPF300T/MPF200T/MPF100T/MPF050T packages.<br>• Updated Figure 8 to include MPF050T package.<br>• Updated Table 2-1 to include MPF050T package.<br>• Updated Table 6-2 to include MPF050T package.<br>• Updated Table 6-1 to include MPF050T package.<br>• Added MPF050T package top-view, side-view, and bottom view in Mechanical Drawings. |
| 12.0 | — | The following is a summary of the changes made in revision 12.0 of this document.<br>• Updated Table 1.<br>• Added "IOD Interfaces" section. |
| 11.0 | — | The following is a summary of the changes made in revision 11.0 of this document.<br>• Updated Table 1.<br>• Added Figure 9, and Figure 10.<br>• Updated Figure 13, Figure 14, Figure 21, Figure 22, Figure 29, and Figure 30.<br>• Updated Table 18 and Table 19. |
| 10.0 | — | The following is a summary of the changes made in revision 10.0 of this document.<br>• PPAT files website link was updated in "Packaging Pin Assignment" section.<br>• Updated Table 4 in HSIO column for the Cold sparing I/O feature.<br>• Updated "Dedicated I/O Bank Pins" section and "JTAG Pins" section.<br>• Updated "Dedicated I/O Bank Pins" section.<br>• A note regarding the ball pinout and spacing are the same on both packages (that is, MPF100 and MPF200), which allows the user to use one PCB footprint was updated. "Mechanical Drawings" section.<br>• Updated Figure 1 through Figure 8.<br>• Updated Table 2. |
| 9.0 | — | MPF300-FCG784N mechanical drawings were added in this revision. See Figure 15, Figure 16, and Figure 17. |
| 8.0 | — | The following is a summary of the changes made in revision 8.0 of this document.<br>• Information about Supply Pins was updated.<br>• A note regarding I/O bank locations was updated. See note below Figure 6, Figure 7, Figure 5, and Figure 8.<br>• Information about preferred clock inputs was updated. See Clocking Pins.<br>• Information about Package Material Information was updated. |


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**Table 18-1.** Revision History (continued)

| Revision | Date | Description |
|---|---|---|
| 7.0 | — | The following is a summary of the changes made in revision 7.0 of this document.<br>• Information about special pins was added. See Table 13.<br>• Information about vent hole diameter was updated. See Table 20.<br>• FF_EXIT_N pin was changed to RESERVED as Flash*Freeze is de-featured in the Libero® SoC PolarFire® software. See Table 13 |
| 6.0 | — | The following is a summary of the changes made in revision 6.0 of this document.<br>• Information about VDD18 was updated. See Table 5.<br>• Information about Pin compatible packages was added. See Table 16.<br>• FCG484 mechanical drawings were added. See Figure 21, Figure 22, Figure 23, Figure 24, Figure 26, and Figure 27.<br>• Information about package material was added. See Package Material Information.<br>• Information about Packaging Pin Assignment. |
| 5.0 | — | Information about I/O bank locations was updated. See Figure 1, Figure 2, Figure 3, Figure 4, Figure 6, Figure 7, Figure 5, and Figure 8. |
| 4.0 | — | The following is a summary of the changes made in revision 4.0 of this document.<br>• Information about shield output pin was updated. See Table 13.<br>• Information about VDDIx (JTAG bank) and VDD_XCVR_CLK operating voltage was updated. See Table 5.<br>• Information about auxiliary supply for I/O circuits was updated. See Table 5.<br>• Information about Thermal resistance was updated. See Thermal Specifications.<br>• Information about PCB design rules was added. See Recommended PCB Design Rules for BGAPackages.<br>• Information about heat sink guidelines was added. See Thermal Management.<br>• FCSG325 and FCSG536 mechanical drawings were added. See Figure 31, Figure 32, Figure 33, Figure 34, Figure 35, and Figure 36. |
| 3.0 | — | The following is a summary of the changes made in revision 3.0 of this document.<br>• Information about Package marking was added. See Package Marking.<br>• Information about thermal resistances of PolarFire Package device was added. See Thermal Specifications.<br>Table 3 and Table 17 were added. |
| 2.0 | — | The following is a summary of the changes made in revision 2.0 of this document.<br>• Figure 6 and Figure 7 were updated.<br>• Information about unused condition of pins was updated. See Table 5, Table 11, Table 12, Table 13, and Table 14, page 16. |
| 1.0 | — | The first publication of this document. |


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ISBN: 979-8-3371-1233-6

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