PolarFire® SoC FPGA: Interrupt Latency and Data Transfer Throughput Measurements

Introduction

Microchip's PolarFire® SoC FPGAs include the industry's RISC-V based Microprocessor Subsystem (MSS) and FPGA fabric that inherits all the features of the PolarFire family. The PolarFire SoC MSS includes 5x 64-bit RISC-V processor cores, AXI switch, DDR controller, Fabric Interface Controllers (FIC), and a rich set of peripherals. It also offers an unparalleled combination of low power consumption, thermal efficiency, and defense-grade security for smart, connected systems. It is the first SoC FPGA with a deterministic L2 memory subsystem enabling real-time applications. Built on the award-winning, mid-range, low-power PolarFire FPGA architecture, PolarFire SoC devices deliver up to 50% lower power than alternative FPGAs, span from 25k to 460k logic elements, and feature 12.7G transceivers.

Microchip's PolarFire SoC Icicle kit features an MPFS250T PolarFire SoC device and on- board memories such as LPDDR4, SPI, and eMMC flash for running Linux. For more information, see the PolarFire® SoC FPGA ICICLE Kit User Guide.

The following measurements are performed on PolarFire SoC FPGA:

- Interrupt latency difference between Global and Local interrupts.
- Data transfer throughput is measured from LIM to Fabric LSRAM and Fabric LSRAM to LIM.

Interrupt latency refers to the delay between the start of an Interrupt and the detection of the interrupt by the processor in the application. The interrupt latency is expressed in processor clock cycles. Latency measurement is carried out and compared between Local interrupt and Global interrupt using the Bare metal application. Local interrupts are signaled directly to an individual hart with a dedicated interrupt value. This allows for reduced interrupt latency. Global interrupts by contrast, are routed through a Platform-Level Interrupt Controller (PLIC), which can direct interrupts to any hart in the system through the external interrupt.

For more information, see the PolarFire SoC FPGA MSS Technical Reference Manual.

The interrupt latency and the data transfer throughput are measured using the PolarFire SoC FPGA Icicle kit. The following table lists the configuration used for the measurements.

Table 1. System Configuration

System Configuration	Description
Device	PolarFire SoC FPGA, RISC-V 64-bit
Application	Bare Metal
CPU Core Frequency	625 MHz
Compiler	RISC-V GCC
Target Processor	riscv64
Tool Chain	SoftConsole v2021.1
SoftConsole Tool Optimization Level	None is used for interrupt latency measurement. Optimize fast (-Ofast) is used for data transfer throughput measurement between LIM and Fabric LSRAM.
MPFS-HAL	Version 1.8.117
Linker Script Settings	Instruction Tightly Integrated Memory (ITIM) used for the code section. Scratchpad is used for the stack.
FIC and Fabric Frequency	200 MHz
Interrupt Lines Used	MSS_INT_F2M0 (Local) and MSS_INT_F2M1 (Global)

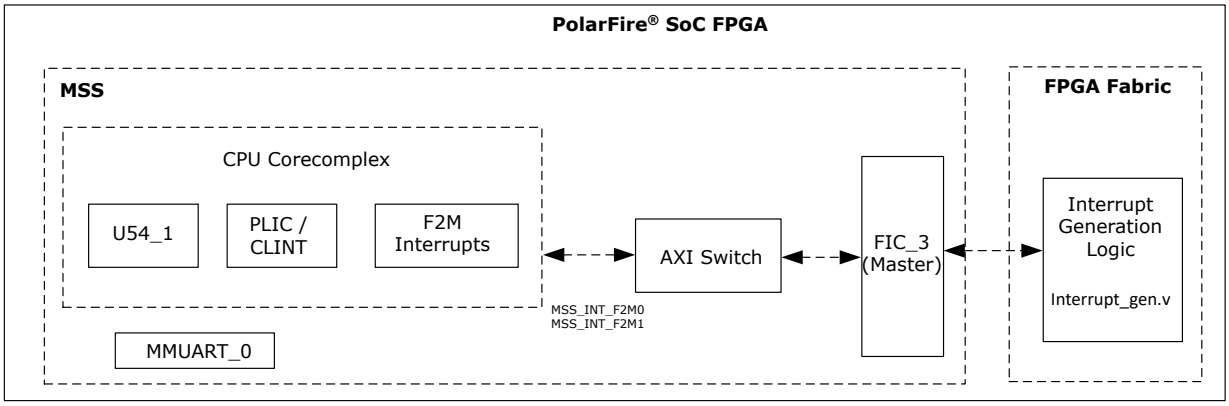
Table of Contents

1. Interrupt Latency Measurement

Figure 1-1 shows the top-level block diagram for Interrupt latency measurement. The **Expose Interrupt ports to Fabric** option in the **PolarFire SoC MSS configurator > Misc** tab and the **Use Master interface** option in the **PolarFire SoC MSS configurator > Fabric Interface Controllers** tab are enabled. The Global or Local interrupt that is generated from the fabric interrupt_gen.v is connected to MSS F2M interrupt lines. The application running on the U54_1 processor clears the interrupt by writing to the fabric register using the FIC3 interface.

Interrupt lines used are MSS_INT_F2M0 and MSS_INT_F2M1. The common interrupt vector is used for global and local interrupts. The source of the interrupt is verified in the handle_trap function of mpfs_hal by reading mcause Control and Status Register (CSR).

Figure 1-1. For Interrupt Latency Measurement



The following table lists the fabric logic address map for generating Local and Global interrupts.

Table 1-1. MSS Memory Map for Interrupt Generation

FIC3 Address	Data	Operation
0x40000000	0x1	Generates the local interrupt
0x40000000	0x0	Clears the interrupt
0x40000000	0x2	Generates the global interrupt
0x40000000	0x0	Clears the interrupt

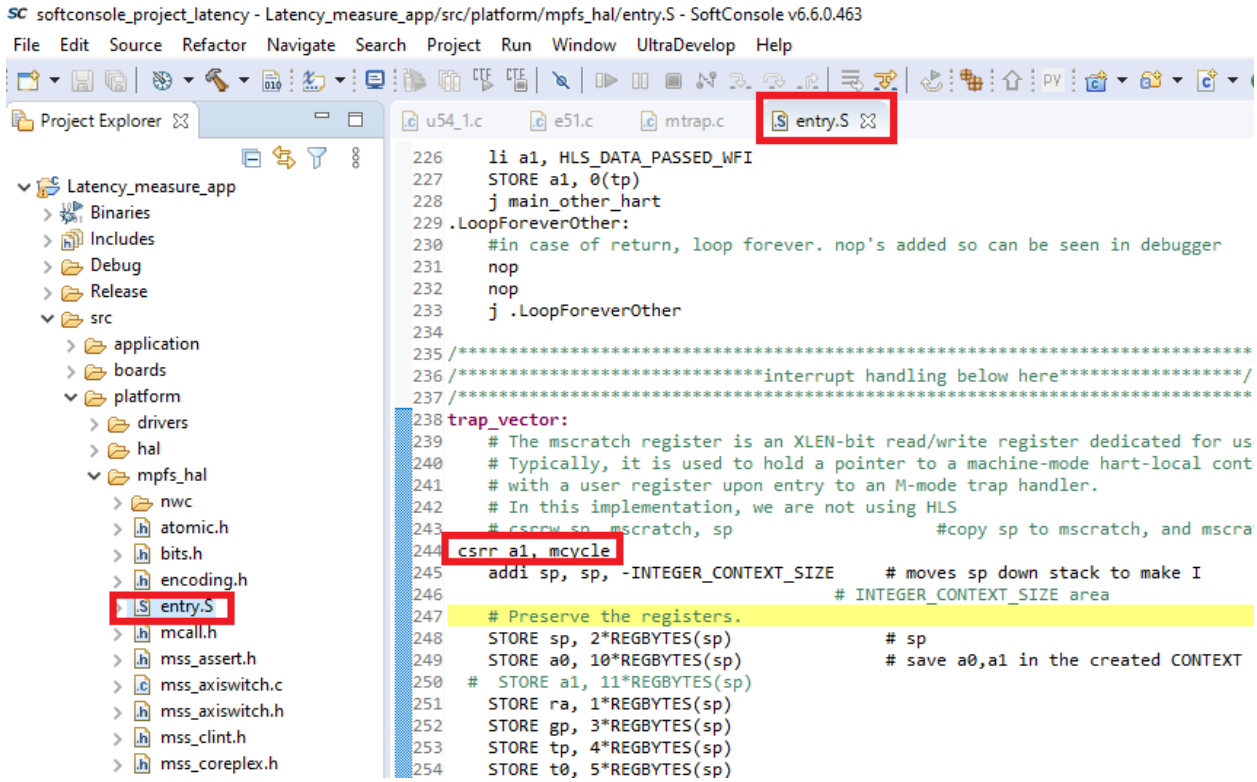
Implementation

The MSS_INT_F2M0 port is used for the local interrupt and MSS_INT_F2M1 port is used for the Global interrupt. Both these interrupts are mapped to the U54_1 application core. The FIC3 is used for interfacing with the fabric interrupt generation logic. The MMUART port is enabled for serial communication.

See Table 1-1 for generating Local and Global interrupts.

For measuring the interrupt latency, the hardware performance monitoring CSR “mcycle” is read before asserting an interrupt. The mcycle CSR is again read as soon as the interrupts enter the trap vector function, as shown in Figure 1-2. The time difference between mcycle read values are used to measure the interrupt latency.

Figure 1-2. Stop mcycle CSR in entry.S



2. Data Transfers Throughput between LIM and FPGA Fabric LSRAM

Figure 2-1 shows the block diagram for measuring the throughput for data transfers between LIM and fabric LSRAM. LSRAM block is connected to the MSS using the FIC0 interface. The core complex Direct Memory Access (DMA) is used for data transfers between LIM and LSRAM, and throughput is measured. To achieve this, the PDMA driver is added to the Bare Metal application and configured with required registers. See Table 2-1 for fabric LSRAM and LIM address map.

Figure 2-1. Data Transfers between LIM and FPGA Fabric LSRAM

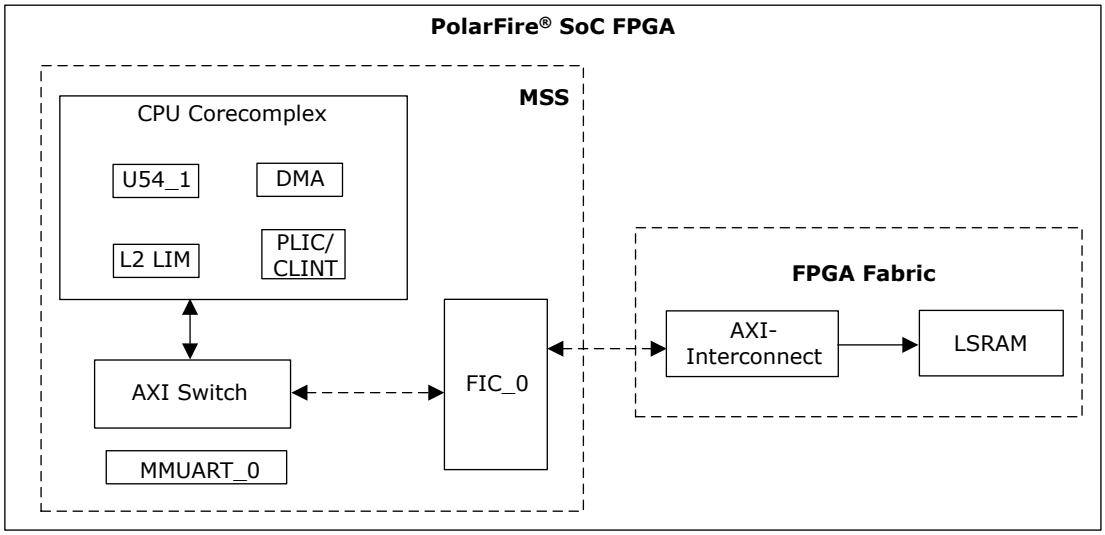


Table 2-1. Memory Map for Data Transfer Between LIM and Fabric LSRAM

Address Range Used	Memory
0x61000000 to 0x61ffffff	Fabric LSRAM
0x08000000 to 0x08100000	LIM

Implementation

To perform LSRAM to LIM data transfer, the fabric LSRAM is initialized by the application core (U54_1), with an incremental data pattern. Core complex DMA is initialized by declaring DMA channel and configured by writing to the channel registers —source address (LSRAM), destination address (LIM), and number of bytes to transfer. The DMA transfer is initiated using setup transfer and start DMA transfer functions. DMA transfer complete status is checked, then the LIM data is read and verified.

To perform LIM to LSRAM data transfer, the source address is replaced with the destination address and vice-versa. The same process as described in preceding paragraph is repeated.

For measuring the data transfer throughput, CSR mcycle is read before DMA transfer and after the DMA transfer completion. The time difference between mcycle read values are used to convert into bits/seconds.

3. Results

The following table lists the interrupt latency measurement results.

Table 3-1. Interrupt Latency Measurement Results

Interrupt Type	Interrupt Latency
Global	37 core clock cycles
Local	30 core clock cycles
CLINT Software Interrupt	16 core clock cycles

Note: Software CLINT latency is generated in u54_1 core and handled in mtrap function.

Table 3-2. Data Transfer Throughput Between LIM and Fabric LSRAM using MSS PDMA

Transfer Size in Bytes	LSRAM to LIM		LIM to LSRAM	
	Core Clock Cycles	Mbits/Seconds	Core Clock Cycles	Mbits/Seconds
1 Kbyte	965	5350.052	1061	4862.298
4 Kbytes	3439	5969.105	3683	5572.789
8 Kbytes	6743	6081.663	7169	5719.872
16 Kbytes	13363	6134.032	14165	5786.537
32 Kbytes	26521	6179.61	28129	5826.251
64 Kbytes	52933	6191.403	56033	5848.817
128 Kbytes	105719	6199.544	112009	5851.376
256 Kbytes	211439	6199.28	223789	5857.155

4. Conclusion

This white paper provides the latency measurements for the Global and Local interrupts, and the throughput measurements for data transfers between LIM and Fabric LSRAM. The Local interrupt detection time is seven core clock cycles faster than the Global interrupt detection. For a DMA transfer of size 64 Kbytes, a throughput of 6191 Mbps for LSRAM to LIM and 5848 Mbps for LIM and LSRAM can be achieved.

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