4Gbps - 10.7Gbps 2:1 LVPECL/CML MULTIPLEXERS with INTERNAL TERMINATION

Precision Edge™ SY58017/18/19U EVALUATION BOARD

FEATURES

- **Precision, fully differential 2:1 multiplexers**
  - **SY58017U—10.7Gbps throughput, CML outputs**
  - **SY58018U—5Gbps throughput, full swing LVPECL outputs**
  - **SY58019U—10.7Gbps throughput, 400mV LVPECL outputs**
- **Low jitter performance**
  - **<10ps$_{p-p}$ total jitter (clock)**
  - **<1ps$_{rms}$ random jitter (data)**
  - **<10ps$_{p-p}$ deterministic jitter (data)**
- **Fully differential inputs/outputs**
- **Unique input isolation design minimizes crosstalk**
- **Accepts an input signal as low as 100mV**
- **Unique input termination and V_T pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **Industrial –40°C to +85°C temperature range**
- **Available in 16-pin (3mm × 3mm) MLF™ package**

APPLICATIONS

- **Redundant clock and/or distribution**
- **OC-12 to OC-192 SONET/SDH clock/data distribution**
- **Loopback**
- **Fibre Channel distribution**

DESCRIPTION

The SY58017U, SY58018U, and SY58019U are 2.5V/3.3V precision, high-speed, fully differential 2:1 multiplexers with CML, LVPECL, and 400mV LVPECL outputs. The SY58017U and SY58019U can process data rates as fast as 10.7Gbps, whereas, the SY58018U (800mV LVPECL) can process data rates as fast as 5Gbps.

The 2:1 MUX family includes Micrel's unique, 3-pin input termination architecture which allows the devices to directly interface to LVPECL, CML, and LVDS differential signals (AC-coupled or DC-coupled) without any level-shifting or termination resistor network in the signal path.

This documentation provides design and implementation information, and a detailed description of the SY58017U, SY58018U, and SY58019U evaluation boards. The evaluation boards are intended to provide a convenient test and evaluation platform for all three devices.

All data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

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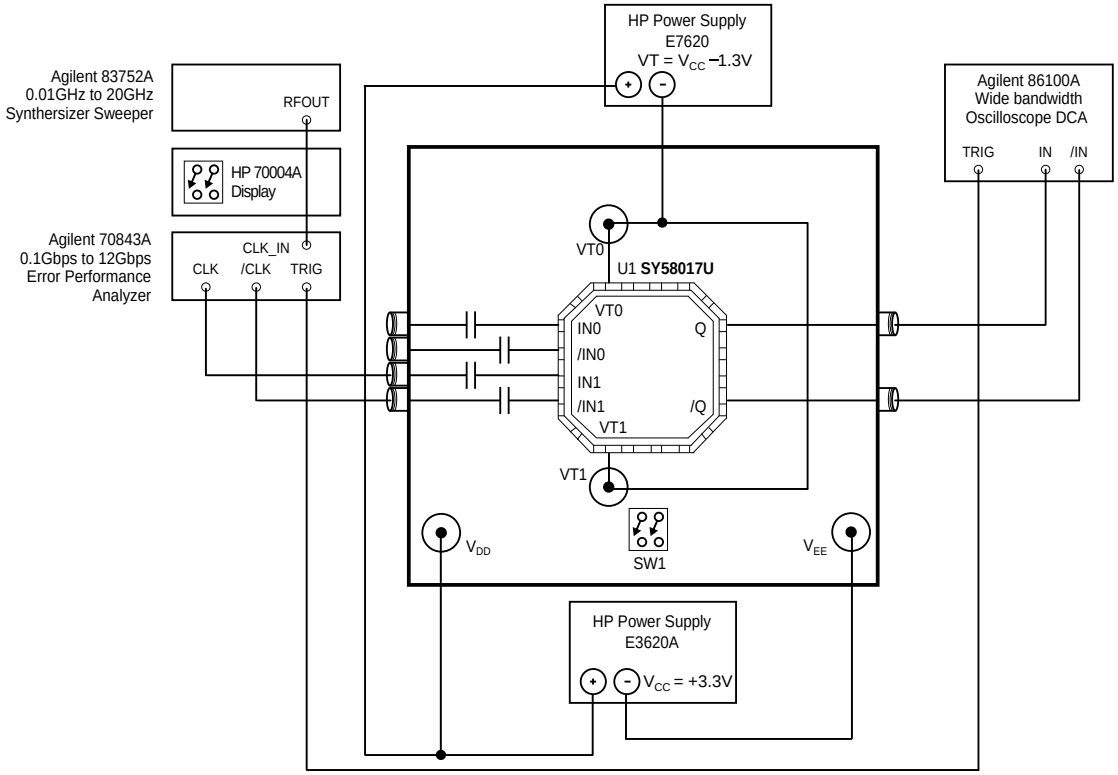


Figure 1. SY58017U Evaluation Board and DC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

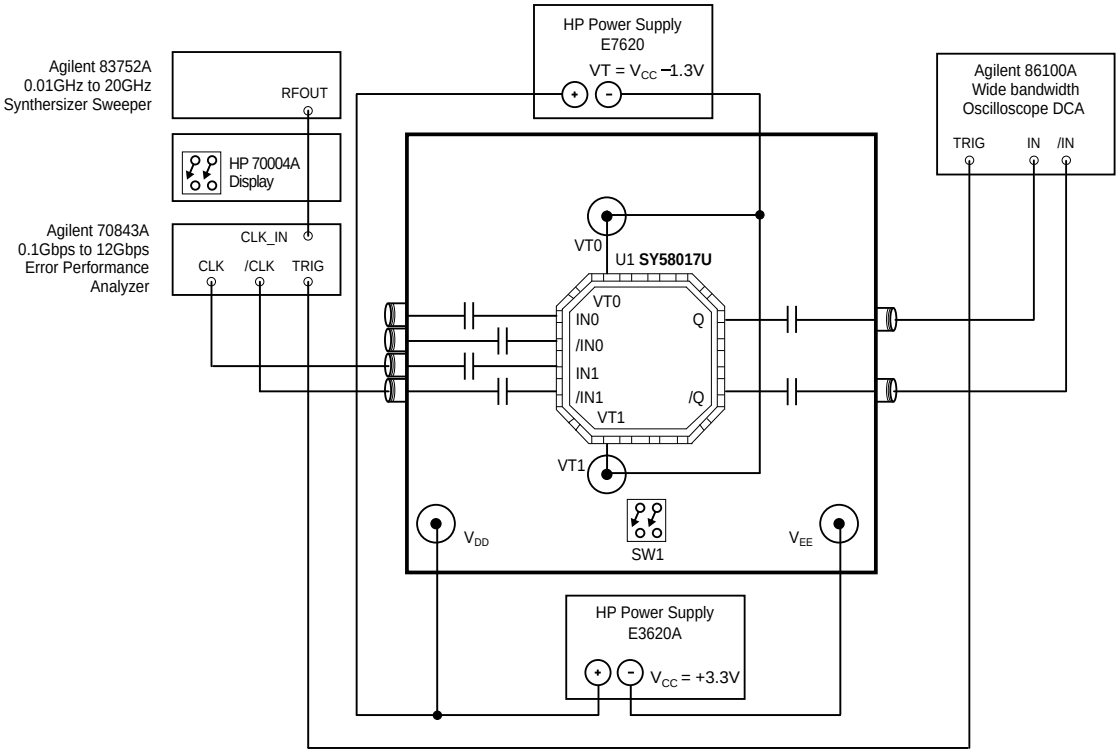


Figure 2. SY58017U Evaluation Board and AC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

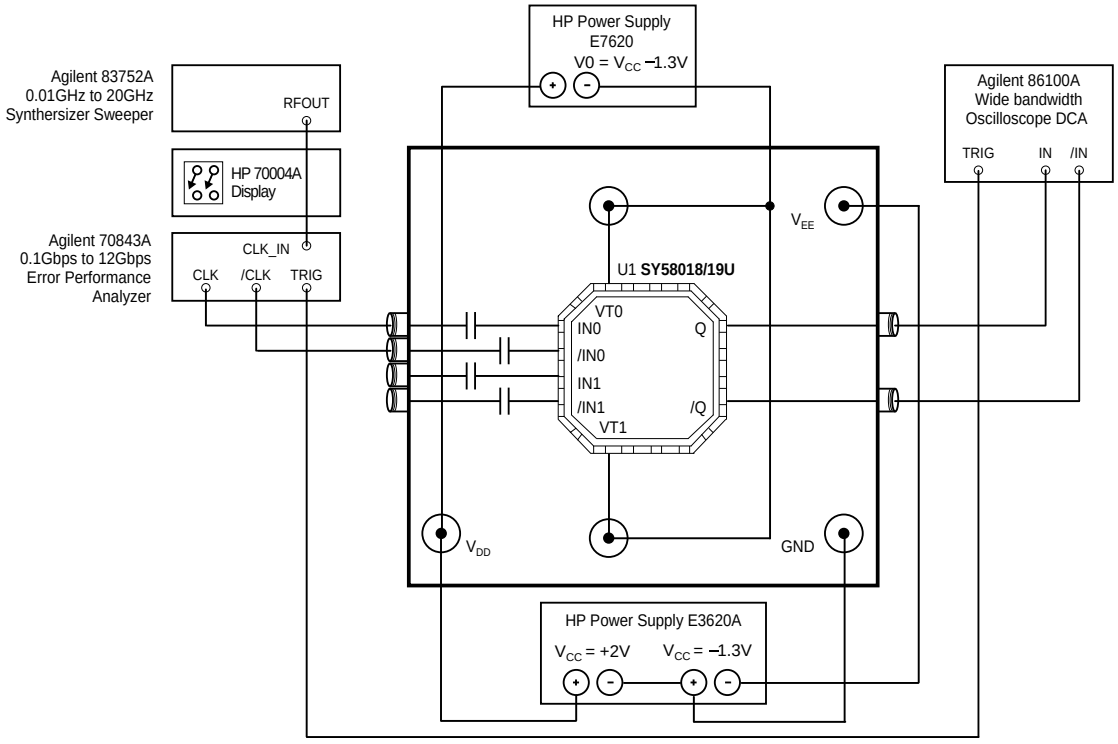


Figure 3. SY58018/19U Evaluation Board and DC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

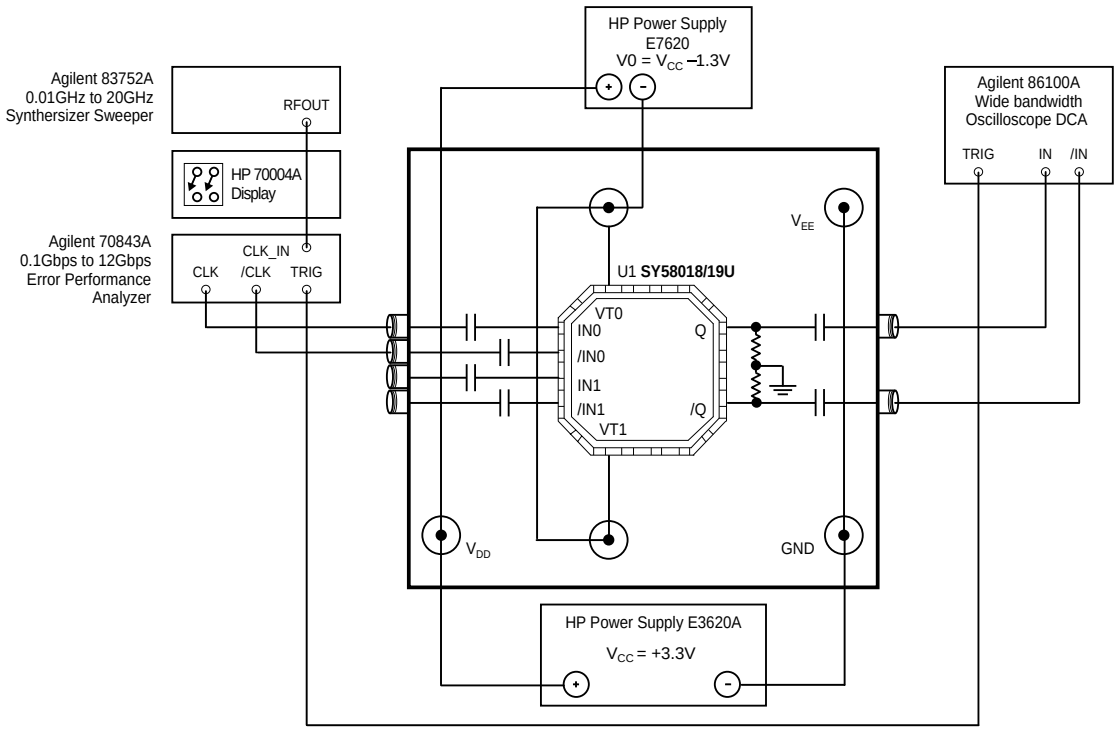


Figure 4. SY58018/19U Evaluation Board and AC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

FUNCTIONAL DESCRIPTION

The SY58017U, SY58018U, and SY58019U evaluation boards simplify test and measurement of jitter and AC-performance and have been preconfigured to function at both 2.5V ±5% and 3.3V ±10% supply voltage.

Signal Inputs/Outputs

The SY58017/18/19U evaluation board have been designed with AC-coupled inputs and DC-coupled outputs. The SY58017U, SY58018U, and SY58019U require a minimum of 100mV input signal to operate. The SY58017U CML outputs typically swing 400mV into 50Ω. The SY58018U provides full 800mV LVPECL swing at the outputs, and the SY58019U provides a faster, reduced swing 400mV at the outputs. Unused output pairs maybe left floating with no impact on jitter.

Power Supply

The SY58018U and SY58019U evaluation boards, as shown in Figure 4, have been configured for split power supply, meaning V_{CC} = 2V, and GND = 0, and V_{EE} = (–0.5V or –1.3V). Therefore, the SY58018U and SY58019U are shipped with split power supply, so that the outputs can directly interface with a 50Ω load. The SY58017U evaluation board, as shown in Figure 1, has been configured for positive power supply, or V_{CC} = +3.3V, GND = 0V and V_{EE} = 0V.

SY58017U—AC-Coupled Output Configuration

The SY58017U can be configured for AC-coupled output and normal supply or V_{CC} = 2.5V/3.3V and GND = V_{EE} = 0 by following the next few steps.

1. Replace the 0Ω resistors at C5 and C6 with 0.1µF capacitors, see Figure 7.

SY58018/19U—AC-Coupled Output Configuration

In addition, the SY58018U and SY58019U can be configured in AC-coupled output mode (V_{CC} = 2.5V/3.3V and GND = V_{EE} = 0V), by following the next few steps.

1. Add capacitors C5 and C6, which normally are 0.1µF, see Figure 8. (The value depends on the frequency of application).
2. Add resistors R2 and R3, which is 50Ω if V_{CC} = 2.5V, and 100Ω if V_{CC} = 3.3V.

Board Layout

The evaluation boards are constructed with Rogers 4003 material and is co-planer in design and is constructed to minimize noise, achieve high bandwidth, and minimize cross-talk.

Layer Stack SY58017U

L1	Signal/V_{DD}
L2	V_{DD}
L3	GND
L4	Signal/GND

Layer Stack SY58018/19U

L1	Signal/GND
L2	Impedance GND
L3	V_{CC}
L4	Signal/GND

Test Description

This section contains step by step instructions for evaluating the SY58017U, SY58018U, and SY58019U. There are several evaluation tests that can be performed. First, the devices can be tested functionally for AC-performance including eye-diagram generation, and second, the devices can be tested for jitter.

Functionality AC-Testing

Equipment

1. HP3620A Power Supply
2. Agilent 86100A Widebandwidth Oscilloscope DCA
3. Agilent 83752A 0.1-20GHz Synthesizer Sweeper
4. HP70004A Display
5. Agilent 70843A 0.1-12Gbps Error Performance Analyzer
6. Wavecrest DTS-2079
7. HP8133A Frequency Generator
8. Harbour Industries Stiff Cables Model 2748 SB-142

AC-Testing

SY58017U

1. Connect V_{CC} to +3.3V, GND to 0V, and V_{EE} = 0V and set V_T = V_{CC} –1.3, as shown in Figure 1.
2. Using an Agilent BERT Stack connect OUT and /OUT to IN and /IN of the SY58017U.
3. Set the desired frequency of operation, and make sure that V_{IL} and V_{IH} and f_{MAX} are within datasheet limits. The SY58017U can accept LVPECL, LVDS, and CML input compatible signals.

   If an eye-diagram is desired, set the Agilent BERT Stack to 2^{23}–1 PRBS pattern. If a clock pattern is desired, set the Agilent BERT Stack accordingly.
4. Connect OUT and /OUT of the evaluation board to an oscilloscope.
5. Connect the trigger out connection of the Agilent BERT Stack to the input trigger of the oscilloscope and make measurement.

SY58018U and SY58019U

1. Connect V_{CC} to 2V, GND to 0V, and V_{EE} = (–0.5V or –1.3V) for DC-coupled outputs, as shown in Figure 3 and connect V_{CC} = 3.3V, GND and V_{EE} to 0V for AC-coupled outputs as shown in Figure 4.
2. Set $V_T = V_{CC}$–1.3V.
3. Using an Agilent BERT Stack connect OUT and /OUT to IN and /IN of the SY58018U or SY58019U.
4. Set the desired frequency of operation, and make sure that V_{IL} and V_{IH} and f_{MAX} are within datasheet limits. The SY58018U and SY58019U can accept LVPECL, LVDS, and CML input compatible signals. In addition, if an eye-diagram is desired, set the Agilent BERT Stack to 2^{23}–1 PRBS pattern, if a clock pattern is desired, set the Agilent BERT Stack accordingly.
5. Connect OUT and /OUT of the evaluation board to an oscilloscope.
6. Connect the trigger out connection of the Agilent BERT Stack to the input trigger of the oscilloscope and make measurement.

Jitter Test

Measuring jitter is a relative process and involves establishing a base line. Measure the generated jitter from a pulse generator used to drive the SY58017U, SY58018U, or SY58018U. Once this is established, jitter generated from the part is compared against the jitter generated from the pulse generator, and the difference is jitter generated from the DUT.

Deterministic Jitter (DJ)

This section describes how to measure DJ using the SY58017/18/19U evaluation board. An example bench setup is shown in Figure 5. Of the various methods to obtain DJ, this document describes how to use the Wavecrest DTS-2079 TIA. Other instruments, will require slightly different procedures, though the major steps are common. Following these instructions, you will be able to measure DJ, and obtain results like Figures 6a and 6b.

You will need:

- A SY58017U, SY58018U or SY58019U evaluation board
- A power supply
- A digital signal source capable of generating a fixed 20-bit or 32-bit pattern, at up to 2.5Gbps
- A Wavecrest DTS-2079 TIA
- Two pair of length-matched SMA cables

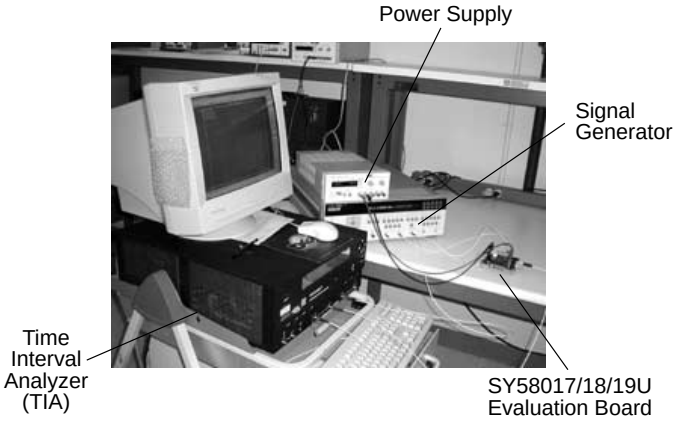


Figure 5. Measuring DJ

The following steps measure DJ using the SY58017U, SY58018U or SY58019U evaluation board:

1. *Connect Power Source:* (see above)

2. *Connect Data Source:* Set your data source to generate a pseudo-random data stream. Any pattern 2^7–1 PRBS or better will do. If there is a choice, use 2^{23}–1 PRBS. Set the data rate to 2.5Gbps. Set the output high level to be +400mV, and the output low level to be –400mV.

Using one pair of length matched SMA cables, connect the differential output of the signal generator to “IN”, labeled “/IN”. In the setup shown in Figure 5, an Agilent 8133A signal source generates a 2^{32} –1 PRBS pattern.

3. *Connect Data Output:* Using another pair of length matched SMA cables, connect “Q” and “/Q” to oscilloscope vertical channels. Connect a trigger output from the digital generator to the trigger input of the oscilloscope.

4. *Terminate Unused Inputs and Outputs:* Cap unused SMA connectors with 50Ω terminators.

5. *Measure Output Amplitude:* Measure the peak-to-peak amplitude of the output from the evaluation board.

6. *Adjust Source Amplitude:* Remove the connections to the oscilloscope. Move the connection from the signal source so that it now goes to the oscilloscope. Adjust the output amplitude of the signal source so that it equals the output amplitude measured in step 5.

7. *Use Data Source:* Set the data source to generate a K28.5 pattern, which is the 20-bit sequence “0011 1110 1011 0000 0101,” where the spaces are added for readability. The Agilent 8133A used in Figure 5 can only generate a 32-bit pattern. In this case, use “0011 1110 1011 1010 1100 0001 0100 0101,” where once again, spaces are added for readability.

8. *Calibrate TIA:* Connect the signal source to the TIA CH1. Connect the signal generator trigger output to the TIA ARM1, and set the signal generator to generate a trigger pulse once for each iteration of the pattern. Select TIA "DATACOM TOOLS," then "KNOWN PATTERN W/ MARKER." Select view of "DCD+DDJ vs. Spacing." Set "Quick Mode" and "Advanced" both on.

Click the PULSE FIND button and verify that there is swing on both CH1 and ARM1. On page 2, click the LEARN button. Set the data rate to 2500, the pattern length to 20 or 32 bits, as appropriate, and select the "DCD" check box. Save the calibration.

Return to page 1. Perform an acquisition, and record the DJ number. This step calibrates the TIA against the signal generator output, and then records the "clean" DJ value from this signal generator and TIA combination. You will get something like Figure 6a.

9. *Use the SY58017U, SY58018U or SY58019U evaluation board:* Connect the signal source to evaluation board "IN" and "/IN," as before. Connect the evaluation board TIA CH1. Connect a 50Ω termination to evaluation board labeled "/Q." Perform an acquisition on the TIA again. You will get something like Figure 6b. Record the new DJ number. The difference between this DJ value, and the DJ recorded in step 8, is the DJ.

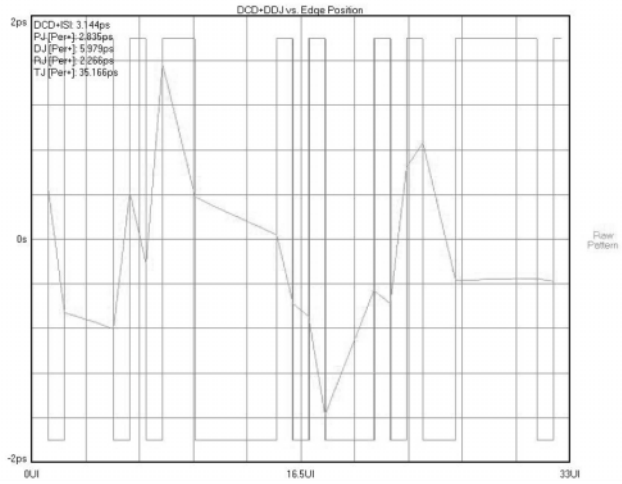


Figure 6a. TIA Output of the Source, Just After Calibration

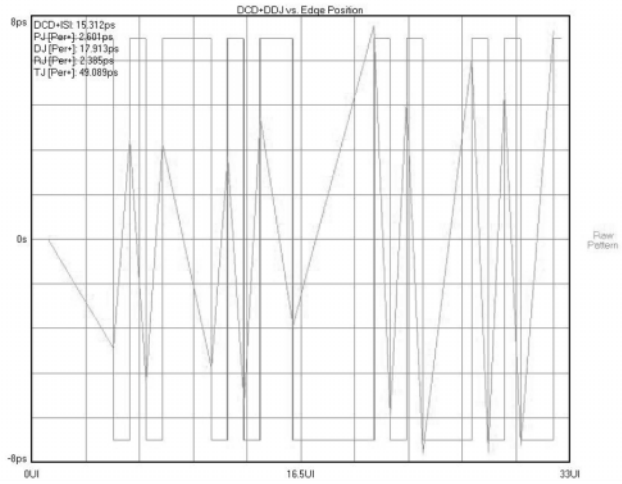
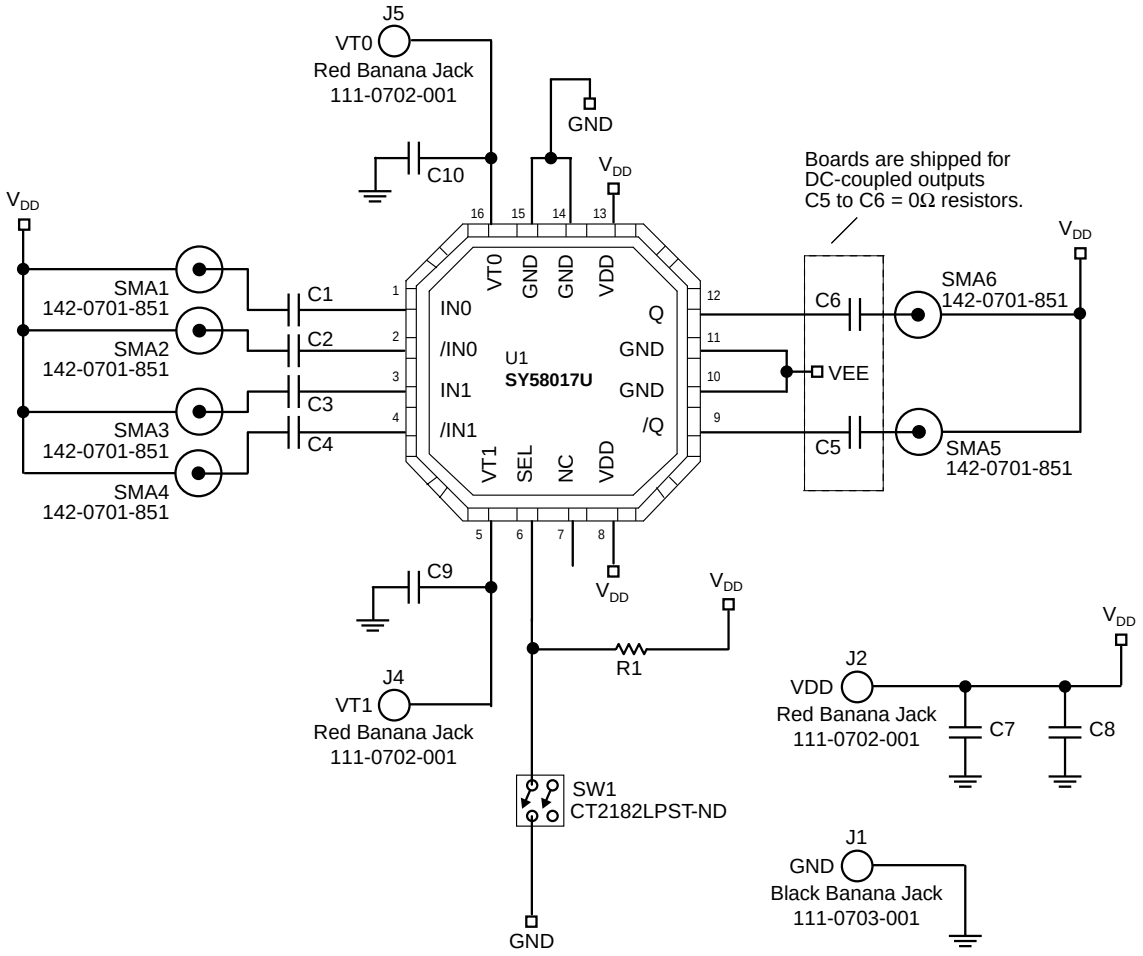


Figure 6b. TIA Output of the SY58017/18/19U Evaluation Board

Random Jitter

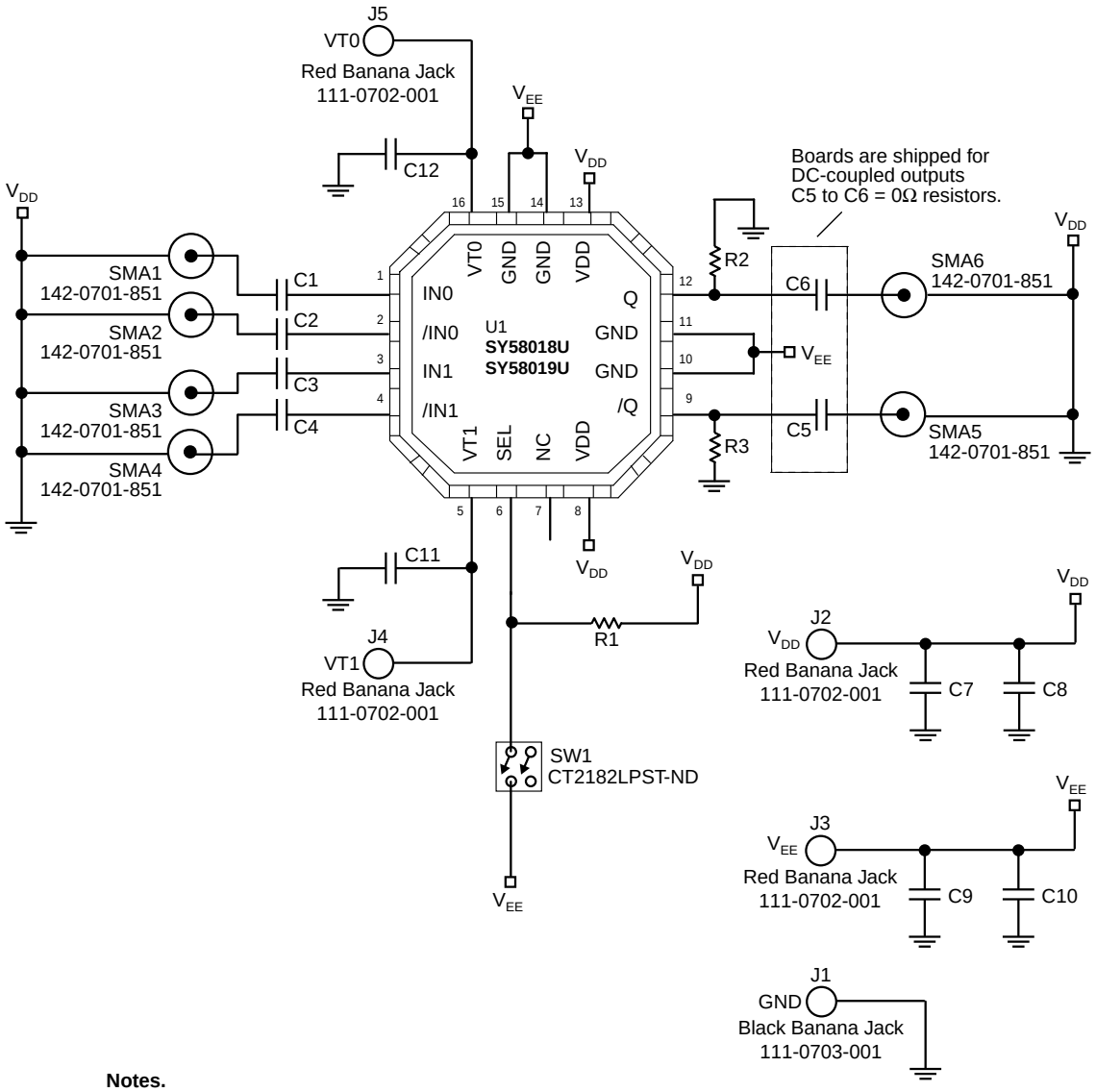
Random jitter can be measured two different ways. One way is similar to measuring the deterministic jitter which uses a Wavecrest DTS Instrument, but with a K28.7 1010... (clock pattern) using the same concept of measuring the jitter generated by the Agilent 8133A, then comparing it to the jitter generated from the device while driven by the Agilent 8133A. Another way is to drive the device using a clock pattern and measuring the histogram at the output using a Tektronic scope and directly measuring the random jitter.



Notes.

1. EPAD = GND.
2. In DC-coupled mode, C5 and C6 are 0Ω resistors.
3. In AC-coupled mode, C5 and C6 are 0.1µF capacitors, (actual value depends on the frequency of interest).

Figure 7. SY58017U Evaluation Board Schematic



Notes.

1. EPAD = V_{EE}.
2. In DC-coupled mode, C5 and C6 are 0Ω resistors and R2 and R3 are not mounted.
3. In AC-coupled mode, C5 and C6 are 0.1µF capacitors, (actual value depends on the frequency of interest). Additionally, R2 and R3 are 100Ω for a 3.3Vdc system and 50Ω for a 2.5Vdc system.

Figure 8. SY58018/19U Evaluation Board Schematic

BILL OF MATERIALS

SY58017U

Item	Part Number	Manufacturer	Description	Qty.
C1-C7, C9-C10		Panasonic(1, 5)	0.1µF, 25V, 10% Ceramic Capacitor, Size 0603, X5R, Dielectric	9
C8		Panasonic(1)	6.8µF, 20V, Tantalum Electrolytic Capacitor, Size C	1
J1	111-0703-001	Johnson Components(2)	Black Banana Jack	1
J2, J4, J5	111-0702-001	Johnson Components(2)	Red Banana Jack	3
R1		Panasonic(1)	3kΩ, 10%, Resistor, Size 0603	1
SMA1-SMA6	142-0701-851	Johnson Components(2)	Jack Assembly End Launch SMA	6
SW1	CT2182LPST-ND	CTS(3)	DIP- SWITCH	1
U1	SY58017U	**Micrel, Inc.**(4)	Evaluation Device	1

SY58018/19U

Item	Part Number	Manufacturer	Description	Qty.
C1-C7, C9, C11, C12		Panasonic(1, 6)	0.1µF, 25V, 10% Ceramic Capacitor, Size 0603, X5R, Dielectric	10
C8, C10		Panasonic(1)	6.8µF, 20V, Tantalum Electrolytic Capacitor, Size C	2
J1	111-0703-001	Johnson Components(2)	Black Banana Jack	1
J2-J5	111-0702-001	Johnson Components(2)	Red Banana Jack	4
R1		Panasonic(1)	3kΩ, 10%, Resistor, Size 0603	1
R2, R3		Panasonic(1, 7)	10%, Resistor, Size 0403	2
SMA1-SMA6	142-0701-851	Johnson Components(2)	Jack Assembly End Launch SMA	6
SW1	CT2182LPST-ND	CTS(3)	DIP- SWITCH	1
U1	SY58017U	**Micrel, Inc.**(4)	Evaluation Device	1

Notes:

1. Panasonic tel: 847-468-5624
2. Johnson Components tel: 800-247-8256
3. CTS tel: 574-293-7511
4. **Micrel, Inc.** tel: 408-944-0800
5. In DC-coupled mode, C5 and C6 are 0Ω resistors.
6. In DC-coupled mode, C5 and C6 are 0Ω resistors, and R2 and R3 are not mounted.
7. R2 and R3 are 0Ω resistors for 2.5V systems, and 100Ω for 3.3V systems.

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