PolarFire SoC Design Flow

AN5282

Introduction (Ask a Question)

This document demonstrates how to implement basic PolarFire® SoC FPGA designs leveraging the Libero® SoC design tool. The design targets the PolarFire SoC Discovery Kit.

After completing this demo, you will be familiar with the following:

- Creating a Libero SoC Project
- Compiling a Design
- Assigning simple I/O Pin constraints
- Programming the device
- Testing your design

Demo Requirements (Ask a Question)

The following table lists the hardware and software requirements for the demo.

Table 1. Design Requirements

Requirements	Version
Operating System	Windows® 10
Hardware	
PolarFire® SoC Discovery Kit (MPFS-DISCO-KIT)	REV 1
Software	
FlashPro® Express	Available with Libero® SoC installation package.
Libero SoC	

Prerequisites (Ask a Question)

Before you start, download and install Libero SoC on the host PC. To evaluate the designs using the PolarFire SoC Discovery Kit, use the free Libero SoC Silver license.

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1. Creating the Design (Ask a Question)

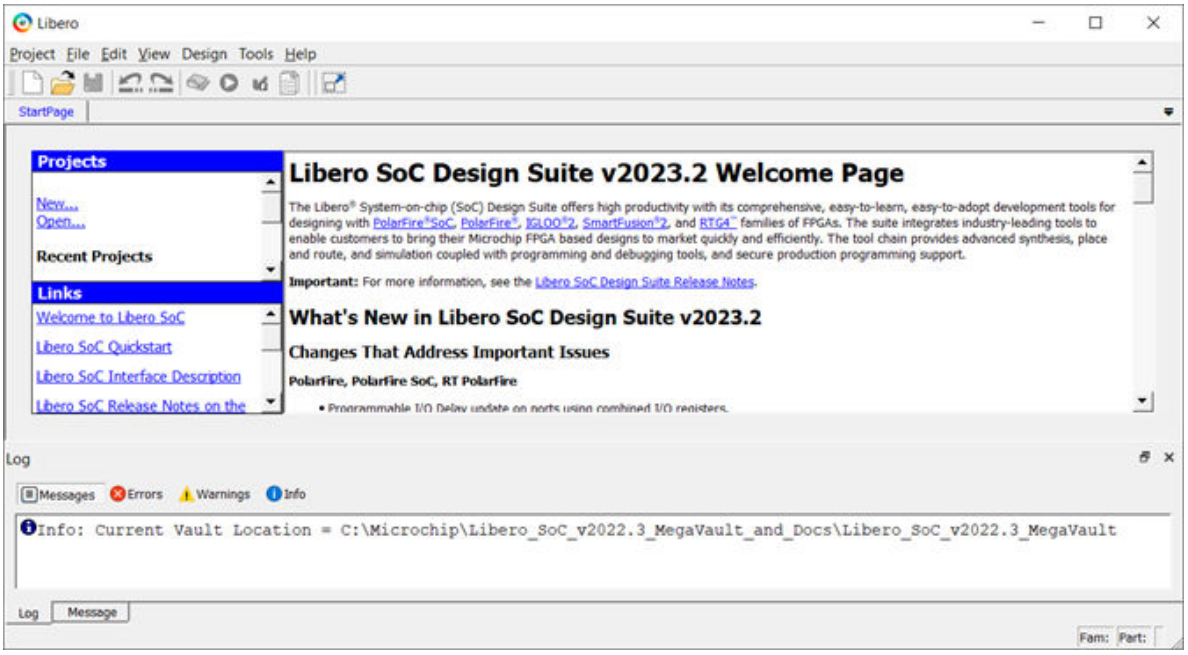
The following steps describe how to create a design using SmartDesign.

1.1 Launching the Libero SoC Software (Ask a Question)

Follow the instructions to launch the Libero SoC software:

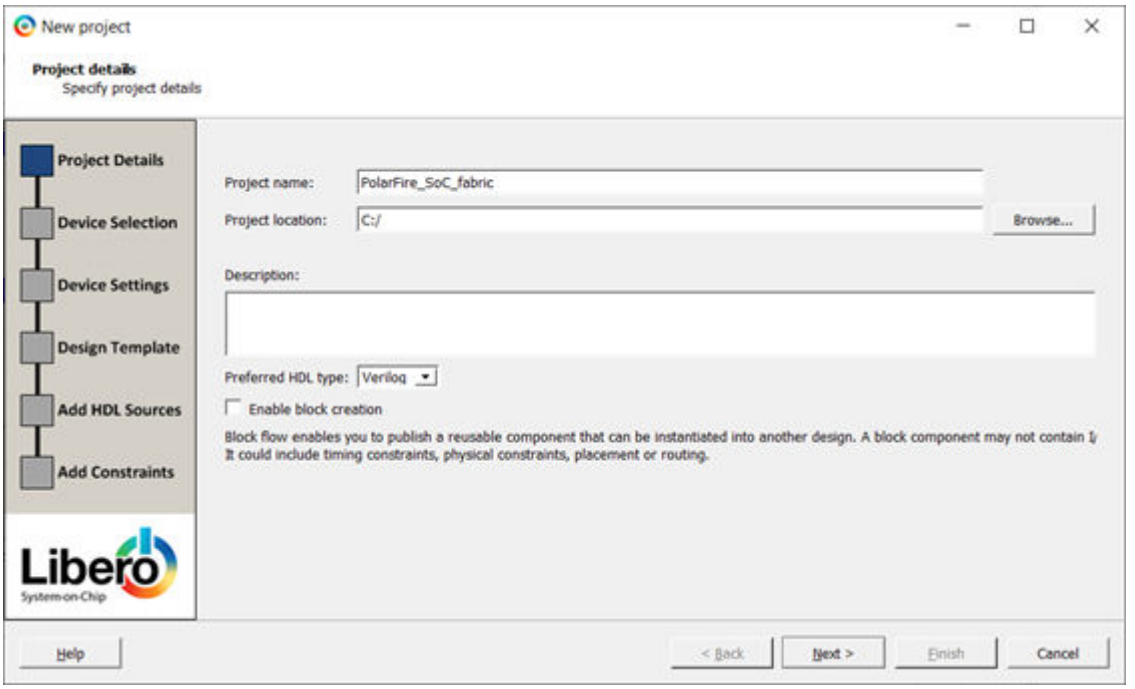
1. To open the **Libero SoC Project Manager,** go to **Start** > **Microchip Libero SoC v2023.2** > **Libero SoC v2023.2**, or double-click the shortcut on the desktop.
2. Create a new project using one of the following options:
   - Click **New** on the **Start Page** tab, as shown in the following figure
   - Go to **Project** > **New Project** from the Libero SoC menu

Figure 1-1. Libero® SoC Project Manager



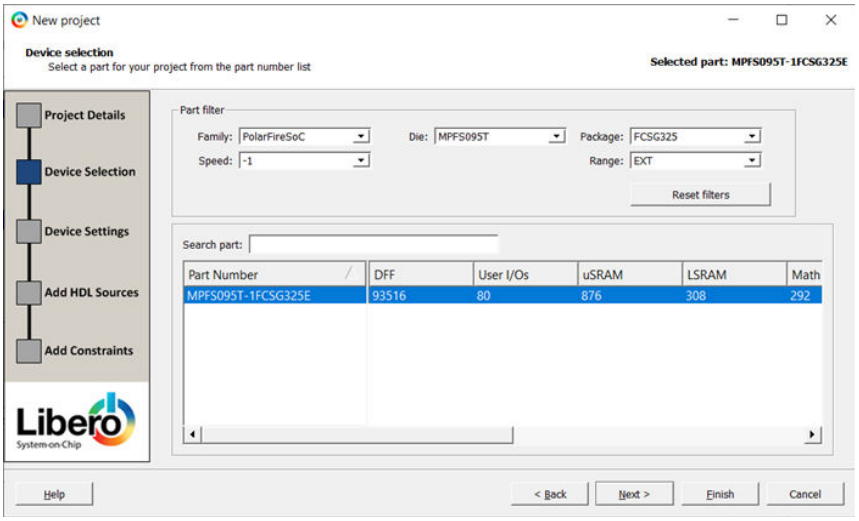
3. Enter the following information in the **Project Details** page of the **New Project** dialog box, as shown in the following figure:
   - **Project Name**: PolarFire_SoC_fabric
   - **Project Location**: `<C:, D:>/`
   - **Preferred HDL Type**: Verilog or VHDL
4. Click **Next**.

Figure 1-2. Project Details



5. Enter the following information in the **Device Selection** page of the **New Project** dialog box and click **Next**:
   - **Family**: PolarFireSoC
   - **Die**: MPFS095T
   - **Package**: FCSG325
   - **Speed**: -1
   - **Range**: EXT

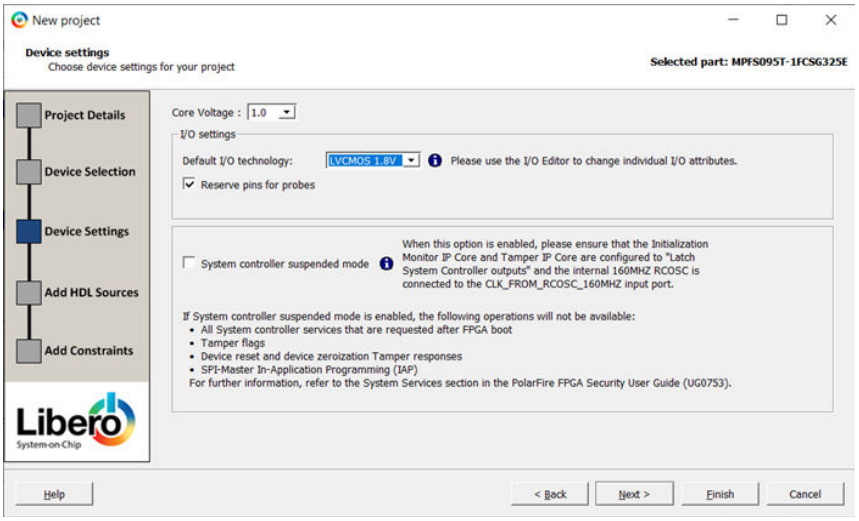
Figure 1-3. Device Selection Settings



6. Enter the following information in the **Device Settings** page of the **New Project** dialog box and click **Next**:
   - **Core Voltage**: 1.0 (default)

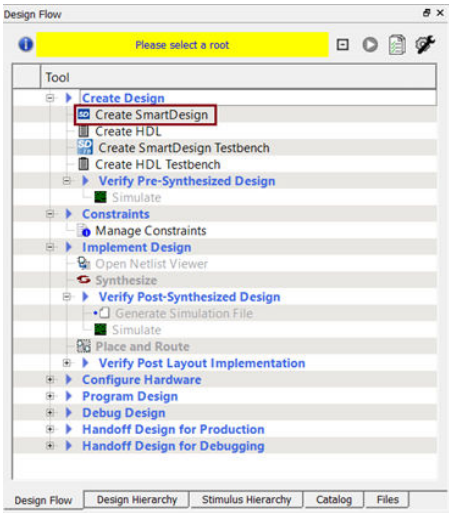
- **Default I/O Technology**: LVCMOS1.8V
- **Reserve Pins for Probes**: Checked (default)
- **System Controller Suspend Mode:** Un-checked (default)

Figure 1-4. Device I/O Settings



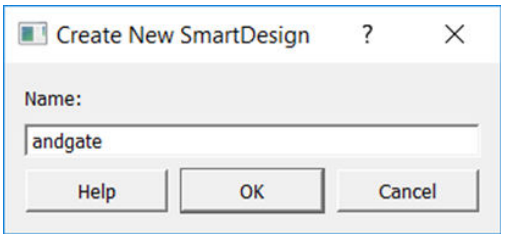
7. Click **Finish**.
8. Open the **SmartDesign canvas** by selecting **File** > **New** > **SmartDesign**, or by double-clicking **Create SmartDesign** under **Create Design** in the **Design Flow** tab.

Figure 1-5. Opening the SmartDesign Canvas



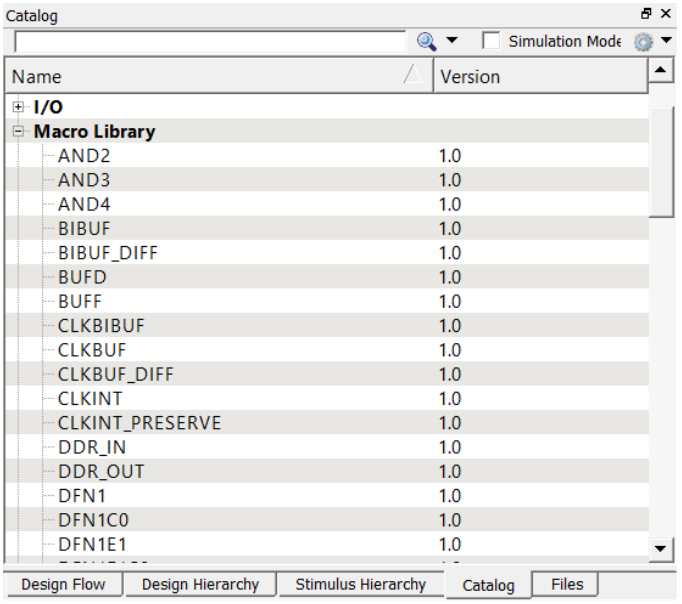
9. Enter **andgate** in the **Create New SmartDesign** dialog box, and click **OK**. For Verilog designs, the name is case sensitive.

Figure 1-6. Entering SmartDesign Name



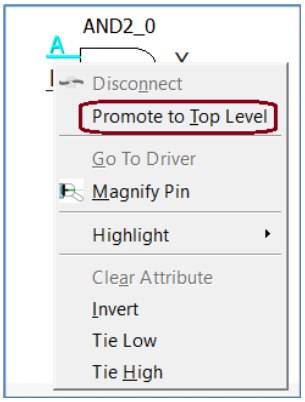
10. Expand **Macro Library** in the Libero SoC **IP catalog**.

Figure 1-7. Macro Library Category of the Libero SoC IP Catalog



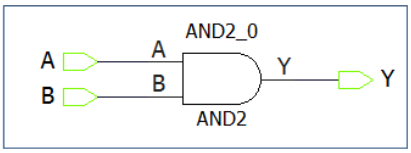
11. Drag-and-drop an instance of **AND2** in the **SmartDesign** Canvas.
12. In the **SmartDesign** canvas, select A, B, and Y pins. Right-click and select **Promote to Top Level** from the menu, as shown in the following figure. This creates an external connection on the device that can be connected to a switch.

Figure 1-8. Promoting Pins to Top Level



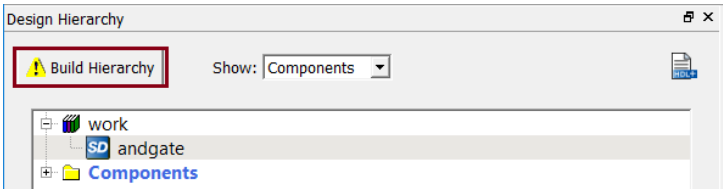
13. After making the connections, the **SmartDesign** canvas is displayed, as shown in the following figure.

Figure 1-9. andgate SmartDesign Canvas



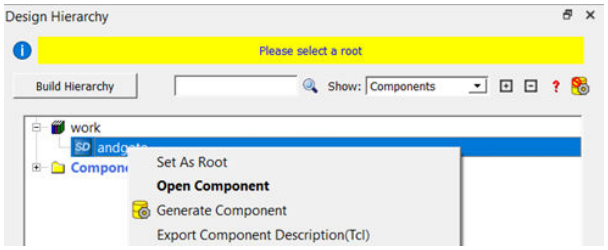
14. Save the design (**File** > **Save top**).
15. Generate the design by clicking **SmartDesign** > **Generate Component**, or **Generate Component** on the **SmartDesign** toolbar.
16. Select the **Design Hierarchy** tab and click **Build Hierarchy**.

Figure 1-10. Build Hierarchy



17. Select **andgate** on the **Design Hierarchy** tab. Right-click and select **Set As Root**. **andgate** appears in bold font on the Design Hierarchy tab indicating that it is the root level.

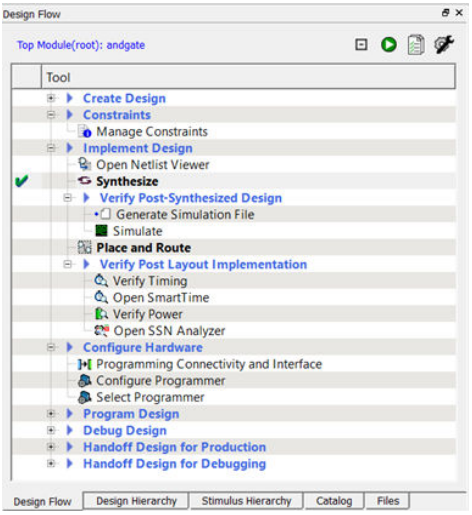
Figure 1-11. Set As Root



2. Synthesize the Design (Ask a Question)

To synthesize the design with Synplify Pro®, navigate to the **Design Flow** window, expand **Impelement Design**, right-click **Synthesize**, and select **Run**, as shown in the following figure.

Figure 2-1. Design Flow—Synthesize

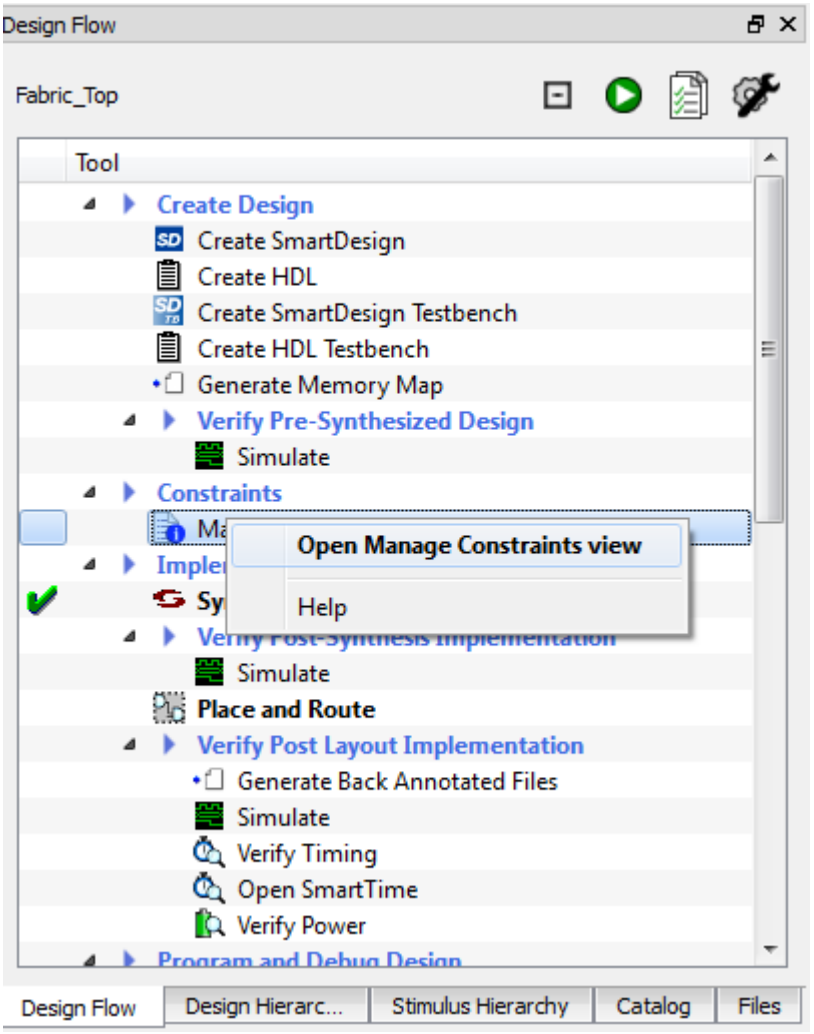


3. Pin Assignments (Ask a Question)

Follow the instructions to assign the pins in the software:

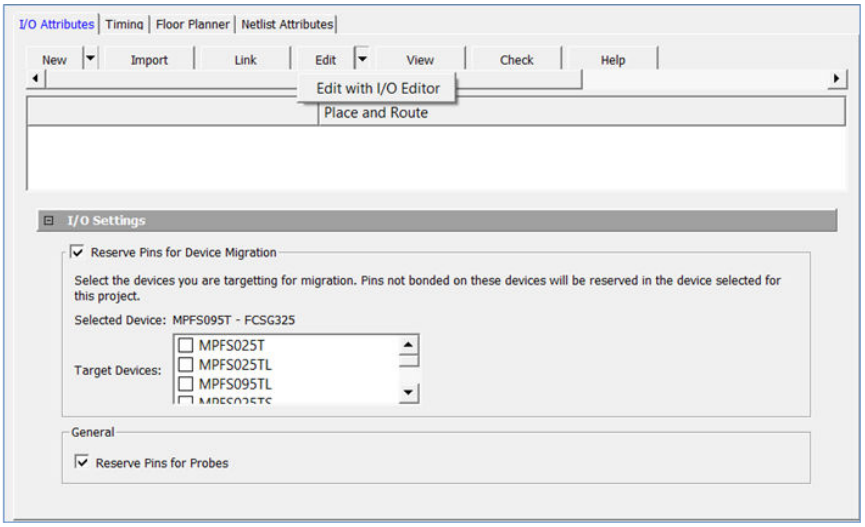
1. Navigate to the **Design Flow** window, expand **Constraints**, right-click **Manage Constraints**, and select **Open Manage Constraints View**.

Figure 3-1. Opening the I/O Editor



2. In the **Constraint Manager** window, select the **I/O Attributes** tab and click **Edit with I/O Editor**, see the following figure.

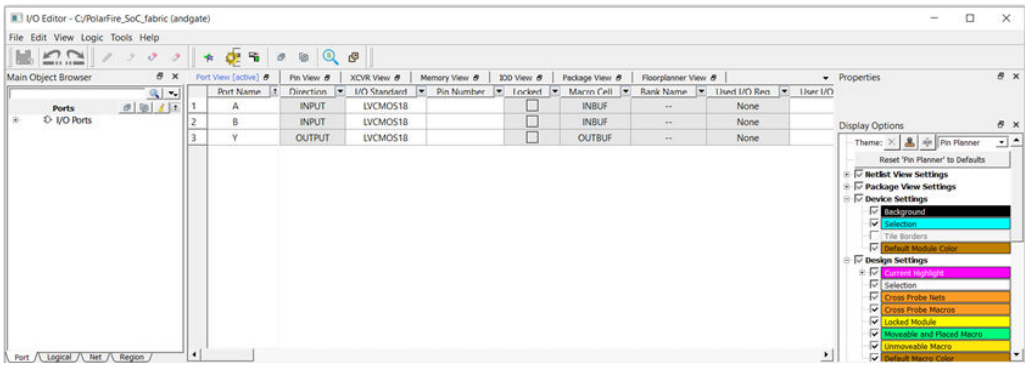
Figure 3-2. Constraint Manager Window



The I/O Editor page appears. See the following figure.

3. Select the **Port View** tab of the I/O Editor.

Figure 3-3. I/O Editor



4. Set the **I/O Standard** and **Pin Number** in this window. Confirm that **LVCMOS18** is the I/O Standard for each pin.
5. Navigate to the **Pin Number** column and click **Unassigned** in the **Pin Number** column to see the available I/O pins in **I/O Editor**. Make the following assignments:
   - A - T19
   - B - U18
   - Y - T18

   You can type the pin number in the field or use the pull-down menu to select the pin.
6. Select **File** > **Commit and Check** from the **I/O Attribute Editor** menu. Ensure that the **I/O Editor Log** window has no errors and the connections match as shown in the following figure.

Figure 3-4. Pin Assignments

	Port Name	Direction	I/O Standard	Pin Number	Locked	Macro Cell	Bank Name	Used I/O Reg	User I/O
1	A	INPUT	LVCMOS18	T19	☑	INBUF	Bank0	None	
2	B	INPUT	LVCMOS18	U18	☑	INBUF	Bank0	None	
3	Y	OUTPUT	LVCMOS18	T18	☑	OUTBUF	Bank0	None	

7. Close the I/O Attribute Editor using **File** > **Exit**.

3.1 Push Button Switches (Ask a Question)

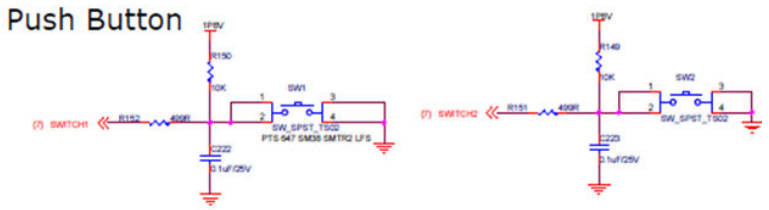
The PolarFire SoC Discovery Kit comes with two debug push-button switches that are connected to the PolarFire SoC FPGA. The following table lists the onboard push-button switches.

Table 3-1. PolarFire SoC Discovery Kit Pin Number and Pin Name

PolarFire® SoC Discovery Board	PolarFire SoC FPGA Pin Number	PolarFire SoC FPGA Pin Name
SWITCH1	T19	HSIO12NB0
SWITCH2	U18	HSIO15NB0/DQS

The following figure shows the schematics of Push Button.

Figure 3-5. Push Button Schematics



3.2 User LEDs (Ask a Question)

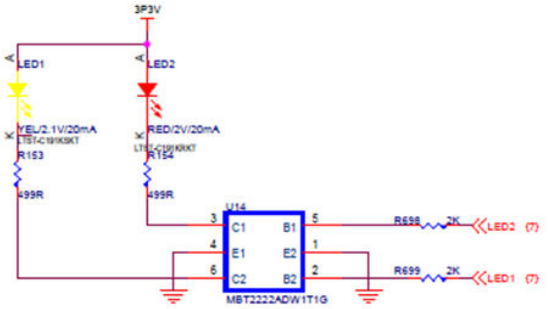
The board provides the access to eight active low LEDs, which are connected to the PolarFire SoC FPGA for debugging applications. The following table lists the onboard debugging LEDs.

Table 3-2. User LEDs

PolarFire® SoC Discovery Board	PolarFire SoC FPGA Pin Number	PolarFire Pin Name
LED1	T18	HSIO12PB0/CLKIN_N_9/CCC_NE_CLKIN_N_9

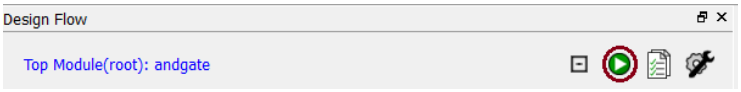
The following figure shows the user LED schematics.

Figure 3-6. User LED Schematics



If you click on the green arrow button at the top of the **Design Flow** window, you can run the design all the way through Place and Route.

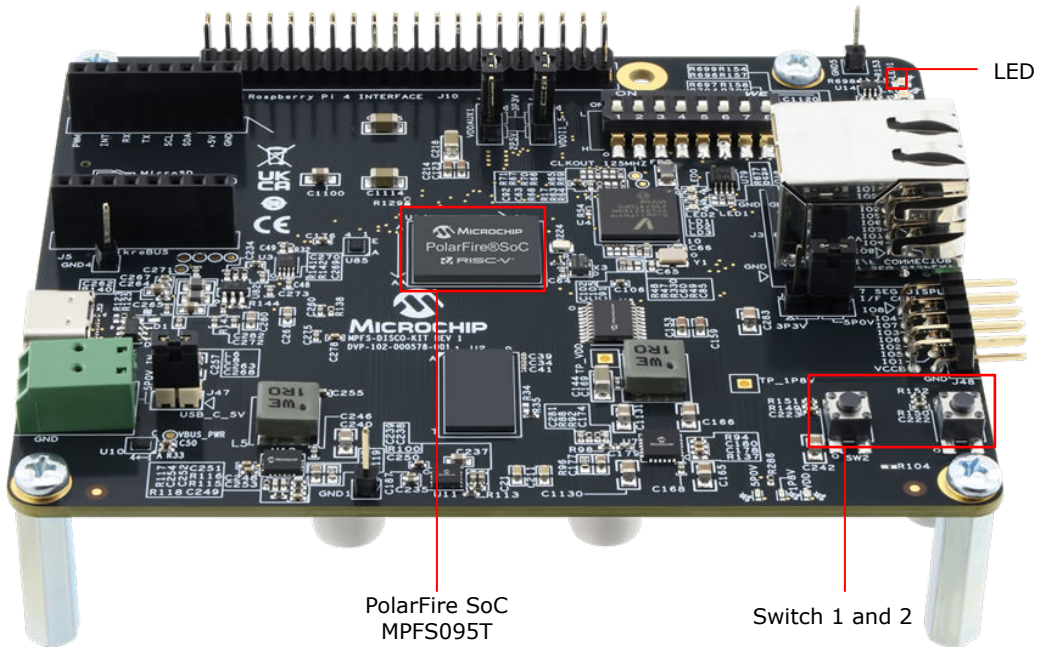
Figure 3-7. Running the Design Flow



4. Setting up the Demo Design (Ask a Question)

The following figure shows the PolarFire SoC Discovery Kit board.

Figure 4-1. PolarFire SoC Discovery Kit Board



The following steps describe how to setup the PolarFire SoC Discovery Kit to run the demo design:

1. Ensure that the board is powered OFF.
2. Before programming and powering up the PolarFire SoC Discovery board, ensure that the jumpers are positioned, as listed in the following table.

Table 4-1. Jumper Settings

Jumper	Location	Purpose	Settings
J45	Near the Raspberry Pi connector	Select the voltage for I/O bank 5 (Pin 1–2 for 3.3V)	1–2 installed
J46	Near the Raspberry Pi connector	Select the VDDAUX1 voltage • Pin 1–2 for 3.3V • Pin 2–3 for 2.5V	1–2 installed
J47	Near the power block	Select the power source for the board Pin 1–2 for board powered by USB Type C connector J4	1–2 installed
J49	Near the RJ45 connector	Jumper to select the voltage for the external 8-digit 7-segment display • Pin 1–2 installed for 3.3V • Pin 2–3 installed for 5.0V	1–2 installed

3. Connect the USB type-C cable between the J4 USB connector and the host PC.

5. Programming the Device (Ask a Question)

The FlashPro Express runs in batch mode to program the PolarFire SoC MPFS095T on the PolarFire SoC Discovery Kit board.

To program the device, follow these steps:

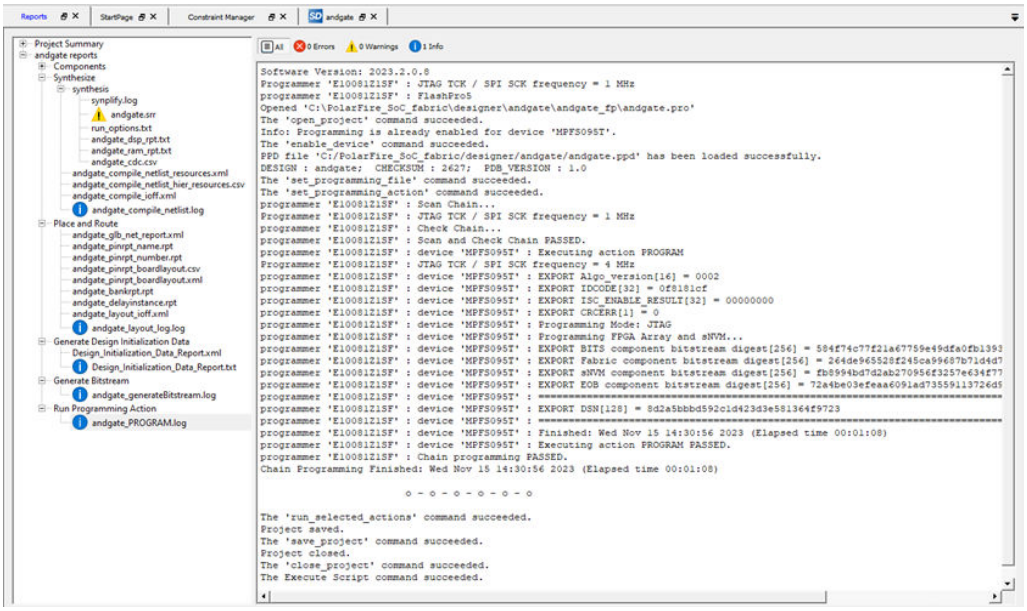
1. Install the FlashPro5 drivers if prompted. The drivers are in the `<Libero SoC v20232.2 Installation Directory>\Designer\fp_drivers` folder.
2. To generate the programming file and begin programming, expand **Program Design** in the **Design Flow** window, right-click **Run PROGRAM Action** and select **Run**.

FlashPro Express runs in batch mode and programs the device. Programming messages are visible in the Libero® SoC log window (programmer number may differ).

Important: Do not interrupt the programming sequence.

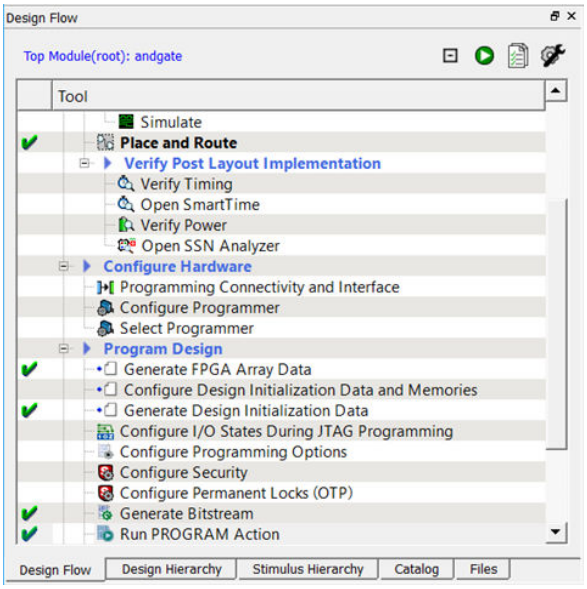
The following message must be visible in the **Reports View** under **Run PROGRAM Action** when the device is programmed successfully (programmer number may differ): `programmer 'E2007ZZUNS': Chain programming PASSED`.

Figure 5-1. Program Report



A green check mark appears next to the **Program Design** and **Run PROGRAM Action** in the **Design Flow** window to indicate programming completed successfully.

Figure 5-2. Design Flow Window



6. Running the Design (Ask a Question)

Follow the instructions to run the application:

1. Release Switch 1 and Switch 2 and observe the pattern of LED 1. LED1 must illuminate.
2. Press Switch 1 and observe the behavior of LED 1. It turns OFF.
3. Press Switch 2 and observe the behavior of LED 1. It turns OFF.
4. Press both the switches and LED 1 turns OFF.
5. Releasing the switch generates a logic one, which illuminates the LED. Invert the input signals to illuminate the LED when both switches are pressed.

7. Design Iterations in Libero SoC (Ask a Question)

Follow the instructions to iterate the design:

1. Reopen the **SmartDesign** Canvas by double-clicking **andgate** on the **Design Hierarchy** tab.
2. Select the **andgate** tab.
3. To bring up the menu, hold the CTRL key and select input ports A and B of AND2_0, and click the right mouse button. Select **Invert** to invert the signals. This is built into the SmartDesign capabilities to invert or Tie off any I/O.
4. Generate the Component. This resets the rest of the compilation functions but keeps the I/O constraints.
5. To run all the steps in between and reprogram the device, right-click **Run PROGRAM Action** on the **Design Flow** window and select **Update and Run**. If it seems to be taking a while, check to see if the **Warning** dialog box about running in non-Timing-driven mode is behind your active window.

Observe the correct behavior on the board by pressing both switches simultaneously to illuminate LED1.

8. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	07/2024	Updated the I/O Standard to "LVCMOS18" from "LVCMOS33" in step 3 of 3. Pin Assignments section
A	01/2024	Initial Revision

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