USBF1600

USB Firmware Memory

Features

- Read and Write Operations:
  - 2.7V-3.6V
- x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
- Firmware Memory Companion for the USB491X family of USB controllers
- Targeted for USB 2.0 High-Speed Infotainment Applications Including:
  - Integration with head unit systems
  - First, second and third row USB media hubs
  - Power delivery
- Memory Size:
  - 2 Mbyte (16 Mbit)
- High-Speed Clock Frequency:
  - 80 MHz maximum
- Superior Reliability:
  - Endurance: 100,000 cycles (minimum)
  - Greater than 100 years data retention
- Low-Power Consumption:
  - Active Read current: 15 mA (typical @ 80 MHz)
  - Standby Current: 15 µA (typical)
- Fast Erase Time:
  - Sector/Block Erase: 18 ms (typical), 25 ms (maximum)
  - Chip Erase: 35 ms (typical), 50 ms (maximum)
- Page Program:
  - 256 bytes per page in x1 or x4 mode
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
- Flexible Erase Capability:
  - Uniform 4-Kbyte sectors
  - Four 8-Kbyte top and bottom parameter overlay blocks
  - One 32-Kbyte top and bottom overlay blocks
  - Uniform 64-Kbyte overlay blocks
- Write Suspend:
  - Suspend Program or Erase operation to access another block/sector
- Software Reset (RST) mode
- Software Write Protection:
  - Individual Block Write Protection with permanent lockdown capability:
    - 64-Kbyte blocks, two 32-Kbyte blocks and eight 8-Kbyte parameter blocks
  - Read Protection on top and bottom 8-Kbyte parameter blocks
  - Security ID
  - One-Time-Programmable (OTP), 2-Kbyte Secure ID:
    - 64-bit unique, factory preprogrammed identifier
    - User-programmable area
- Temperature Range:
  - Extended: -40°C to +125°C
- All Devices are RoHS Compliant
- Automotive AEC-Q100 Grade 1 Qualified

Packages

- 8-Lead SOIC (3.90 mm)
- 8-Contact WDFN (6 mm x 5 mm)

Product Description

USBF1600, a USB Firmware memory chip, is a companion to the Microchip Automotive USB Smart Hub devices: USB491X. Factory preprogramming is available for custom firmware and configurations. The USBF1600 memory function assures proper functionality, providing for decreased development time and engineering resources and overall faster time to market.

The USB Firmware memory features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin count package.

USBF1600 is manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturing compared with alternate approaches.

See Figure 1-1 for pin assignments.

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1.0 PIN DESCRIPTIONS

FIGURE 1-1: PIN DESCRIPTIONS

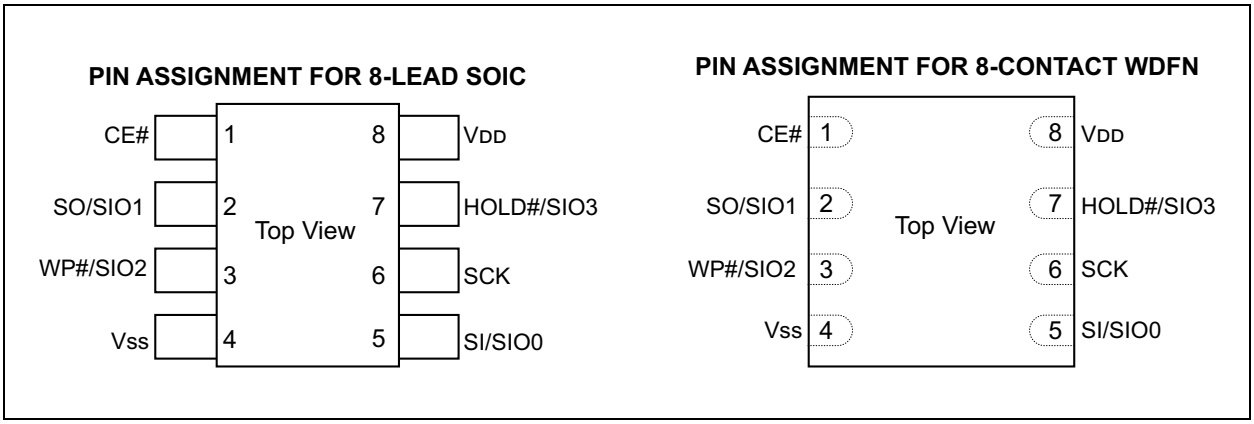


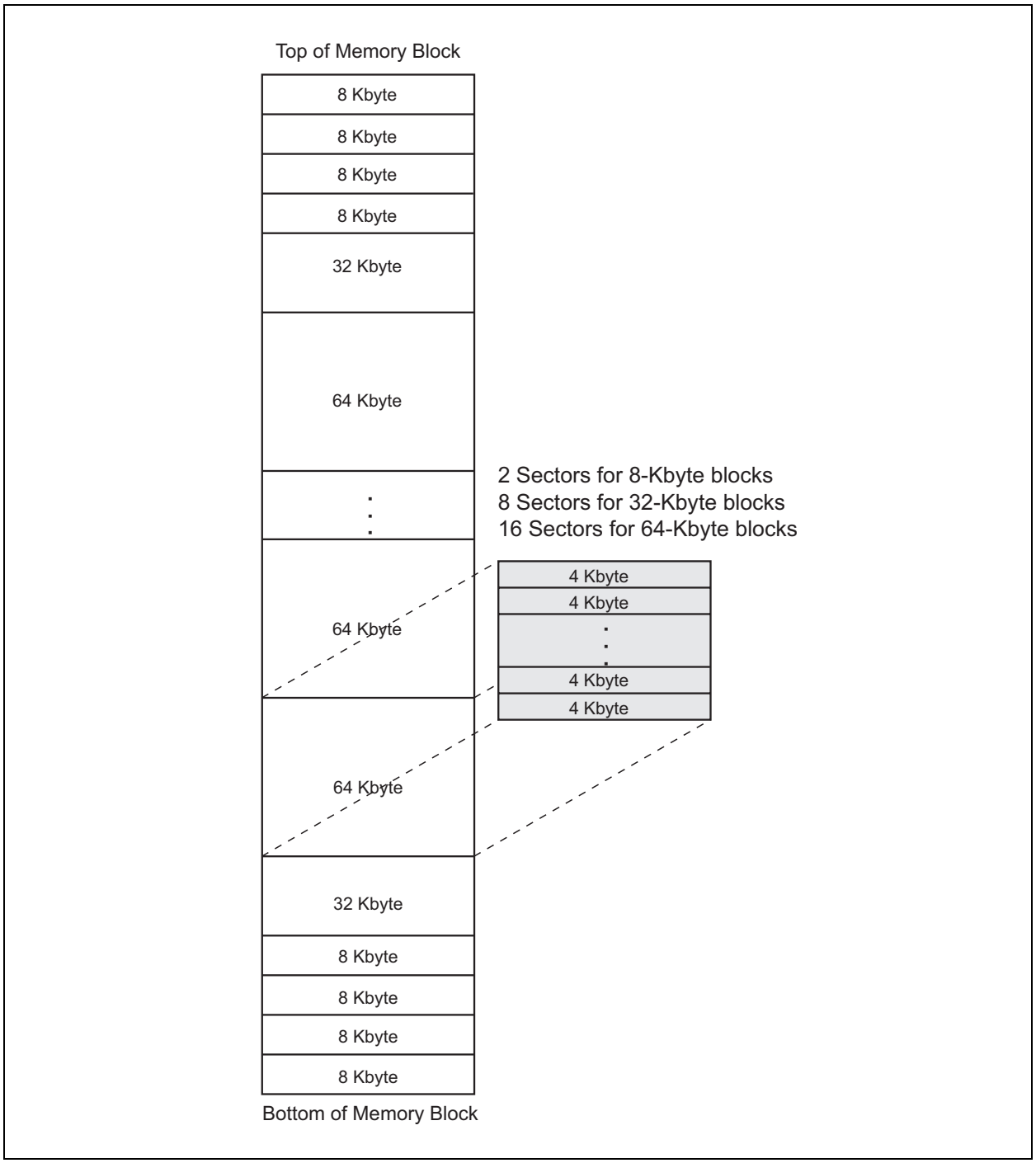
TABLE 1-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of write operations, for the command/data input sequence.
SO	Serial Data Output for SPI mode	Transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock. SO is the default state after a Power-on Reset.
SIO[3:0]	Serial Data Input/Output	Transfer commands, addresses or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data are shifted out on the falling edge of the serial clock. The Enable Quad I/O (EQIO) command instruction configures these pins for Quad I/O mode.
WP#	Write-Protect	The WP# is used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block Protection register. This pin only works in SPI, single-bit and dual-bit Read mode.
VSS	Ground	
SI	Serial Data Input for SPI mode	Transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a Power-on Reset.
SCK	Serial Clock	Provide the timing of the serial interface. Commands, addresses or input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single-bit and dual-bit Read mode and must be tied high when not in use.
VDD	Power Supply	Provide power supply voltage.

2.0 MEMORY ORGANIZATION

The USBF1600 SQI memory array is organized in uniform, 4-Kbyte erasable sectors with the following erasable blocks: eight 8-Kbyte parameter, two 32-Kbyte overlay and thirty 64-Kbyte overlay blocks (see Figure 2-1).

FIGURE 2-1: MEMORY MAP



3.0 DEVICE OPERATION

USBF1600 supports both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a Power-on Reset is SPI mode which supports multi-I/O (x1/x2/x4) Read/Write commands. A command instruction configures the device to SQI mode. The dataflow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address and data sequence.

The device supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus host is in standby mode and no data are being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) are sampled at the rising edge of the SCK clock signal for input and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as shown in Figure 3-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 3-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

FIGURE 3-1: SPI PROTOCOL

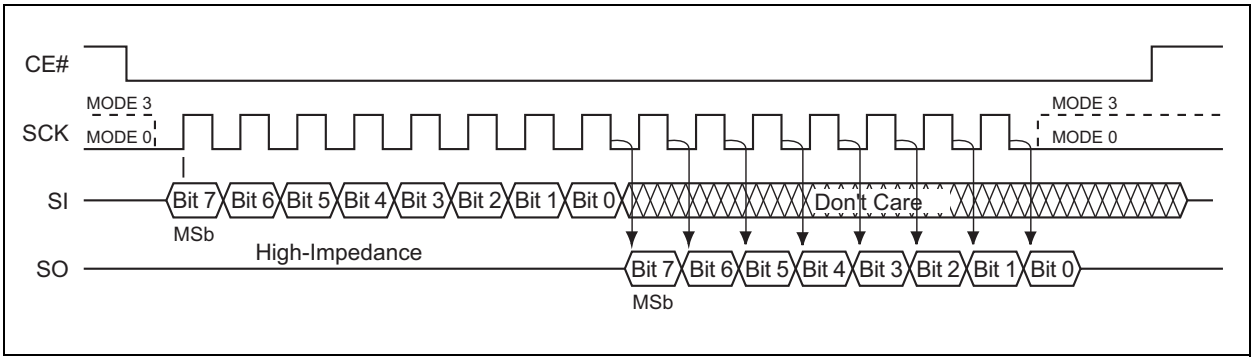
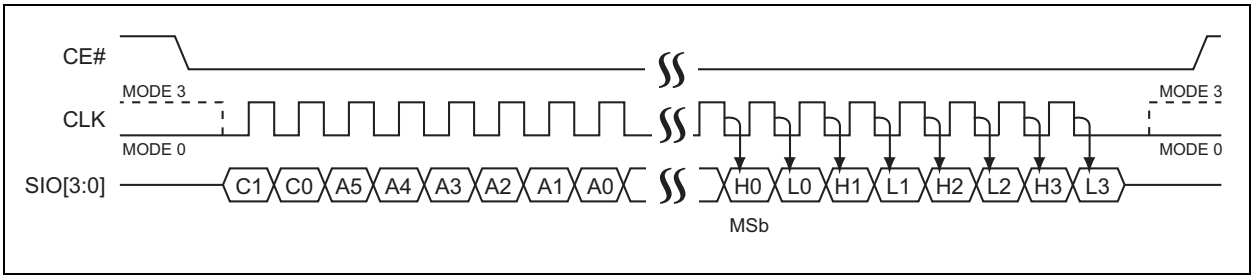


FIGURE 3-2: SERIAL QUAD I/O PROTOCOL



4.0 INSTRUCTIONS

Instructions are used to read, write (erase and program) and configure the USBF1600. The complete list of the instructions is provided in Table 4-1.

TABLE 4-1: DEVICE OPERATION INSTRUCTIONS FOR USBF1600

Instruction	Description	Command Cycle(1)	Mode		Address Cycle(s)(2,3)	Dummy Cycle(s)(3)	Data Cycle(s)(3)	Max Freq
			SPI	SQI				
Configuration								
NOP	No Operation	00H	X	X	0	0	0	80 MHz
RSTEN	Reset Enable	66H	X	X	0	0	0	
RST(4)	Reset Memory	99H	X	X	0	0	0	
EQIO	Enable Quad I/O	38H	X		0	0	0	
RSTQIO(5)	Reset Quad I/O	FFH	X	X	0	0	0	
RDSR	Read STATUS Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
WRSR	Write STATUS Register	01H	X	X	0	0	2	
RDCR	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
Read	Read Memory	03H	X		3	0	1 to ∞	40 MHz
High-Speed Read	Read Memory at Higher Speed	0BH		X	3	3	1 to ∞	80 MHz
			X		3	1	1 to ∞	
SQOR(6)	SPI Quad Output Read	6BH	X		3	1	1 to ∞	
SQIOR(7)	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
SDOR(8)	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
SDIOR(9)	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	
SB	Set Burst Length	C0H	X	X	0	0	1	
RBSQI	SQI Read Burst with Wrap	0CH		X	3	3	n to ∞	
RBSPI(7)	SPI Read Burst with Wrap	ECH	X		3	3	n to ∞	

Note 1: Command cycle is two-clock periods in SQI mode and eight-clock periods in SPI mode.

2: Address bits above the Most Significant bit of each density can be VIL or VIH.

3: Address, Dummy/Mode bits and Data cycles are two-clock periods in SQI and eight-clock periods in SPI mode.

4: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

5: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.

6: Data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

7: Address, Dummy/Mode bits and data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

8: Data cycles are four-clock periods.

9: Address, Dummy/Mode bits and Data cycles are four-clock periods.

10: Sector Addresses: Use AMS - A12, remaining address are don't care, but must be set to VILor VIH.

11: Blocks are 64 KByte, 32 KByte or 8KByte, depending on location. Block Erase Address: AMS - A16 for 64 Kbyte; AMS - A15 for 32 Kbyte; AMS - A13 for 8 Kbyte. Remaining addresses are don't care, but must be set to VIL or VIH.

TABLE 4-1: DEVICE OPERATION INSTRUCTIONS FOR USBF1600 (CONTINUED)

Instruction	Description	Command Cycle(1)	Mode		Address Cycle(s)(2,3)	Dummy Cycle(s)(3)	Data Cycle(s)(3)	Max Freq
			SPI	SQI				
Identification								
JEDEC-ID	JEDEC-ID Read	9FH	X		0	0	3 to ∞	80 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
SFDP	Serial Flash Discoverable Parameters	5AH	X		3	1	1 to ∞	
Write								
WREN	Write Enable	06H	X	X	0	0	0	80 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
SE(10)	Erase 4 Kbytes of Memory Array	20H	X	X	3	0	0	
BE(11)	Erase 64, 32 or 8 Kbytes of Memory Array	D8H	X	X	3	0	0	
CE	Erase Full Array	C7H	X	X	0	0	0	
PP	Page Program	02H	X	X	3	0	1 to 256	
SPI Quad PP(6)6	SQI Quad Page Program	32H	X		3	0	1 to 256	
WRSU	Suspends Program/Erase	B0H	X	X	0	0	0	
WRRE	Resumes Program/Erase	30H	X	X	0	0	0	

Note 1: Command cycle is two-clock periods in SQI mode and eight-clock periods in SPI mode.

2: Address bits above the Most Significant bit of each density can be VIL or VIH.

3: Address, Dummy/Mode bits and Data cycles are two-clock periods in SQI and eight-clock periods in SPI mode.

4: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

5: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.

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TABLE 4-1: DEVICE OPERATION INSTRUCTIONS FOR USBF1600 (CONTINUED)

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2,3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
Protection								
RBPR	Read Block Protection Register	72H	X		0	0	1 to 6	80 MHz
				X	0	1	1 to 6	
WBPR	Write Block Protection Register	42H	X	X	0	0	1 to 6	
LBPR	Lock Down Block Protection Register	8DH	X	X	0	0	0	
nVWLDR	Nonvolatile Write Lockdown Register	E8H	X	X	0	0	1 to 6	
ULBPR	Global Block Protection Unlock	98H	X	X	0	0	0	
RSID	Read Security ID	88H	X		2	1	1 to 2048	
				X	2	3	1 to 2048	
PSID	Program User Security ID area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	
Power Saving								
DPD	Deep Power-Down Mode	B9H	X	X	0	0	0	80 MHz
RDPD	Release from Deep Power-Down and Read ID	ABH	X	X	3	0	1 to ∞	

Note 1: Command cycle is two-clock periods in SQI mode and eight-clock periods in SPI mode.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: Address, Dummy/Mode bits and Data cycles are two-clock periods in SQI and eight-clock periods in SPI mode.

4: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

5: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.

6: Data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

7: Address, Dummy/Mode bits and data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

8: Data cycles are four-clock periods.

9: Address, Dummy/Mode bits and Data cycles are four-clock periods.

10: Sector Addresses: Use AMS - A12, remaining address are don't care, but must be set to V_{IL}or V_{IH}.

11: Blocks are 64 KByte, 32 KByte or 8KByte, depending on location. Block Erase Address: AMS - A16 for 64 Kbyte; AMS - A15 for 32 Kbyte; AMS - A13 for 8 Kbyte. Remaining addresses are don't care, but must be set to V_{IL} or V_{IH}.

5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD} + 0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD} + 2.0V

Package power dissipation capability (T_A = +25°C) 1.0W

Surface mount solder reflow temperature ..... +260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 5-1: OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Extended	-40°C to +125°C	2.7V-3.6V

TABLE 5-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
3 ns	C_L = 30 pF

Note 1: See Figure 7-5.

5.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 5-3 and Figure 5-1 for more information.

When V_{DD} drops from the operating voltage to below the minimum V_{DD} threshold at power-down, all operations are disabled and the device does not respond to commands. Data corruption may result if a power-down occurs while a Write Registers, program or erase operation is in progress (see Figure 5-2).

TABLE 5-3: RECOMMENDED SYSTEM POWER-UP/DOWN TIMINGS

Symbol	Parameter	Minimum	Maximum	Units	Condition
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	100	—	µs	
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	100	—	µs	
T_{PD}[1]	Power-down Duration	100	—	ms	
V_{OFF}	V_{DD} off time	—	0.3	V	0V recommended

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

FIGURE 5-1: POWER-UP TIMING DIAGRAM

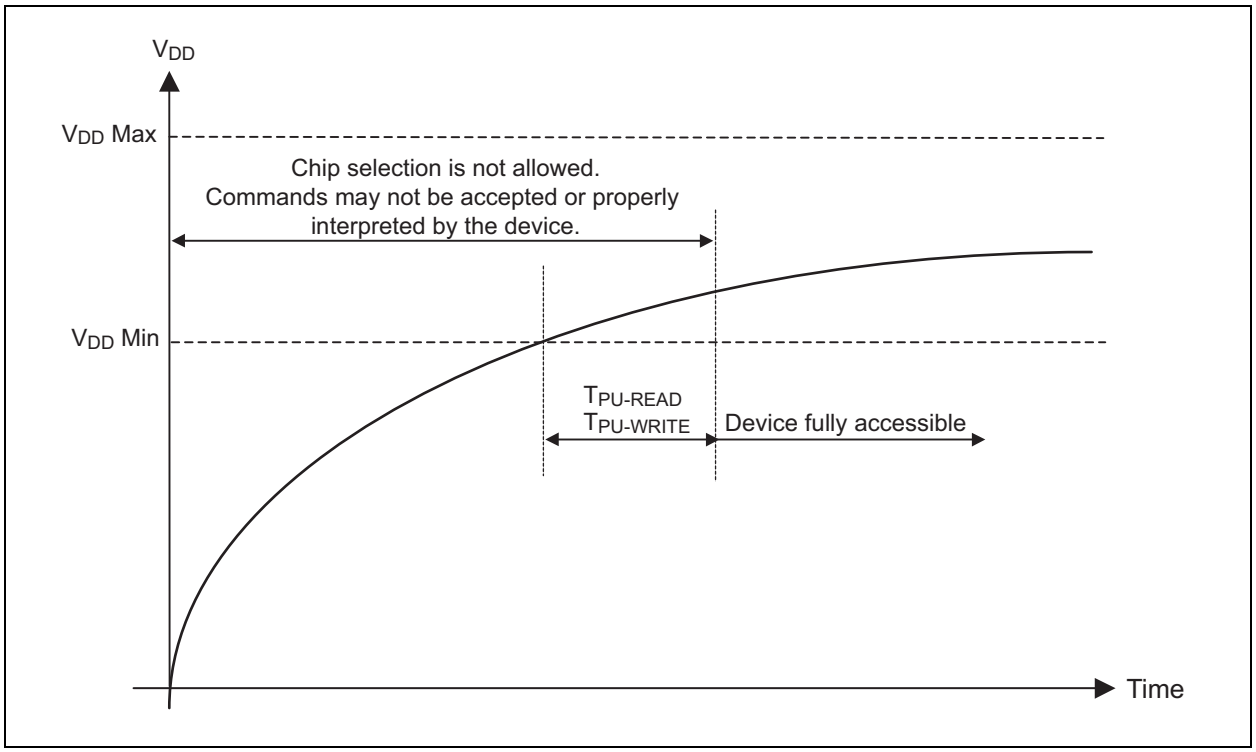
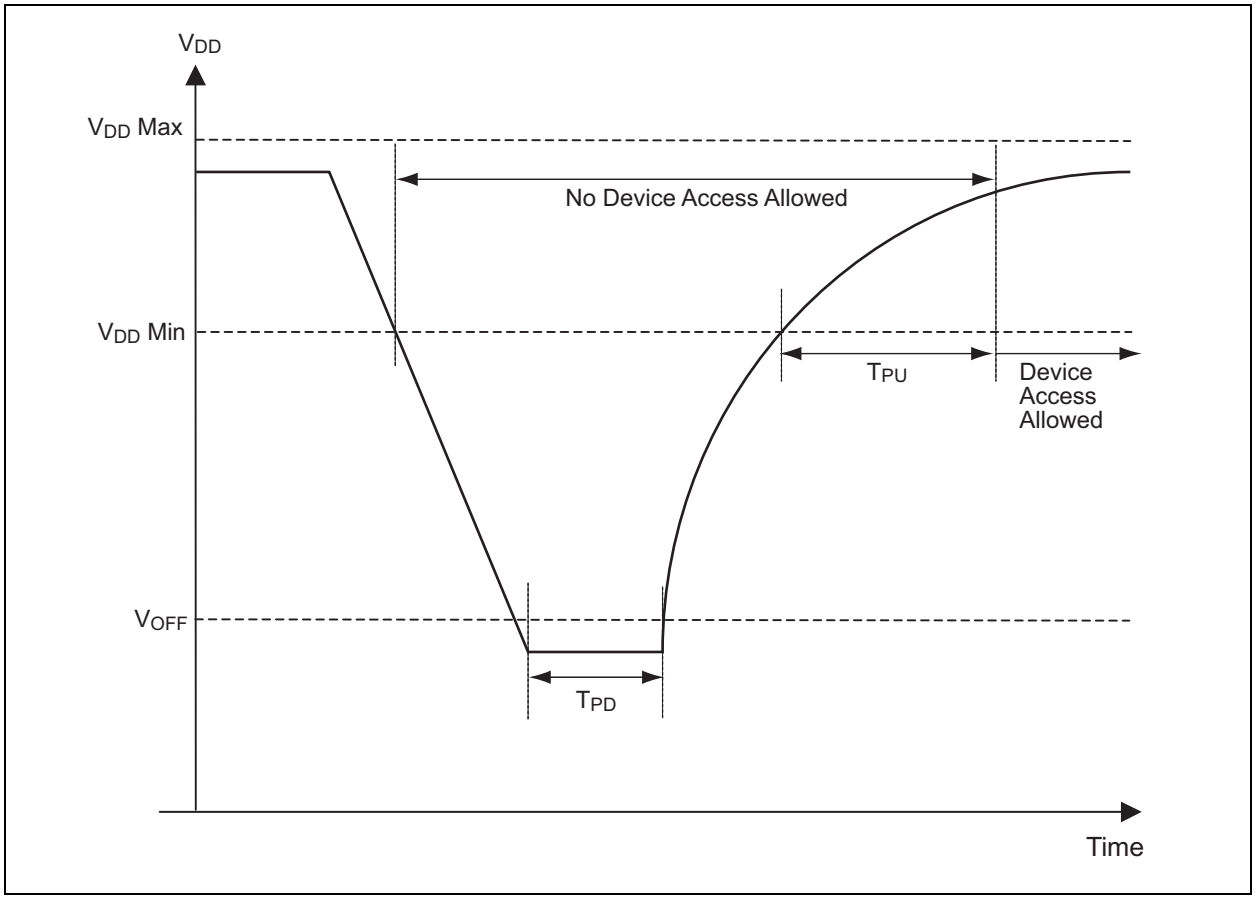


FIGURE 5-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM



6.0 DC CHARACTERISTICS

TABLE 6-1: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions
		Minimum	Typical	Maximum	Units	
I_{DDR1}	Read Current	—	8	15	mA	V_{DD} = V_{DD} Max, CE# = 0.1 V_{DD}/0.9 V_{DD} @ 40 MHz, SO = open
I_{DDR2}	Read Current	—	—	20	mA	V_{DD} = V_{DD} Max, CE# = 0.1 V_{DD}/0.9 V_{DD} @ 80 MHz, SO = open
I_{DDW}	Program and Erase Current	—	—	25	mA	V_{DD} Max
I_{SB}	Standby Current	—	15	45	µA	CE# = V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{DPD}	Deep Power-Down Current	—	8	25	µA	CE# = V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{LI}	Input Leakage Current	—	—	2	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current	—	—	2	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low Voltage	—	—	0.8	V	V_{DD} = V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}	—		V	V_{DD} = V_{DD} Max
V_{OL}	Output Low Voltage		—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2	—	—	V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min

TABLE 6-2: CAPACITANCE (T_A = +25°C, F = 1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	8 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]1	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR1}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH1}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-4: WRITE TIMING PARAMETERS

Symbol	Parameter	Minimum	Maximum	Units
T_{SE}	Sector Erase	—	25	ms
T_{BE}	Block Erase	—	25	ms
T_{SCE}	Chip Erase	—	50	ms
T_{PP}[1]	Page Program	—	1.5	ms
T_{PSID}	Program Security ID	—	1.5	ms

Note 1: Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes).

TABLE 6-4: WRITE TIMING PARAMETERS (CONTINUED)

Symbol	Parameter	Minimum	Maximum	Units
TWS	Write Suspend Latency	—	25	µs
TWPEN	Write Protection Enable Bit Latency	—	25	ms

Note 1: Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes).

7.0 AC CHARACTERISTICS

TABLE 7-1: AC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits - 40 MHz		Limits - 80 MHz		Units
		Min.	Max.	Min.	Max.	
FCLK	Serial Clock Frequency	—	40	—	80	MHz
TCLK	Serial Clock Period	—	25	—	12.5	ns
TSCKH	Serial Clock High Time	11	—	5.5	—	ns
TSCKL	Serial Clock Low Time	11	—	5.5	—	ns
TSCKR(1)	Serial Clock Rise Time (slew rate)	0.1	—	0.1	—	V/ns
TSCKF1(1)	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	V/ns
TCES(2)	CE# Active Setup Time	8	—	5	—	ns
TCEH(2)	CE# Active Hold Time	8	—	5	—	ns
TCHS(2)	CE# Not Active Setup Time	8	—	5	—	ns
TCHH(2)	CE# Not Active Hold Time	8	—	5	—	ns
TCPH	CE# High Time	25	—	12.5	—	ns
TCHZ	CE# High to High-Z Output	—	19	—	12.5	ns
TCLZ	SCK Low to Low-Z Output	0	—	0	—	ns
THLS	HOLD# Low Setup Time	8	—	5	—	ns
THHS	HOLD# High Setup Time	8	—	5	—	ns
THLH	HOLD# Low Hold Time	8	—	5	—	ns
THHH	HOLD# High Hold Time	8	—	5	—	ns
THZ	HOLD# Low-to-High-Z Output	—	8	—	8	ns
TLZ	HOLD# High-to-Low-Z Output	—	8	—	8	ns
TDS	Data In Setup Time	3	—	3	—	ns
TDH	Data In Hold Time	4	—	4	—	ns
TOH	Output Hold from SCK Change	0	—	0	—	ns
TV	Output Valid from SCK	—	8/5(3)	—	8/5(3)	ns

Note 1: Maximum Rise and Fall time may be limited by TSCKH and TSCKL requirements.

2: Relative to SCK.

3: 30 pF/10 pF

FIGURE 7-1: HOLD TIMING DIAGRAM

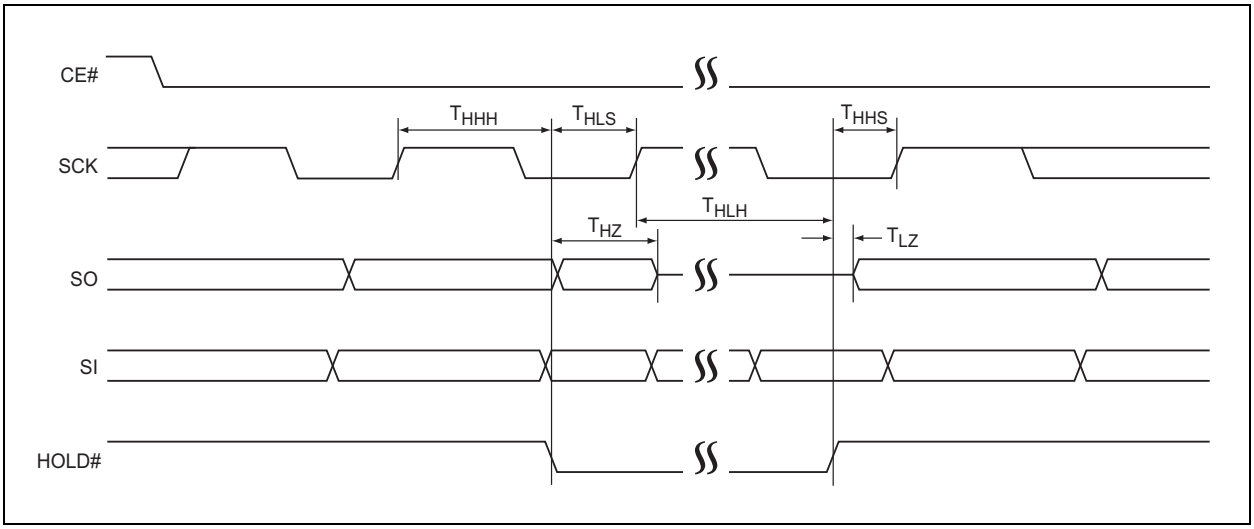


FIGURE 7-2: SERIAL INPUT TIMING DIAGRAM

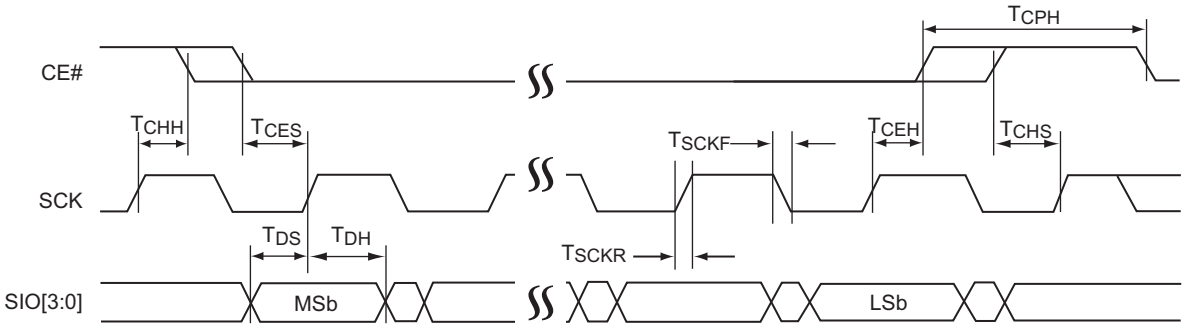


FIGURE 7-3: SERIAL OUTPUT TIMING DIAGRAM

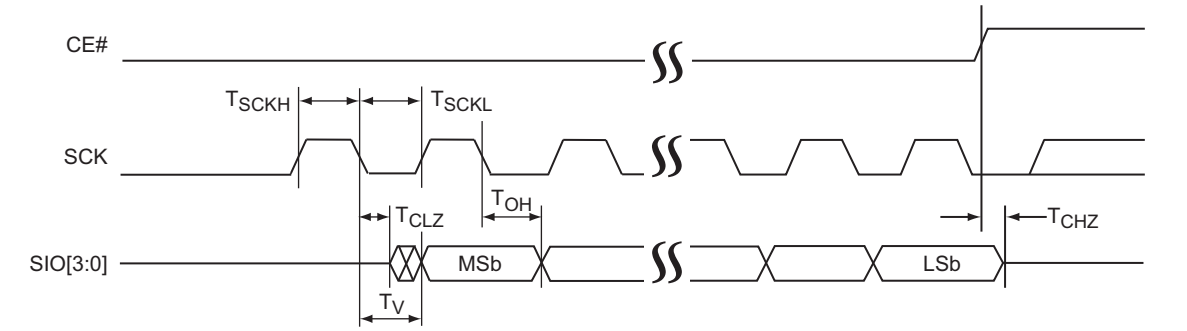
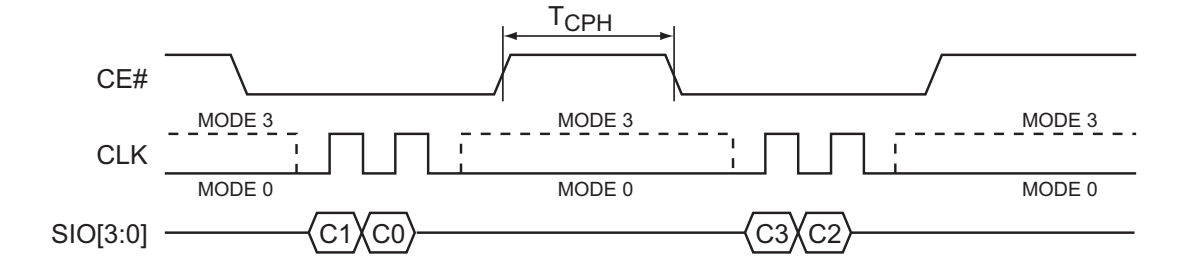


TABLE 7-2: RESET TIMING PARAMETERS

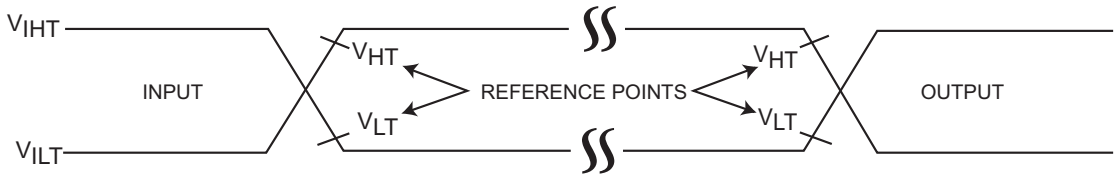
$T_{R(i)}$	Parameter	Minimum	Maximum	Units
TR(O)	Reset to Read (non-data operation)	—	20	ns
TR(P)	Reset Recovery from Program or Suspend	—	100	µs
TR(E)	Reset Recovery from Erase	—	1	ms

FIGURE 7-4: RESET TIMING DIAGRAM



Note: C[1:0] = 66H; C[3:2] = 99H

FIGURE 7-5: AC INPUT/OUTPUT REFERENCE WAVEFORMS



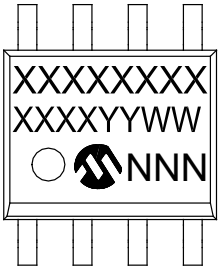
Note 1: AC test inputs are driven at VIHT (0.9VDD) for a logic '1' and VILT (0.1VDD) for a logic '0'. Measurement reference points for inputs and outputs are VHT (0.6V_{DD}) and VLT (0.4VDD). Input rise and fall times (10% ↔ 90%) are <3 ns.

2: VHT- VHIGH Test
VLT - VLOW Test
VIHT - VINPUT HIGH Test
VILT - VINPUT LOW Test

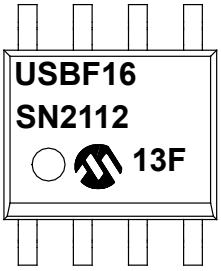
8.0 PACKAGING INFORMATION

8.1 Package Marking

8-Lead SOIC (3.90 mm)

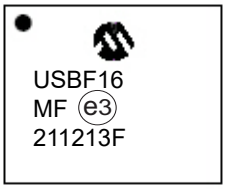


Example



8-Contact WDFN (5x6 mm)

Example



Part Number	1st Line Marking Codes	
	SOIC	WDFN
USBF1600	USBF16	USBF16

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

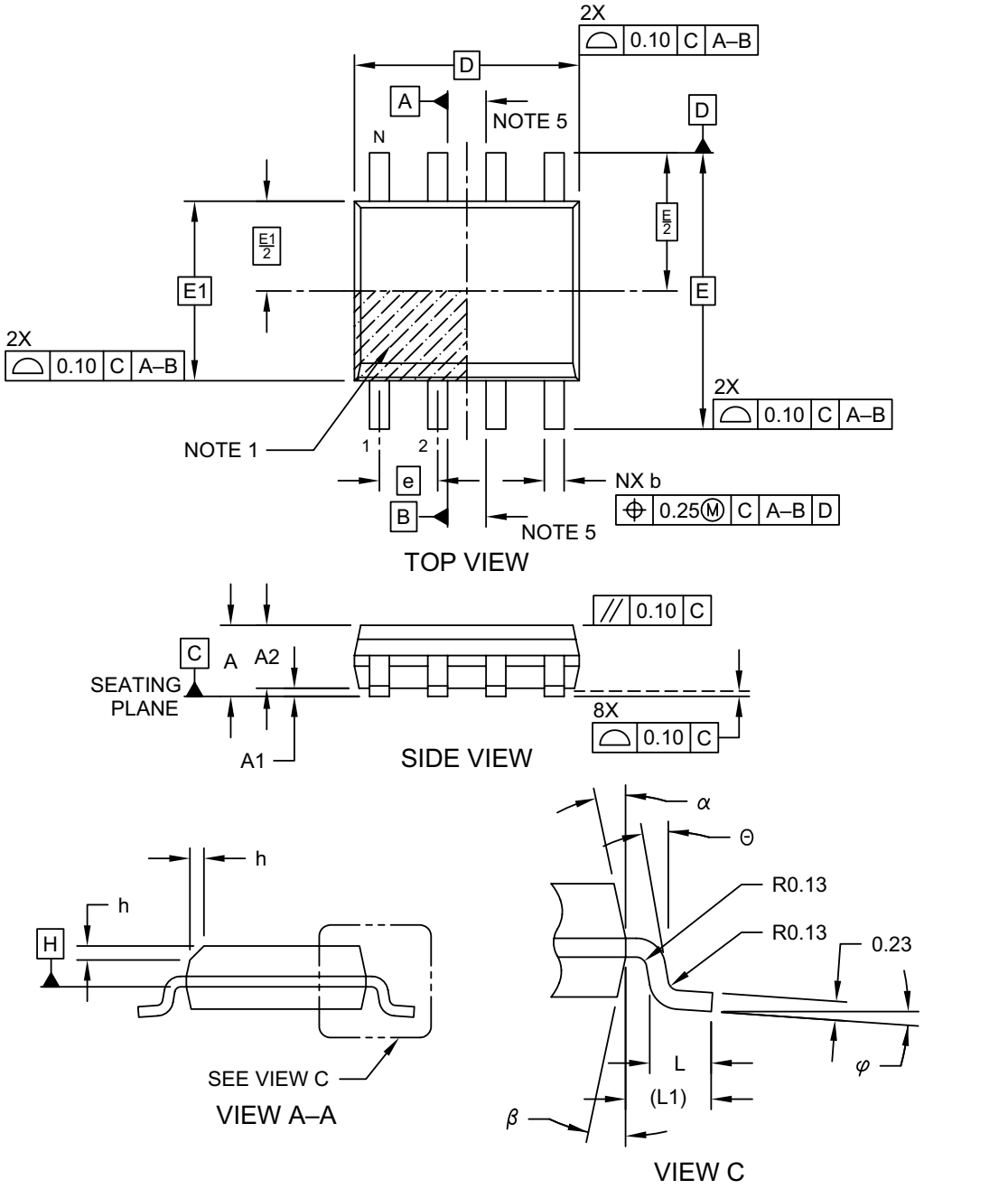
Note: For very small packages with no room for the Pb-free JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8.2 Packaging Diagrams

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

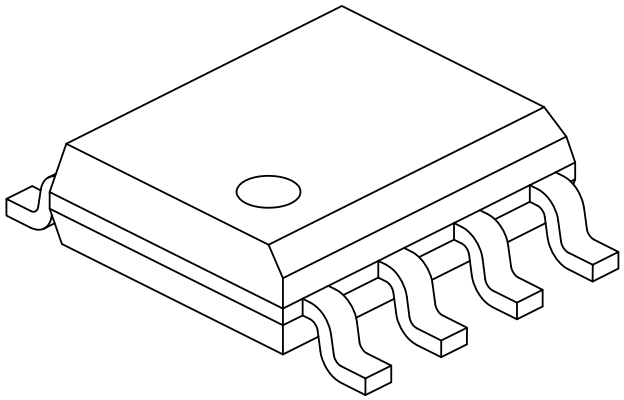
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

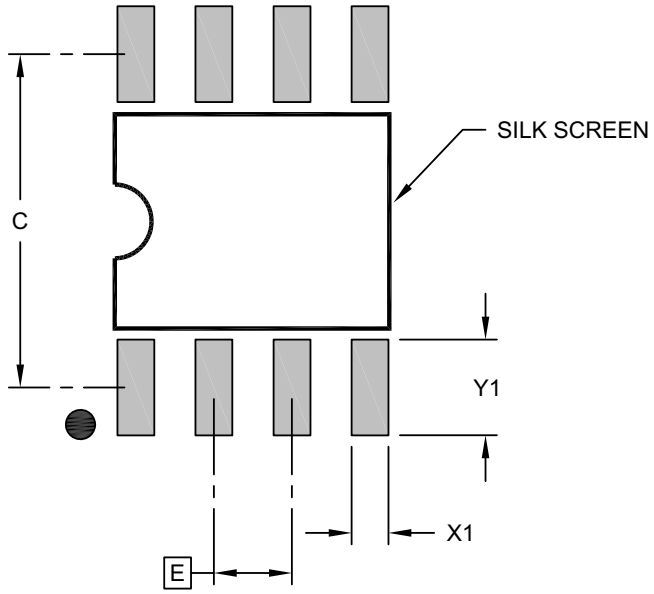
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

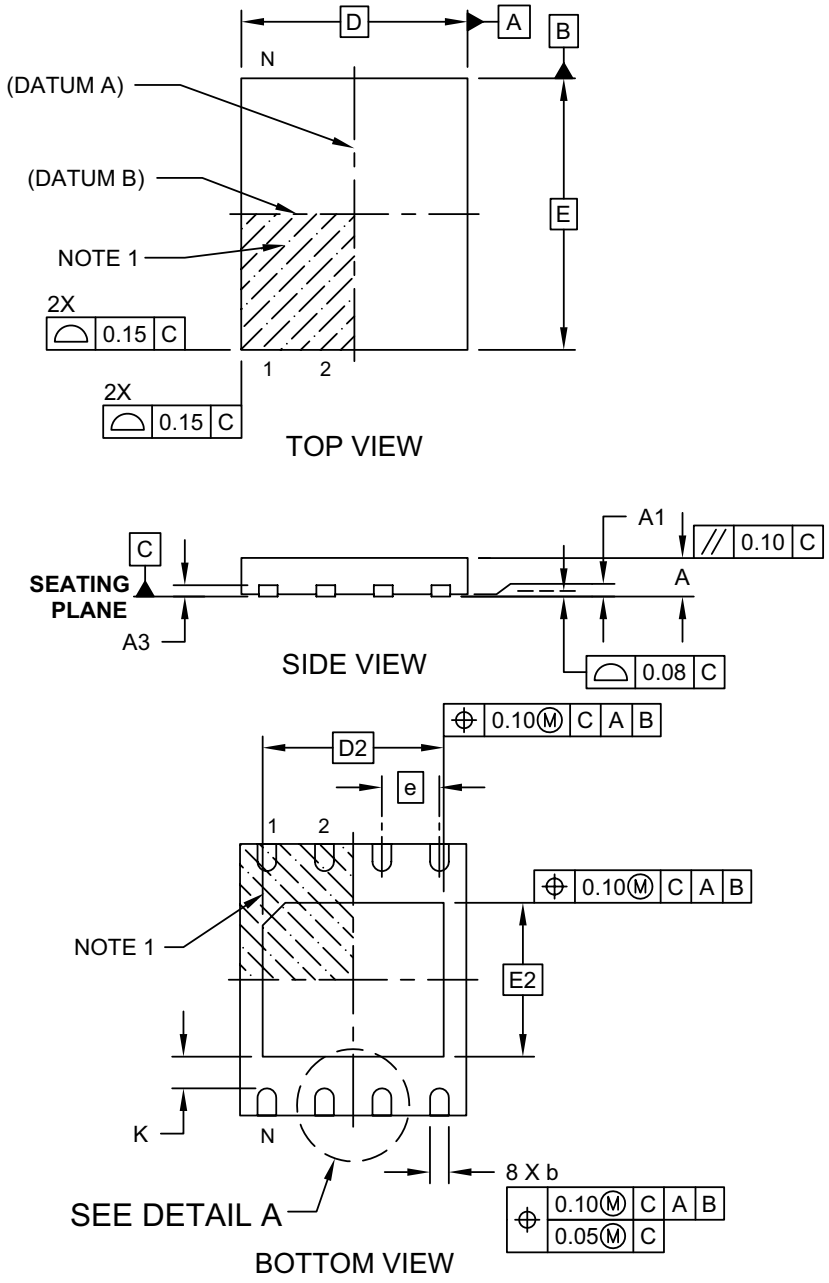
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

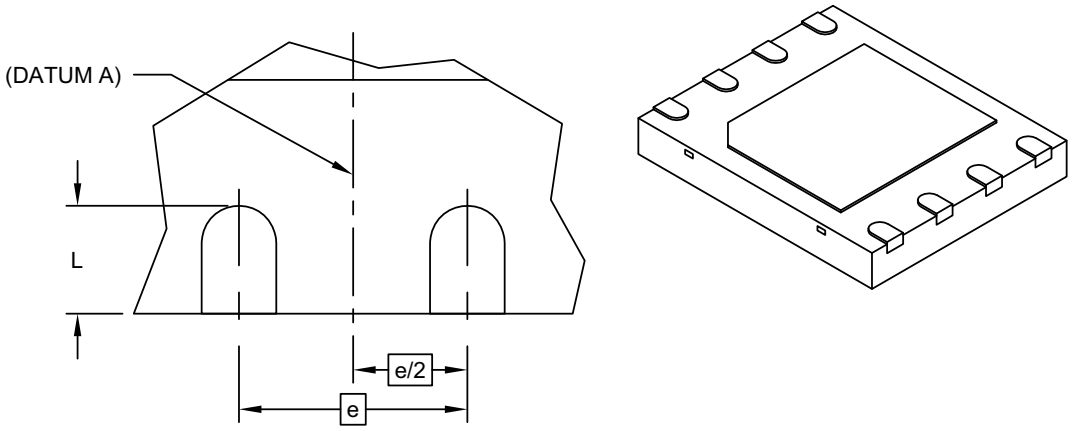
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-210B Sheet 1 of 2

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	D		5.00 BSC	
Exposed Pad Width	D2		4.00 BSC	
Overall Length	E		6.00 BSC	
Exposed Pad Length	E2		3.40 BSC	
Terminal Width	b	0.35	0.42	0.48
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

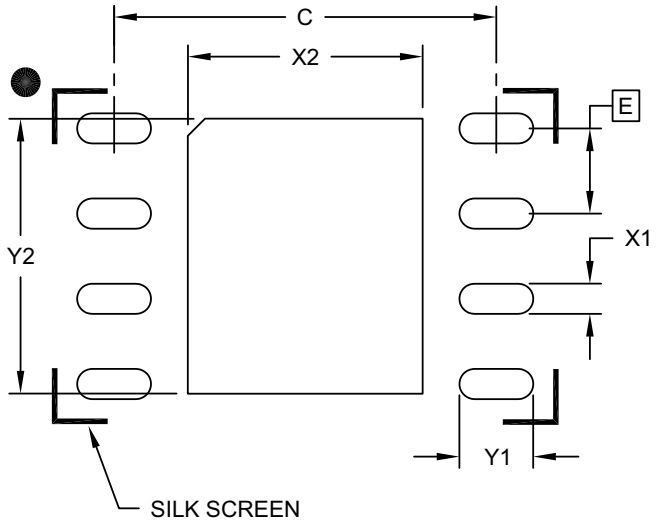
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-210B Sheet 2 of 2

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.50
Optional Center Pad Length	Y2			4.10
Contact Pad Spacing	C		5.70	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2210A

9.0 REVISION HISTORY

Revision B (July 2021)

Updated the marking information; Updated SOIC and WDFN package drawings.

Revision A (December 2018)

Initial release of the document.

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PART NO.	[X](1)	–X	/XX	XXX(3,4)
Device	Tape and Reel Indicator	Temperature Range	Package	Variant

Device:	USBF1600	=	USB Firmware Memory
Tape and Reel Indicator:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel(1)
Temperature Range:	E	=	-40°C to + 125°C (AEC-Q100 Grade 1)
Package:	SN	=	SOIC (3.90 mm Body), 8-Lead
	MF	=	WDFN (6 mm x 5 mm Body), 8-Contact
Variant(3,4):	VAO	=	Standard Automotive
	XXX/VXX	=	Customer-Specific Automotive

Valid Combinations(2):

a) USBF1600T-E/SNVAO
b) USBF1600T-E/MFVAO

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Customer-specific part numbers are not listed.

3: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

4: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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