APPLICATION NOTE

SAMA5D3 Layout Recommendations

Atmel | SMART SAMA5D3 Series

Introduction

The Atmel® | SMART SAMA5D3 series is based on the ARM® Cortex®-A5 processor. This series of embedded microprocessor units (eMPU) operates at up to 536 MHz and integrates various peripherals and communication interfaces in one chip, thereby increasing the complexity of the Printed Circuit Board (PCB).

How to place components and route critical traces while preserving the signal integrity constitutes a challenge for any hardware engineer. This document provides a few layout recommendations for some critical components in the SAMA5D3 platform.

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1. Stack-up Design

As a general rule, PCB layouts are easier to design when more layers are used – but at a higher cost.

The general stack-up for the SAMA5D3 board includes eight or ten layers. The most common stack arrangements of 8-layer and 10-layer models used in our designs are listed below. Other arrangements can be used, depending on the design complexity and as required to preserve the signal integrity.

8-layer model:

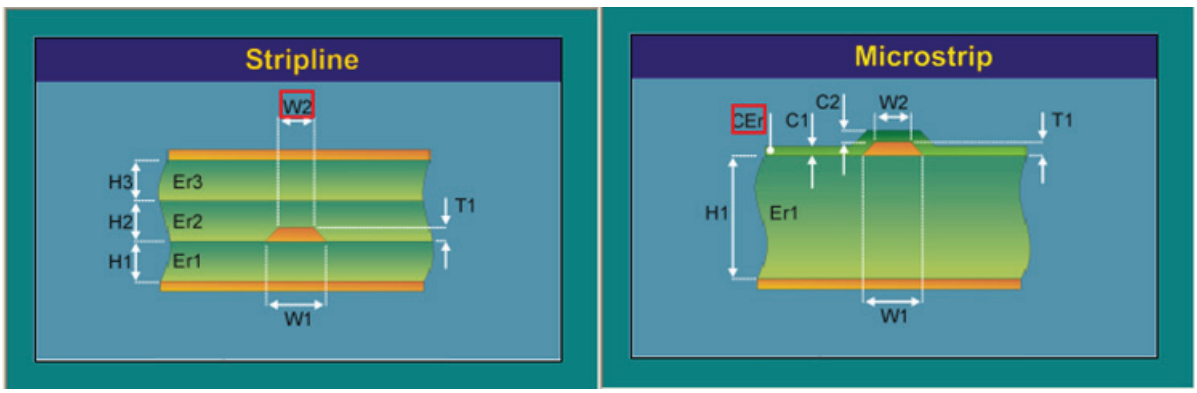
- Layer 1 — Signal (Microstrip), component side
- Layer 2 — Ground plane
- Layer 3 — Signal (Stripline)
- Layer 4 — Power plane
- Layer 5 — Ground plane
- Layer 6 — Signal (Stripline)
- Layer 7 — Ground plane
- Layer 8 — Signal (Microstrip)

10-layer model:

- Layer 1 — Signal (Microstrip), component side
- Layer 2 — Ground plane
- Layer 3 — Signal (Stripline)
- Layer 4 — Signal (Stripline)
- Layer 5 — Ground plane
- Layer 6 — Power plane
- Layer 7 — Signal (Stripline)
- Layer 8 — Signal (Stripline)
- Layer 9 — Ground plane
- Layer10 — Signal (Microstrip)

Stripline and Microstrip are “transmission line” routing approaches that take the neighboring power planes and PCB dielectric characteristics into consideration in order to achieve impedance-controlled traces that are determined by the layer’s parameters (both copper and dielectric). The impedance can be computed by software based on parametric inputs.

Figure 1-1. Stripline and Microstrip Implementations



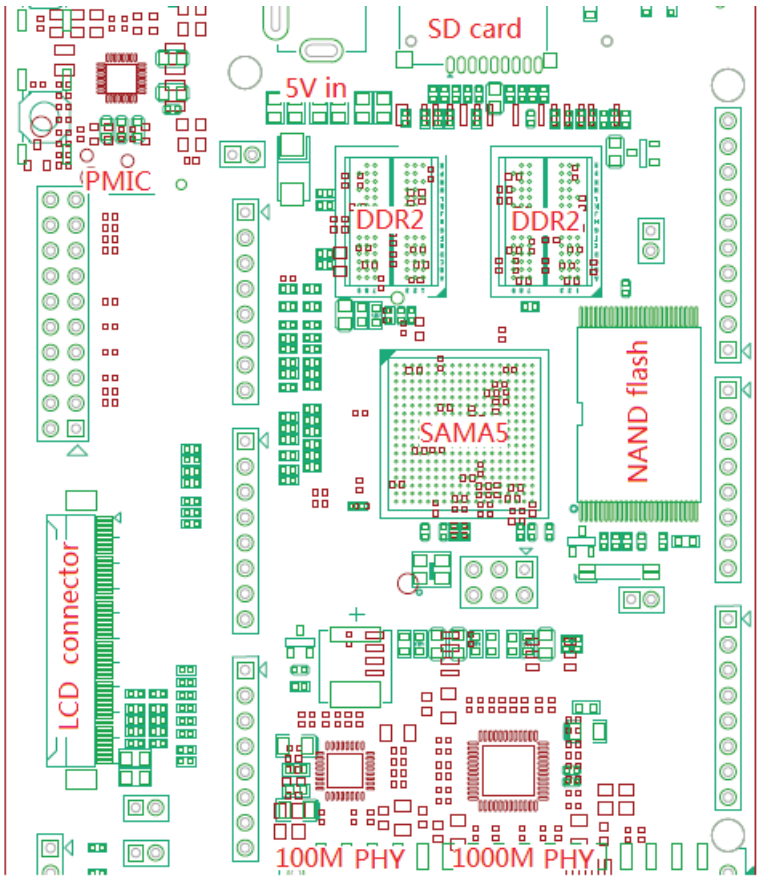
2. Layout

2.1 Board Layout Example

Figure 2-1 shows an example of a PCB layout for a basic SAMA5D3 system.

- Power Management IC (PMIC): At the top-left corner of the PCB
- Two 16-bit DDR2 chips: Above the SAMA5D3, and parallel to each other
- NAND Flash: On the right side of SAMA5D3
- 100M Ethernet PHY and 1000M Ethernet PHY: Below the SAMA5D3
- LCD connector: On the left edge of the PCB

Figure 2-1. SAMA5D3-XPLD PCB Layout Example



2.2 General Board Layout Strategies

Some general layout strategies for an SAMA5D3 board are listed below:

- First place the connectors of the board and any other item having compulsory mechanical and location constraints; lock them on your layout so that any further displacement is made impossible.
- Place the DDR2, Flash memory and oscillator parts as a first-level priority. The traces should be as short as possible with a minimum number of vias.
- Place the SD card, Ethernet PHY and LCD/ISI parts as a second-level priority.
- Place components of the same function circuit close together, and keep a clearance from other circuits.
- Place the decoupling capacitors (0.1 µF or smaller) as close as possible to each IC power pin, and place the bulk capacitors (1 µF or larger) properly on the PCB to charge the decoupling capacitors.

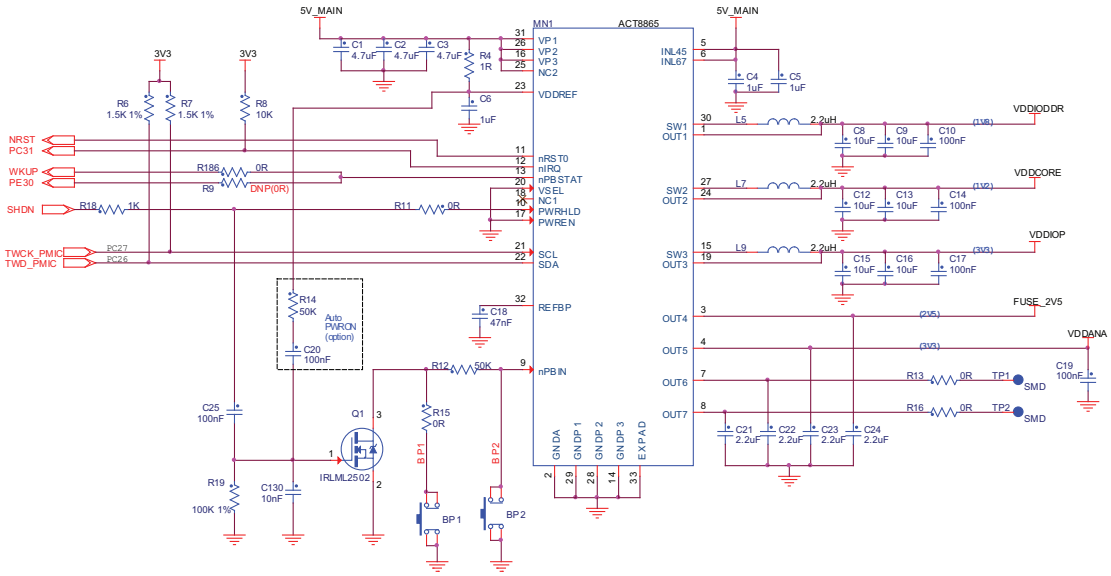
- As far as possible, avoid splitting ground planes, and avoid routing signals above the splits in ground planes, as that is a major source of Electro-Magnetic Interference (EMI).

3. Critical Layout Recommendations

3.1 Power Management IC

A Power Management IC (PMIC) integrates several DCDC and LDO controllers in one chip and manages all the system power rails and their sequencing. The PMIC needs several external components such as inductors, capacitors and resistors. Figure 3-1 shows a typical implementation of a PMIC.

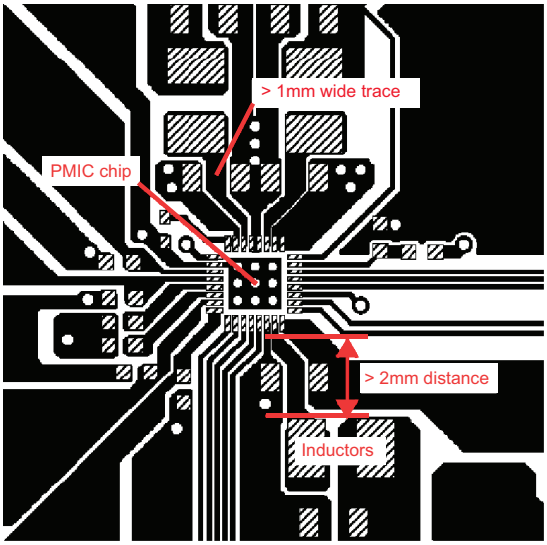
Figure 3-1. PMIC Schematic Example



The DCDC inductors must be close to the PMIC output pins. The inductors will produce heat while the DCDC controller is operating. The PMIC is typically surrounded by three inductors; a sufficient air gap (at least 2 mm) must be reserved around each one of them to evacuate the heat.

The power traces should be wide enough for the current load. A minimum width of 20 mil is recommended (a 1-A current needs at least a 1-mm width). Generally, these traces should be enlarged after they fan out from the PMIC. Figure 3-2 shows an example of a PMIC circuit layout.

Figure 3-2. PMIC Layout Example



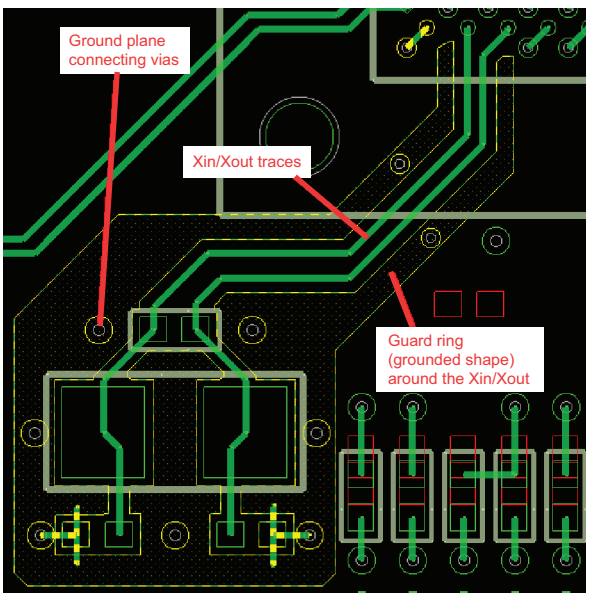
3.2 Clock

SAMA5D3 devices include two clock inputs: A slow clock input and a main clock input. In most cases, one crystal and two load capacitors are required for each input. A ground plane should be positioned under the crystal. It is recommended to shield the oscillator nets and pads with a ground ring connected to the board ground plane through several vias.

The crystal XIN/XOUT are signals of very low amplitude and high impedance; therefore, they must be particularly “protected" to ensure signal integrity. For this purpose, place the crystal part as close as possible to the MPU XIN/XOUT pins, and position a grounded ring around the XIN/XOUT nets, as close as possible to the IC pins.

Do not add vias at the end of the guard ground ring that is close to the XIN/XOUT pins.

Figure 3-3. Clock Layout Example



3.3 Dynamic RAM Memory

SAMA5D3 devices support several types of dynamic RAM memory, including DDR2, LPDDR2 and LPDDR1. Currently, the most commonly used memory type is DDR2.

The DDR2 controller interface includes:

- Four data lanes: DQS[3:0], DQSN[3:0], DM[3:0], DQ[31:0]
- ADDR/CMD/CTL signals: BA[2:0], A[13:0], RAS/CAS, CS, CKE, WE
- Clock signals: CK/CKn

Here are some recommendations for the data lane signal layout:

- In each data lane (e.g. lane0 includes DQ[7:0]/DM0/DQS0), the length difference between each signal and the respective DQS/DQSn signal should not exceed 100 mil.
- It is recommended to route all signals of the same data lane on the same layer.
- The DQS/DQSN signal pair should be routed as differential traces. The length difference between the differential traces should not exceed 20 mil, with a controlled impedance of 100 ±10% Ω.
- The length difference between the data lane and the CK signal should not exceed 400 mil.
- The impedance of any single-end signal trace should be 50 ±10% Ω.

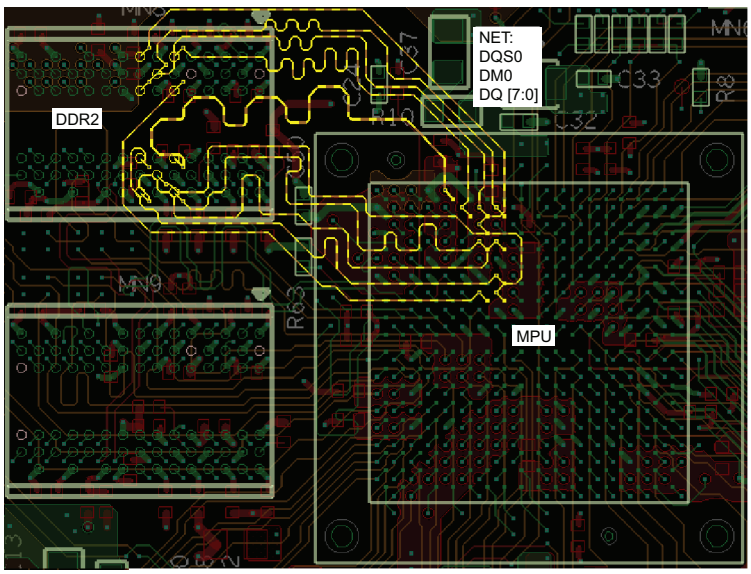
Here are some recommendations for the ADDR/CMD/CTL/CK signal layout:

- The length difference between the ADDR/CMD/CTL signal and the CK signal should not exceed 200 mil.
- It is recommended to route all those signals on the same layer.
- CK/CKn signals should be routed as differential traces. The length difference between the differential traces should not exceed 20 mil, with a controlled impedance of 100 ±10% Ω.
- The impedance of any single-end signal trace should be 50 ±10% Ω.

To minimize the crosstalk, the recommended trace spacing is as follows:

- In the same data lane: 8 to 12 mil
- Data lane signal to other signals: > 20 mil
- ADDR/CMD/CTL/CK to other signals: > 20 mil

Figure 3-4. DDR2 Layout Example



3.4 NAND Flash

The NAND Flash interface bus includes:

- Control signals: NANDCLE, NANDALE, NRD, NWE, NANDCE, NANDRDY
- Data signals: EBI_D[7:0]

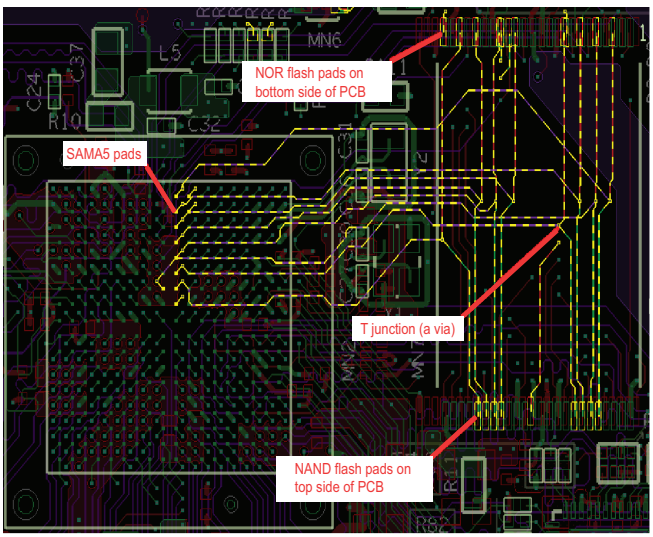
Layout recommendations:

- It is recommended to route all data signals on the same layer, and to make sure that the length differences do not exceed 400 mil.
- The impedance of all signal traces should be 50 ±10% Ω.

Figure 3-5 illustrates the routing of an EBI_D[7:0] data signal to a NAND Flash (mounted on the top side) and a parallel NOR Flash (mounted on the bottom side). The routing follows a simple T-type topology. The traces from the junction via to each device should have the same length.

In this case, there are no matching resistors as the trace is very short (no more than 2 inches). In many cases, a serial resistor (about 27 Ω) should be added to match the impedance of the line.

Figure 3-5. NAND Flash Layout Example



3.5 Ethernet

SAMA5D3 devices include an on-chip Gigabit Ethernet MAC that supports a 10/100/1000 Mbps Ethernet technology compatible with the IEEE 802.3 standard; furthermore, it supports several interface types including MII, GMII and RGMII.

The Media Independent Interface (MII) signals include transmit data, receive data and control signals.

Here are some recommendations for the data lane signal layout:

- It is recommended to route all signals of the same data lane (TX or RX) on the same layer.
- The length difference between the TX data and TXCK lanes should not exceed 300 mil.
- The length difference between the RX data and RXCK lanes should not exceed 300 mil.
- The impedance of any single-end signal trace should be 50 ±10% Ω.

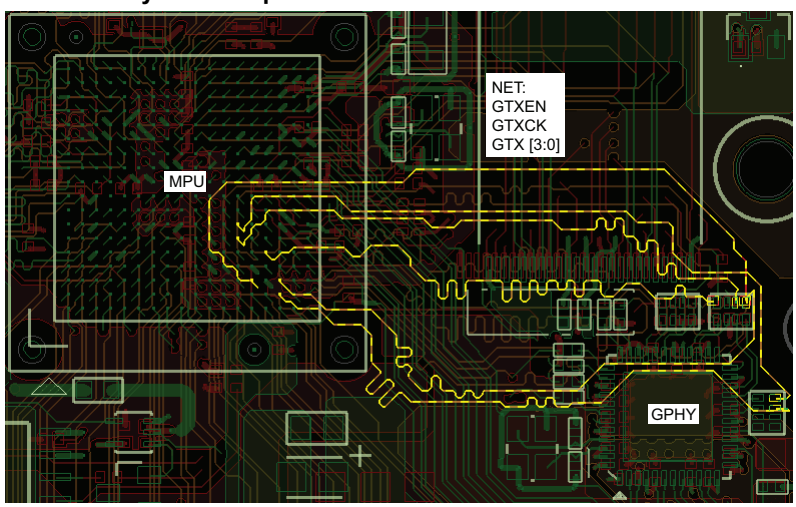
The Media Dependent Interface (MDI) (TX+/- or RX+/-) signals are routed to the Ethernet transformer and then further into the cable. The 100M-Base Ethernet cable has two pairs and the 1000M-Base Ethernet cable has four pairs.

The following layout rules apply:

- Differential pairs (TX+/- or RX+/-) should be routed away from all other signals (with a clearance of at least three times the trace width).
- The length difference between the MDI differential pairs (TX+/- or RX+/- lines) should not exceed 20 mil.
- Route differential pairs (TX+/- or RX+/-) over solid ground plane and/or chassis ground plane to achieve a 100 Ω differential (50 Ω for single-ended traces) impedance.

Figure 3-6 shows an example of RGMII transmitter data trace layout.

Figure 3-6. 1000M Ethernet PHY Layout Example



3.6 USB Signal

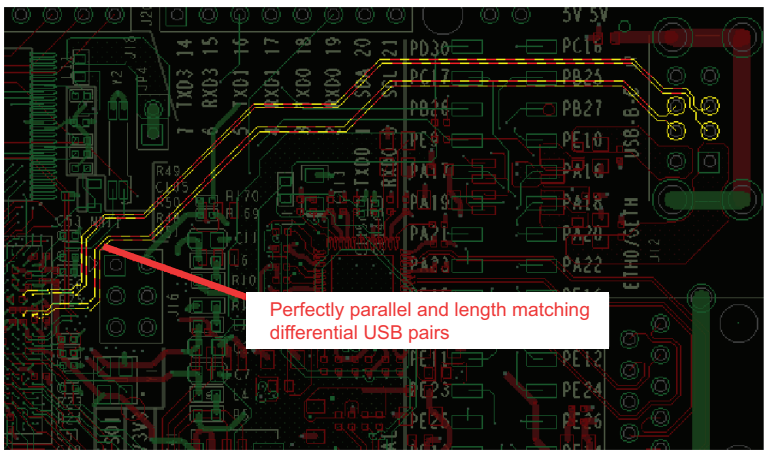
The USB ports in SAMA5D3 devices are compliant with USB v2.0 High-speed Specification.

Layout recommendations are:

- The USB DM and DP signals should be routed as differential traces and be perfectly parallel to each other.
- The reference plane should be continuous.
- If a routing layer must be changed, then the DM and DP signals should be transferred together to the other layer.
- The impedance of the differential traces should be 90 ±10% Ω.

Figure 3-7 shows a layout example of USB traces which fan out from BGA on the top layer, then go to the bottom layer through vias, and finally connect to the USB connector on the bottom layer.

Figure 3-7. USB Layout Example



4. Conclusion

This Application Note briefly introduces some of the most critical aspects to be taken into consideration when designing a SAMA5D3-based system. To beginners, we recommend to use these guidelines, but also to obtain support from expert PCB design services if relevant skills are unavailable in house.

We also recommend reading the excellent "High-Speed Digital Design: A Handbook of Black Magic" by Howard Johnson and Martin Graham, published by Prentice Hall.

5. Revision History

In the table that follows, the most recent version of the document appears first.

Table 5-1. Revision History

Doc. Rev.	Comments
11284B	Section 3.3 “Dynamic RAM Memory”: updated max length difference between each signal and the respective DQS/DQSn signal to100 mil.
11284A	First issue

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