



Multi-Purpose Flash Power Ratings

Application Note

March 2003

INTRODUCTION

SST's unique SuperFlash technology offers several advantages, including low power operation. Most flash memory applications require random access times ranging from 45 ns to 200 ns. In the past, SST's Multi-Purpose Flash (MPF) data sheets have specified active read current ratings that are based on 70 ns test results. However, many other flash memory vendors specify current ratings at very low speeds (typically 200 ns or slower), resulting in lower perceived current ratings. As a result, some SST customers have been unclear about the low power advantages of SST flash memories. SST is expanding its active read supply current specifications for MPF products in order to communicate more useful information to customers. This application note explains these specification changes, and also describes SST's low power advantages for programming and erasing.

READ CURRENT SPECIFICATIONS (I_{DD})

Prior to 2003, SST's MPF data sheets specified only a maximum limit (worst case) for I_{DD} , the Power Supply Current, during active read. Although it was not explicitly stated on most data sheets, this rating was based on 14 MHz (equivalent to 70 ns) testing speed values. For existing MPF products, SST will continue to specify and test all production devices for less than the max I_{DD} specification at this speed. In addition, SST now specifies typical¹ I_{DD} Active Read values in its MPF data sheets to help customers estimate typical system power usage.

In the future, SST will also specify 5 MHz (equivalent to 200 ns) maximum and typical I_{DD} active read values for MPF devices. For consistency and quality purposes, for existing products, i.e. devices that have been specified in the past using the 14 MHz rating, SST will test production units at both the 14 MHz max spec and at the 5 MHz max spec limits. This dual testing scheme will ensure quality and full backwards compatibility for all SST customers.

Because SST uses statistical process control methods requiring large sample sizes over time, most MPF data sheets at the time of this publication are not updated to reflect final 5 MHz ratings. However, this chart indicates the preliminary 5 MHz I_{DD} ratings versus actual 14 MHz I_{DD} ratings for SST's MPF devices:

TABLE 1: 5 MHz (200 NS) VERSUS 14 MHz (70 NS) I_{DD} READ RATINGS

Device(s)	5 MHz Test Rating (Preliminary)		14 MHz Test Rating (Actual)	
	I_{DD} Read Typical (mA)	I_{DD} Read Max (mA)	I_{DD} Read Typical (mA)	I_{DD} Read Max (mA)
SST39SF512	8.5	20	10	30
SST39SF040 / 020A / 010A	8.5	20	10	25
SST39LF/VF040 / 020 / 010 / 512	4	10	5	20
SST39LF/VF800A / 400A / 200A	6	16	9	30
SST39LF/VF080	4.5	10	12	15
SST39LF/VF160/016	4.5	10	12	20

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CURRENT AND ENERGY USAGE DURING PROGRAM AND ERASE

SST SuperFlash technology, based on SST's patented split-gate architecture, is quite unique compared to all other NOR flash vendors, most of whom utilize a stacked-gate architecture. These advantages and the technology behind them are described in several of SST's technical papers, available online at www.SST.com and in the SST data book.

1. Typical condition ratings are average values of devices tested at 25°C (room temperature) and $V_{DD} = 3V$ for "VF" devices (such as SST39VF040) or $V_{DD} = 5V$ for "SF" devices (such as SST39SF040).



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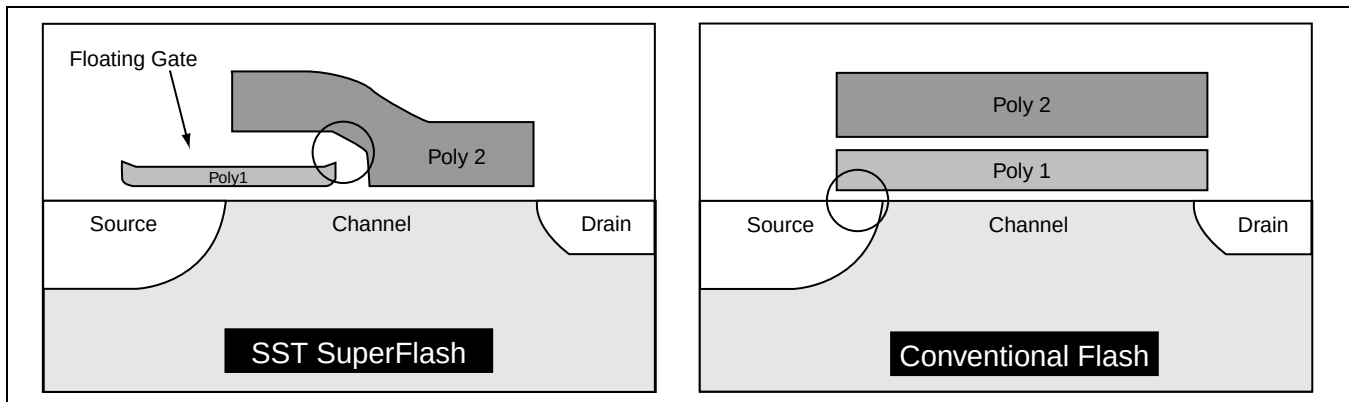


FIGURE 1: SST SUPERFLASH CELL VERSUS CONVENTIONAL STACKED GATE FLASH CELL

One particular advantage (besides fast Program times and low current during Program and Erase) is substantially lower Erase times, on the order of 40 to 600 times faster than other vendors (and 1,000 times faster at higher densities). Since energy consumed is a function of (current) x (time) x (voltage), energy consumed using SST flash during Program and Erase cycles is substantially lower. The table below illustrates this, and shows that for typical Erase cycles, SST SuperFlash is approximately 500 times more energy efficient than other flash architectures.

TABLE 2: COMPARISON OF ERASE TIME, CURRENT, AND ENERGY CONSUMPTION

	SST39VF160		Am29LV160D		28F160B3	
	Typ	Max	Typ*	Max*	Typ	Max
Sector Erase Time (2KW, ms)	18	25	N/A	N/A	N/A	N/A
Block Erase Time (32KW, ms)	18	25	700	15,000	1,000	5,000
Chip Erase Time (ms)	70	100	25,000	N/S	38,000 [†]	N/S
Erase Current (mA)	16 [†]	25	20	30	16*	45*
Energy per Block Erase (mJ) [‡]	0.9	1.9	42.0	1,350.0	48.0*	675.0*
Energy per Chip Erase (mJ) [‡]	3.4	7.5	1,500.0		1,824.0*	

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* Excludes pre-programming

† Based on SST tests only

‡ Calculated as (ms x mA x 3V)

Note: Data source: SST, AMD, and Intel data sheets unless noted.

N/A: Not Available

N/S: Not Specified

This does not even take into account the fact that SST SuperFlash does not require pre-programming before erasing, which otherwise lengthens the total Erase cycle and requires a brief 30 to 70 mA (typ) current spike.

SUMMARY

In summary, SST's SuperFlash technology provides excellent power and total energy efficiency. In order to communicate more useful information to customers, SST now provides typical I_{DD} active read values in its MPF data sheets as well as 5 MHz I_{DD} active read ratings in this application note. In future data books, SST will also specify 5 MHz ratings for MPF products within the respective data sheets.