

## Migrating from the LAN9117 to the LAN9211

### OBJECTIVE

The purpose of this application note is to assist Microchip customers with existing LAN9117 designs when upgrading to the new LAN9211 devices. Migrating from the LAN9117 to the LAN9211 will require PCB modifications to support the new LAN9211 package type and the HP Auto-MDIX PHY (even if this mode is not used). This application note addresses all the differences between the LAN9117 and the LAN9211 devices, making this transition as easy as possible.

### References

LAN9211 Data Sheet

- One-Page Reference Design for the LAN9211
- One-Page Reference Design for the LAN9117
- Application Note 8-13 Suggested Magnetics

### Overview of Changes Required

Table 1 summarizes the changes needed to migrate from the LAN9117 to the LAN9211.

**TABLE 1: SUMMARY OF CHANGES REQUIRED**

Change Required	Comments	References
New PCB	Needed to support footprint change, magnetics and passive component changes.	This application note and 1-Page Reference Designs are available at <a href="http://www.Microchip.com">www.Microchip.com</a> .
New magnetics and passive component network on PHY side of magnetics	Needed to support HP Auto-MDIX.	See Application Note 8-13 for list of recommended magnetics. AN8-13, this application note and the LAN9211 Data Sheet are available at <a href="http://www.Microchip.com">www.Microchip.com</a> .
Firmware Upgrade	Needed to take advantage of faster Host Bus timing and mixed endian support	This application note and LAN9211 Data Sheet are available at <a href="http://www.Microchip.com">www.Microchip.com</a> .
Upgrade drivers	Recognize new device ID and utilize new Checksum Offload Engine	Refer to <a href="#">Table 3, "Driver Support"</a>

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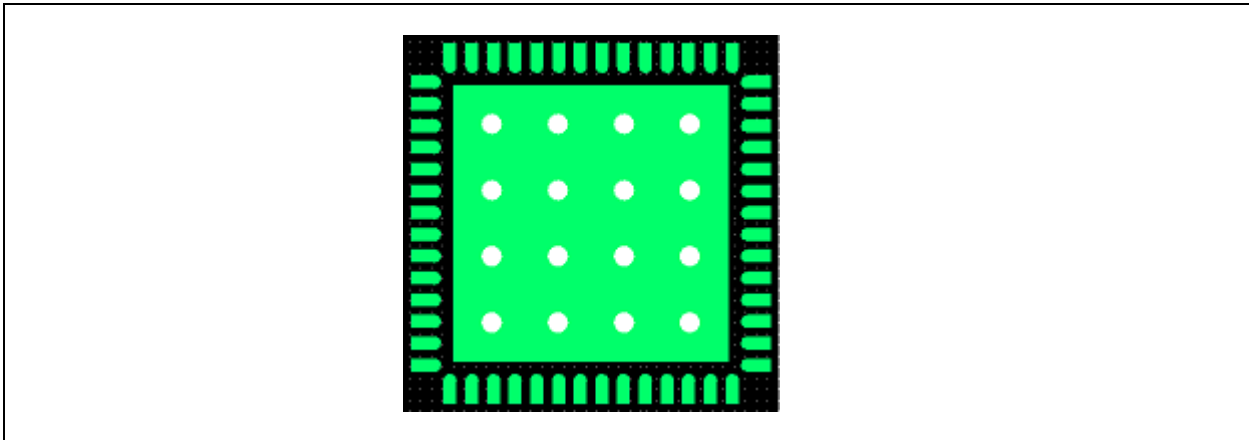
## HARDWARE CHANGES

### Component Changes

#### DEVICE PACKAGE

The LAN9211 is packaged in a 56-pin QFN with an exposed VSS pad. Therefore, the LAN9211 is not a drop in replacement for the LAN9117 and will require a new PCB. The recommended PCB land pattern can be found in Chapter 8 of the LAN9211 Data Sheet. It is recommended to place a 4x4 grid of vias at 60mil spacing in the exposed pad area for connection to the board's ground plane, as shown in [Figure 1](#) below. Please consult with your Assembly House for their process capabilities and recommendations.

**FIGURE 1: PCB LAND PATTERN**



#### MAGNETICS

Migrating to the LAN9211 requires different magnetics than those used on the LAN9117. These magnetics have symmetrical channel configurations to allow for the switching of the receive and transmit channels. A list of suggested magnetics for the LAN9211 can be found in [Application Note 8-13, entitled "Suggested Magnetics"](#).

### Circuit Changes

#### TRANSMIT CIRCUIT

The transmit circuit used by the LAN9211, as shown in [Figure 2](#) below, is similar to that of the LAN9117.

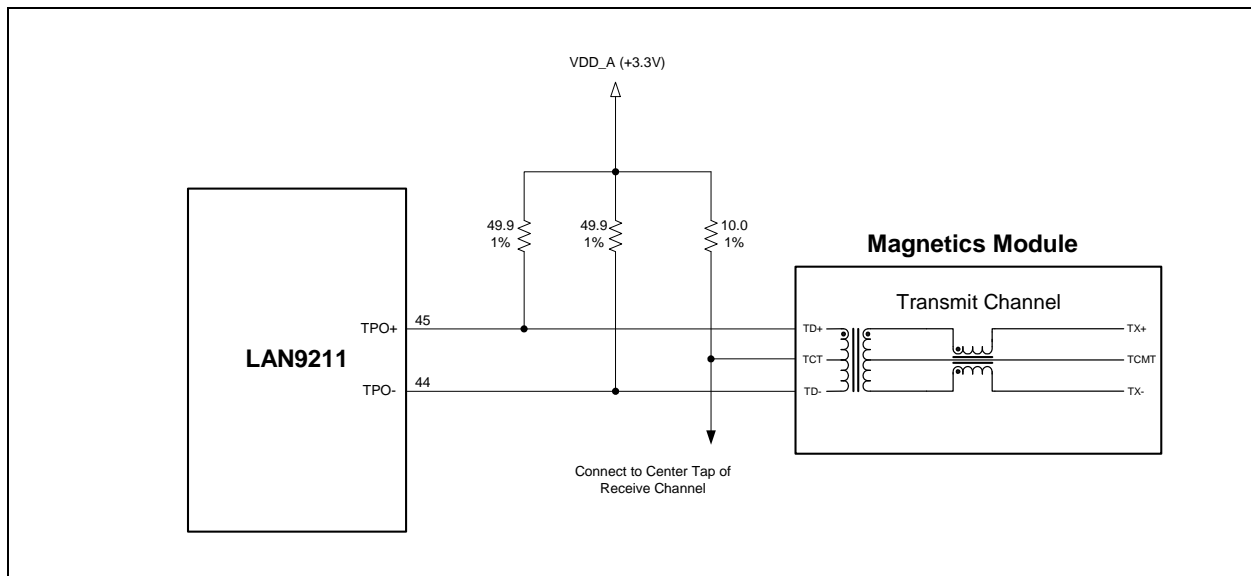
The similarities between the LAN9211 and the LAN9117 are as follows:

- A 49.9 ohm, 1% resistor from each side of the twisted pair to VDD\_A (+3.3V).
- A 10 ohm, 1% resistor from the transmit center tap to VDD\_A (+3.3V).

The differences between the LAN9211 and the LAN9117 are as follows:

- The LAN9211 uses magnetics that support HP Auto-MDIX.
- The device-side center tap of the transmit core (TCT) is attached to the device-side center-tap of the receive core (RCT).
- The 49.9 ohm resistors should be placed as close as possible to the LAN9211.

FIGURE 2: LAN9211 TRANSMIT CIRCUIT



## RECEIVE CIRCUIT

The receive circuit used by the LAN9211, as shown in [Figure 3](#) below, is similar to that of the LAN9117.

The similarities between the LAN9211 and the LAN9117 are as follows:

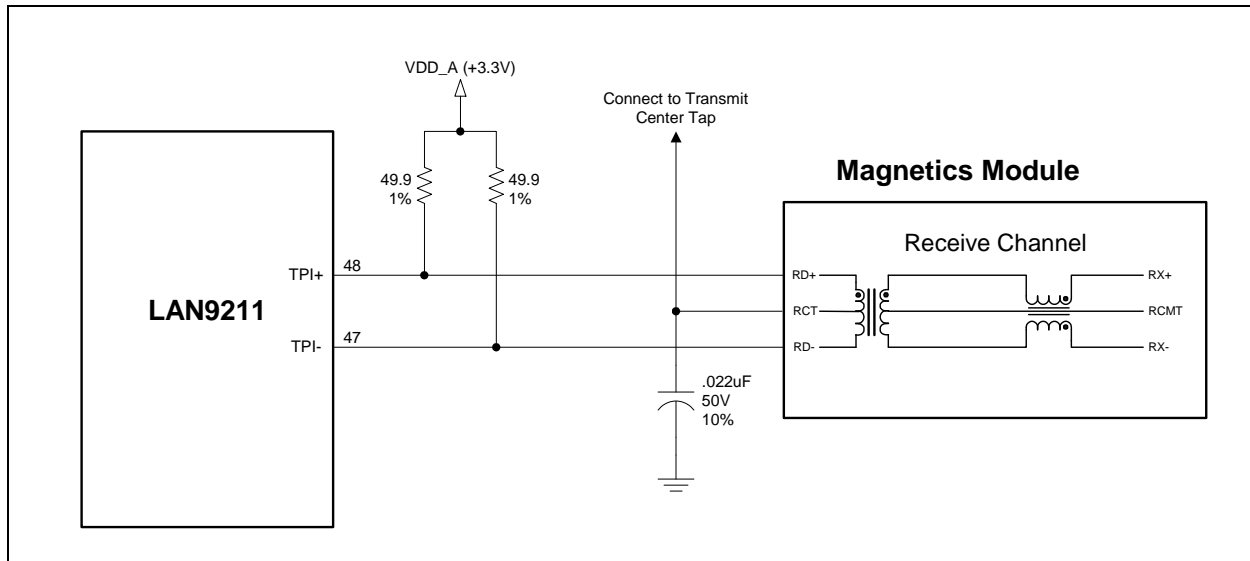
- Both designs have two 49.9 ohm, 1% resistors between the two signals in the twisted pair.

The differences between the LAN9211 and the LAN9117 are as follows:

- The LAN9211 uses magnetics that support HP Auto-MDIX.
- The LAN9117 had two 6.8nF capacitors, one in series with each side of the twisted pair. These are eliminated (shorted) in the LAN9211.
- In the LAN9117, the mid-point between the two 49.9 ohm resistors is tied to the center tap of the magnetics (RCT) and to a 0.01uF bypass capacitor to ground. In the LAN9211, both resistors are tied to VDD\_A (+3.3V), and the 0.01uF bypass capacitor has been eliminated. The center-tap of the receive channel of the magnetics is tied to the transmit center tap (TCT) and to a common 0.022uF bypass capacitor to ground.
- The 49.9 ohm resistors should be placed as close as possible to the LAN9211.

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**FIGURE 3: LAN9211 RECEIVE CIRCUIT**



## EMC CONSIDERATIONS

For LAN9211 designs that must operate in an EMI constrained environment, the designer should include four low valued capacitors (less than 15pF) on the TPO+, TPO-, TPI+ & TPI- pins and terminate them to digital ground. These capacitors should be placed as close as possible to the magnetics. These capacitors can then be populated as required for EMI compliance. Additionally, the use of a discrete magnetic and RJ-45 connector is highly recommended, as the integrated magnetics are known to cause EMI compliance issues.

## Pin Changes

### PIN CROSS-REFERENCE

Table 2 below cross-references signal/pin changes between the LAN9117 and the LAN9211.

**TABLE 2: PIN CROSS-REFERENCE**

LAN9117		LAN9211	
Signal	Pin	Signal	Pin
D[15:0]	43-46, 49-53, 56-59, 62-64	D[15:0]	19-23, 25-29, 31-36
A[7:1]	12-18	A[7:1]	6-12
nRD	92	nRD	15
nWR	93	nWR	16
nCS	94	nCS	17
IRQ	72	IRQ	43
Reserved	73, 71, 84, 90, 91	Reserved	14
		AMDIX_EN	52
SPEED_SEL	74		
FIFO_SEL	76	FIFO_SEL	13
TPO+	79	TPO+	45
TPO-	78	TPO-	44
TPI+	83	TPI+	48
TPI-	82	TPI-	47
EXRES1	87	EXRES1	50

TABLE 2: PIN CROSS-REFERENCE (CONTINUED)

LAN9117		LAN9211	
Signal	Pin	Signal	Pin
EEDIO	67	EEDIO	38
EECS	68	EECS	39
EECLK	69	EECLK	40
XTAL1	6	XTAL1	55
XTAL2	5	XTAL2	54
nRESET	95	nRESET	42
PME	70	PME	41
GPIO[2:0]	100, 99, 98	GPIO[2:0]	5, 4, 3
RBIAS	10		
ATEST	9		
VREG	2		
VDD_IO	20, 28, 35, 42, 48, 55, 61, 97	VDD_IO	1, 18, 24, 30, 56
GND_IO	19, 27, 34, 41, 47, 54, 60, 96		
VDD_A	81, 85, 89	VDD_A33	46, 49, 51
VSS_A	77, 80, 86, 88		
VDD_CORE	3, 65	VDD_CORE	2, 37
GND_CORE	1, 66		
VDD_PLL	7		
VSS_PLL	4		
VDD_REF	8		
VSS_REF	11		
		VDD_A18	53
		VSS	Exposed Pad
TX_CLK	40		
TXD[3:0]	36-39		
TX_EN	21		
RX_CLK	26		
RX_ER	25		
COL	33		
RXD[3:0]	24, 23, 22, 75		
CRS	32		
RX_DV	29		
MDIO	30		
MDC	31		

## SIGNAL PINS NOT AVAILABLE ON THE LAN9211

The following signal pins are not available on the LAN9211:

- SPEED\_SEL
- RBIAS
- ATEST
- TX\_CLK, TXD[3:0], TX\_EN
- RX\_CLK, RX\_ER, RXD[3:0], RX\_DV
- COL, CRS
- MDIO, MDC

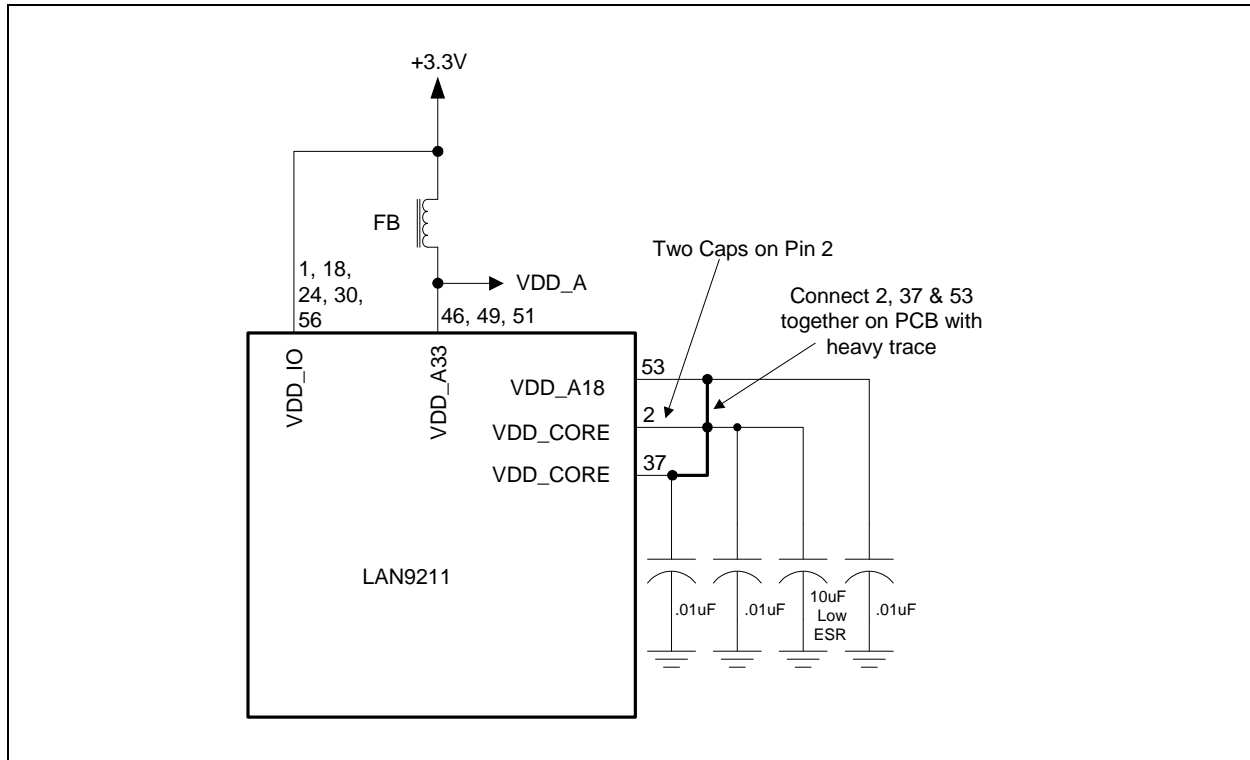
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## POWER AND GROUND PIN CHANGES

The LAN9117 has several different ground pins (GND\_IO, VSS\_A, GND\_CORE, VSS\_PLL and VSS\_REF). However, the LAN9211 uses a single ground connection (VSS) on the exposed pad. Also, the LAN9211 does not have VDD\_PLL, VDD\_REF, and VREG power pins.

The LAN9211 has a VDD\_A18 (pin 53) that must be externally connected to VDD\_CORE (pins 2, 37) with traces at least 10 mil wide and connected to a 10uF low ESR ceramic capacitor. Each of these 3 pins must be individually decoupled with a 0.01uF capacitor as close as possible to the pin, as shown in [Figure 4](#).

**FIGURE 4: POWER CONNECTIONS**



## AMDIX\_EN (PIN 52)

The LAN9211 includes an HP Auto-MDIX enabled PHY, this pin can be used to enable/disable Auto-MDIX on power-up/reset. This pin has an internal pull-up and must be pulled low to disable Auto-MDIX. To enable Auto-MDIX, this pin should be pulled high or left unconnected. The state of this pin can be read via the HW\_CFG register and can also be overridden via Phy register 27, as described in [Section , "Register Changes"](#).

## REGISTER CHANGES

### SCSR Register Changes

#### ID\_REV REGISTER (OFFSET: 50H)

- Bit 31:16 changed to 9211h

#### HW\_CFG REGISTER (OFFSET: 74H)

- Bits 6:2 become reserved
- Bit 24 becomes AMDIX\_EN Strap State. This read-only bit reflects the state of the AMDIX\_EN strap pin (pin 52). This pin can be overridden by PHY registers 27.15 and 27.13.
- Bit 28 becomes FSELEND, Direct FIFO Access Endian Ordering. This control bit determines the endianness of RX and TX data FIFO host accesses when accessed using the FIFO\_SEL signal. When this bit is cleared, FIFO\_SEL accesses utilize little endian byte ordering. When this bit is set, FIFO\_SEL accesses utilize big endian byte ordering. Please refer to Section 3.8 of the LAN9211 Data Sheet for more information on this feature.
- Bit 29 becomes FPORTEND, FIFO Port Endian Ordering. This control bit determines the endianness of RX and TX data FIFO host accesses when accessed through the RX/TX Data FIFO ports, including the alias addresses (any access from 00h to 3Ch). When this bit is cleared, data FIFO port accesses utilize little endian byte ordering. When this bit is set, data FIFO port accesses utilize big endian byte ordering. Please refer to Section 3.8 of the LAN9211 Data Sheet for more information on this feature.

### MAC Register Changes

#### COE\_CR REGISTER (OFFSET: DH)

The Checksum Offload Engine Control Register (COE\_CR), has been added to the LAN9211 at offset Dh. This register controls the transmit and receive checksum offload engines. Please refer to Section 3.6 of the LAN9211 Data Sheet for more information on this feature.

- Bits 31:17 - Reserved
- Bit 16 - TX Checksum Offload Engine Enable (TXCOE\_EN). TXCOE\_EN may only be changed if the TX data path is disabled. If cleared, the TXCOE is bypassed. If set, the TXCOE is enabled.
- Bits 15:2 - Reserved
- Bit 1 - RX Checksum Offload Engine Mode (RXCOE\_MODE). This bit indicates whether the RXCOE will check for VLAN tags or a SNAP header prior to beginning its checksum calculation. In its default mode, the calculation will always begin 14 bytes into the frame. RXCOE\_MODE may only be changed if the RX data path is disabled. If set, begin checksum calculation after first 14 bytes of Ethernet Frame. If cleared, begin checksum calculation at start of L3 packet by adjusting for VLAN tags and/or SNAP header.
- Bit 0 - RX Checksum Offload Engine Enable (RXCOE\_EN). RXCOE\_EN may only be changed if the RX data path is disabled. If cleared, the RXCOE is bypassed. If set, the RXCOE is enabled.

### PHY Register Changes

#### PHY IDENTIFIER 2 (OFFSET: 4)

The value of this register is changed from 0xC0D1 to 0xC0C3.

#### SPECIAL CONTROL/STATUS INDICATIONS (OFFSET: 27)

- Bit 15 becomes Override AMDIX Strap.
  - 0 - AMDIX\_EN (pin 52) enables or disables HP Auto-MDIX.
  - 1 - Override pin 52. PHY register 27.14 and 27.13 determine MDIX function.
- Bit 14 becomes Auto-MDIX Enable. Only effective when 27.15 = 1, otherwise ignored.
  - 0 = disable Auto-MDIX, 27.13 determines normal or reversed connection.
  - 1 = enable Auto-MDIX, 27.13 must be set to 0.

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- Bit 13 becomes Auto-MDIX State. Only effective when 27.15 = 1, otherwise ignored.

When 27.14 = 0 (manually set MDIX state):

0 = no crossover (TPO = output, TPI = input).

1 = crossover (TPO = input, TPI = output).

When 27.14 = 1 (Auto-MDIX) this bit must be set to 0.

Do not use the combination 27.15 = 1, 27.14 = 1, 27.13 = 1.

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## ADDITIONAL FEATURE CHANGES

### Mixed Endian Support

In addition to the Word Swap function supported by both the LAN9117 and the LAN9211, the LAN9211 also provides support for mixed endian data FIFO accesses. The LAN9211 provides the ability to select data FIFO endianness separately for accesses through the data FIFO ports (addresses 00h-3Ch) or using the FIFO\_SEL input signal. This is accomplished via the FPORTEND and FSELEND bits of the HW\_CFG—Hardware Configuration Register, respectively. Please refer to Section 3.8 of the LAN9211 Data Sheet for more information.

**Note:** CSR and status FIFO accesses are not affected by the FPORTEND and FSELEND endianness select bits.

### Checksum Offload Engine (COE)

The LAN9211 contains two checksum offload engines, which offload the calculation of the 16-bit checksum for transmitted and received Ethernet frames. Please refer to Section 3.6 of the LAN9211 Data Sheet for detailed information on the use of the COE's. Please note that currently only the Linux driver supports checksum offloading.

#### RECEIVE CHECKSUM OFFLOAD ENGINE (RXCOE)

The receive checksum offload engine provides assistance to the CPU by calculating a 16-bit checksum for a received Ethernet frame. The RXCOE readily supports the following IEEE 802.3 frame formats:

- Type II Ethernet frames
- SNAP encapsulated frames
- Support for up to 2, 802.1q VLAN tags

#### TRANSMIT CHECKSUM OFFLOAD ENGINE (TXCOE)

The transmit checksum offload engine provides assistance to the CPU by calculating a 16-bit checksum, typically for TCP, for a transmit Ethernet frame. The TXCOE calculates the checksum and inserts the results back into the data stream as it is transferred to the MAC.

### External PHY

The LAN9211 does not support an external PHY, therefore all signal pins associated with the external PHY on the LAN9115 are no longer available on the LAN9211. These include:

- TX\_CLK, TXD[3:0], TX\_EN
- RX\_CLK, RX\_ER, RXD[3:0], RX\_DV
- COL, CRS
- MDIO, MDC

**Note:** TX\_CLK, TX\_EN, RX\_CLK and RX\_DV can still be observed the GPO3 and GPO4 pins.

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## DRIVER SUPPORT

Table 3 below shows the version of drivers needed to support the LAN9211.

**TABLE 3: DRIVER SUPPORT**

Driver	Revision
WinCE 5.0 - XScale (PXA270)	1.10 or later
Linux - XScale (PXA270)	1.52 or later

## APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003002A (03-18-19)	Replaces the previous SMSC version, Rev. 04 (04-04-13)	
Rev. 0.4 (04-04-13)	Document co-branded: Microchip logo added to cover page, legal disclaimer modified.	
Rev. 0.4 (04-03-08)	Standard SMSC formatting applied	
Rev. 0.3 (03-10-08)	<a href="#">Transmit Circuit on page 2</a> , <a href="#">Receive Circuit on page 3</a> and <a href="#">EMC Considerations on page 4</a>	Added resistor placement bullet  Added section

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