

## PIC18F2X/4XQ10 Memory Programming Specification

### 1.0 OVERVIEW

This programming specification describes an SPI-based programming method for the PIC18F2X/4XQ10 family of microcontrollers. [Section 3.0 “Programming Algorithms”](#) describes the programming commands, programming algorithms and electrical specifications used in that particular programming method. [Appendix B: “PIC18F2X/4XQ10 Device ID, Checksums and Pinout Descriptions”](#) contains individual part numbers, device identification and checksum values, pinout and packaging information, and Configuration Words.

**Note 1:** This is an SPI-compatible programming method with 8-bit commands.

**2:** The low-voltage entry code is now 32 clocks and MSb first, unlike previous PIC18 devices which had 33 clocks and LSb first.

### 1.1 Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming (ICSP) interface. Data can be programmed into the Program Flash Memory (PFM), Data EEPROM Memory, dedicated “User ID” locations and the Configuration Words.

### 1.2 Write and/or Erase Selection

Erasing or writing is selected according to the command used to begin operation (see [Table 3-1](#)). The terminologies used in this document, related to erasing/writing to the program memory, are defined in [Table 1-1](#) and are detailed below.

**TABLE 1-1: PROGRAMMING TERMS**

| Term            | Definition                             |
|-----------------|----------------------------------------|
| Programmed Cell | A memory cell at logic ‘0’             |
| Erased Cell     | A memory cell at logic ‘1’             |
| Erase           | Change memory cell from a ‘0’ to a ‘1’ |
| Write           | Change memory cell from a ‘1’ to a ‘0’ |
| Program         | Generic erase and/or write             |

#### 1.2.1 ERASING MEMORY

Memory is erased by 128-word sectors or in bulk, where ‘bulk’ includes many subsets of the total memory space. The duration of the data memory erase is determined by the size of data memory. All Bulk ICSP Erase commands have minimum VDD requirements, which are higher than the Sector Erase and Write requirements.

Sectors pertain to PFM and User ID memory only. Configuration and data memory should be erased by the Bulk Erase command. For self-write operations, each byte write to data memory includes an automatic erase cycle for the location about to be programmed.

#### 1.2.2 WRITING MEMORY

Memory is written one word at a time. The duration of the write is determined internally.

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## 1.3 Hardware Requirements

### 1.3.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for VDD and one for the MCLR/VPP pin.

### 1.3.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, the device can be programmed using a single VDD source in the device operating range. The MCLR/VPP pin does not have to be brought to programming voltage, but can instead be left at the normal operating voltage.

#### 1.3.2.1 Single-Supply ICSP Programming

The device's LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled). The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to VIH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

**Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIH to the MCLR/VPP pin.

**2:** While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit. Also, the port pin can no longer be used as a general purpose input.

## 1.4 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in [Table 1-2](#). For pin locations and packaging information, please refer to [Table B-3](#).

**TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING**

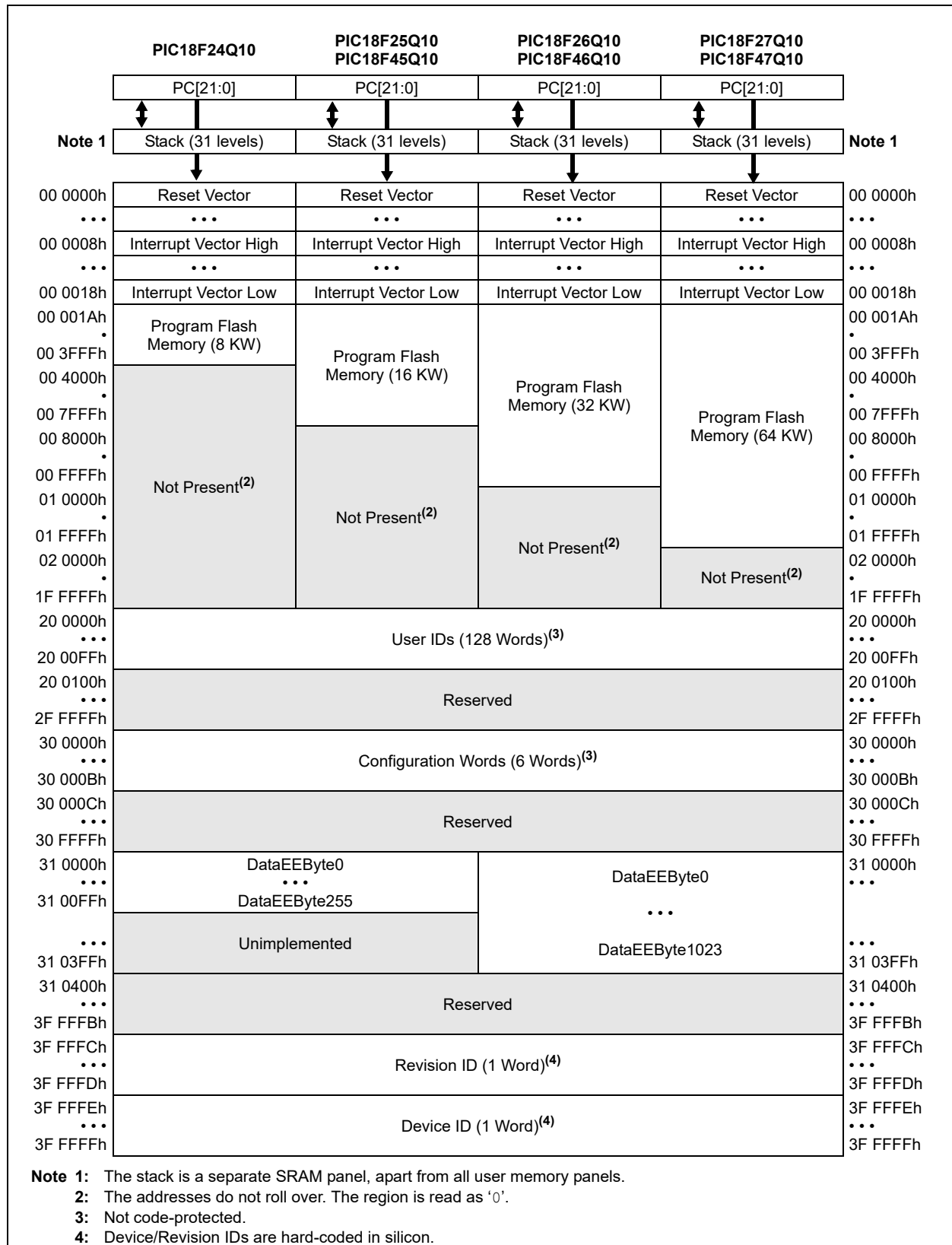
| Pin Name | During Programming  |                  |                                           |
|----------|---------------------|------------------|-------------------------------------------|
|          | Function            | Pin Type         | Pin Description                           |
| ICSPCLK  | ICSPCLK             | I                | Clock Input – Schmitt Trigger Input       |
| ICSPDAT  | ICSPDAT             | I/O              | Data Input/Output – Schmitt Trigger Input |
| MCLR/VPP | Program/Verify mode | I <sup>(1)</sup> | Program Mode Select                       |
| VDD      | VDD                 | P                | Power Supply                              |
| VSS      | VSS                 | P                | Ground                                    |

**Legend:** I = Input, O = Output, P = Power

**Note 1:** The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current.

## 2.0 MEMORY MAP

**FIGURE 2-1: PROGRAM AND DATA EEPROM MEMORY MAP**



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**TABLE 2-1: MEMORY MAP AND CODE PROTECTION CONTROL**

| Reg. | Address<br>(from/to)                                                                         | Device                             |                                    |                                    |                                    |                                    |                   |  |  |
|------|----------------------------------------------------------------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|-------------------|--|--|
|      |                                                                                              | PIC18F24Q10                        | PIC18F25Q10<br>PIC18F45Q10         | PIC18F26Q10<br>PIC18F46Q10         | PIC18F27Q10<br>PIC18F47Q10         |                                    |                   |  |  |
| PFM  | 00 0000h<br>00 07FFh                                                                         | Boot Block 1 KW<br>CP, WRTB, EBTRB | Boot Block 1 KW<br>CP, WRTB, EBTRB | Boot Block 1 KW<br>CP WRTB, EBTRB  | Boot Block 1 KW<br>CP WRTB, EBTRB  |                                    |                   |  |  |
|      | 00 0800h<br>00 1FFFh                                                                         | Block 0<br>3 KW<br>CP, WRT0, EBTR0 | Block 0<br>3 KW<br>CP, WRT0, EBTR0 | Block 0<br>7 KW<br>CP, WRT0, EBTR0 | Block 0<br>7 KW<br>CP, WRT0, EBTR0 |                                    |                   |  |  |
|      | 00 2000h<br>00 3FFFh                                                                         | Block 1<br>4 KW<br>CP, WRT1, EBTR1 | Block 1<br>4 KW<br>CP, WRT1, EBTR1 |                                    |                                    |                                    |                   |  |  |
|      | 00 4000h<br>00 5FFFh<br>00 6000h<br>00 7FFFh<br>00 8000h<br>00 BFFFh<br>00 C000h<br>00 FFFFh | Not present                        | Block 2<br>4 KW<br>CP, WRT2, EBTR2 | Block 1<br>8 KW<br>CP, WRT1, EBTR1 | Block 1<br>8 KW<br>CP, WRT1, EBTR1 |                                    |                   |  |  |
|      | 01 0000h<br>01 3FFFh<br>01 4000h<br>01 7FFFh<br>01 8000h<br>01 BFFFh<br>01 C000h<br>01 FFFFh |                                    | Block 3<br>4 KW<br>CP, WRT3, EBTR3 |                                    |                                    |                                    |                   |  |  |
|      | Not present                                                                                  |                                    | Not present                        | Block 2<br>8 KW<br>CP, WRT2, EBTR2 | Block 2<br>8 KW<br>CP, WRT2, EBTR2 |                                    |                   |  |  |
|      |                                                                                              |                                    |                                    | Block 3<br>8 KW<br>CP, WRT3, EBTR3 | Block 3<br>8 KW<br>CP, WRT3, EBTR3 |                                    |                   |  |  |
|      |                                                                                              |                                    |                                    | Not present                        | Not present                        | Block 4<br>8 KW<br>CP, WRT4, EBTR4 |                   |  |  |
|      |                                                                                              |                                    |                                    |                                    |                                    | Block 5<br>8 KW<br>CP, WRT6, EBTR5 |                   |  |  |
|      |                                                                                              |                                    |                                    |                                    |                                    | Block 6<br>8 KW<br>CP, WRT6, EBTR6 |                   |  |  |
|      |                                                                                              |                                    |                                    |                                    |                                    | Block 7<br>8 KW<br>CP, WRT7, EBTR7 |                   |  |  |
|      |                                                                                              |                                    |                                    | CONFIG                             | 30 0000h<br><br>30 000Bh           | 6 Words<br>WRTC                    |                   |  |  |
|      |                                                                                              |                                    |                                    |                                    |                                    |                                    |                   |  |  |
|      |                                                                                              | Data<br>EEPROM                     |                                    | 31 0000h<br>31 00FFh               | 256 Words<br>CPD, WRTD             |                                    | 1 KW<br>CPD, WRTD |  |  |
|      |                                                                                              |                                    |                                    | 31 0100h<br>31 03FFh               | Unimplemented                      |                                    |                   |  |  |
|      |                                                                                              |                                    |                                    |                                    |                                    |                                    |                   |  |  |
|      |                                                                                              |                                    |                                    |                                    |                                    |                                    |                   |  |  |

## 2.1 User ID Location

A user may store identification information (User ID) in 128 designated locations. The User ID locations are mapped to 20 0000h-20 00FFh. Each location is 16 bits in length. It is recommended that the Most Significant nibble of each ID be Fh. In doing so, if the user code inadvertently tries to execute from the ID space, the ID data will execute as a **NOB**. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

## 2.2 Device/Revision ID

The 16-bit Device ID Word is located at 3F FFEh and the 16-bit Revision ID is located at 3F FFFCh. These locations are read-only and cannot be erased or modified.

### REGISTER 2-1: DEVICEID: DEVICE ID REGISTER

|           |   |   |   |       |   |   |   |
|-----------|---|---|---|-------|---|---|---|
| R         | R | R | R | R     | R | R | R |
| DEV[15:8] |   |   |   |       |   |   |   |
| bit 15    |   |   |   | bit 8 |   |   |   |

|          |   |   |   |       |   |   |   |
|----------|---|---|---|-------|---|---|---|
| R        | R | R | R | R     | R | R | R |
| DEV[7:0] |   |   |   |       |   |   |   |
| bit 7    |   |   |   | bit 0 |   |   |   |

#### Legend:

R = Readable bit      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **DEV[15:0]:** Device ID bits (see [Table B-1](#))

### REGISTER 2-2: REVISIONID: REVISION ID REGISTER

|        |   |   |   |             |   |   |   |
|--------|---|---|---|-------------|---|---|---|
| R      | R | R | R | R           | R | R | R |
| 1      | 0 | 1 | 0 | MJRREV[5:2] |   |   |   |
| bit 15 |   |   |   | bit 8       |   |   |   |

|             |   |             |   |       |   |   |   |
|-------------|---|-------------|---|-------|---|---|---|
| R           | R | R           | R | R     | R | R | R |
| MJRREV[1:0] |   | MNRREV[5:0] |   |       |   |   |   |
| bit 7       |   |             |   | bit 0 |   |   |   |

#### Legend:

R = Readable bit      '1' = Bit is set      0' = Bit is cleared      x = Bit is unknown

bit 15-12      **Read as '1010'**

These bits are fixed with value, '1010', for all devices in this programming specification.

bit 11-6      **MJRREV[5:0]:** Major Revision ID bits

These bits are used to identify a major revision. A major revision is indicated by an all layer revision (A0, B0, C0, etc...).

Revision A = 6'b00\_0000

bit 5-0      **MNRREV[5:0]:** Minor Revision ID bits

These bits are used to identify a minor revision.

Revision A0 = 6'b00\_0000

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## 2.3 Configuration Words

The devices have six Configuration Words, starting at address, 30 0000h. The individual bits within these Configuration Words are critical to the correct operation of the system. Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, these important Configuration bits should be considered:

### 1. LVP: Low-Voltage Programming Enable bit

- 1 = ON – Low-Voltage Programming is enabled.  $\overline{\text{MCLR}}/\text{VPP}$  pin function is  $\overline{\text{MCLR}}$ .  
MCLRE Configuration bit is ignored.
- 0 = OFF – High voltage on  $\overline{\text{MCLR}}/\text{VPP}$  must be used for programming.

It is important to note that the LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the configuration state. For more information, see [Section 3.1.2 “Low-Voltage Programming \(LVP\) Mode”](#).

### 2. MCLRE: Master Clear ( $\overline{\text{MCLR}}$ ) Enable bit

- If LVP = 1:  
RE3 pin function is  $\overline{\text{MCLR}}$ .
- If LVP = 0:  
1 =  $\overline{\text{MCLR}}$  pin is  $\overline{\text{MCLR}}$   
0 =  $\overline{\text{MCLR}}$  pin function is a port-defined function

### 3. CPD: Data NVM (EEPROM) Memory Code Protection bit

- 1 = OFF – Data NVM code protection is disabled
- 0 = ON – Data NVM code protection is enabled

### 4. CP: User NVM Program Memory Code Protection bit

- 1 = OFF – User NVM code protection is disabled
- 0 = ON – User NVM code protection is enabled

For more information on code protection, see [Section 3.3 “Code Protection”](#).

## 3.0 PROGRAMMING ALGORITHMS

### 3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted, MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK pins are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

#### 3.1.1 HIGH-VOLTAGE PROGRAM/VERIFY MODE ENTRY AND EXIT

There are two different modes of entering Program/Verify mode via high voltage:

- VPP – First Entry mode
- VDD – First Entry mode

##### 3.1.1.1 VPP – First Entry Mode

To enter Program/Verify mode via the VPP-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on  $\overline{\text{MCLR}}$  from 0V to  $V_{\text{IH}}H$ .
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-First Entry mode prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has already been programmed to have MCLR disabled ( $\text{MCLRE} = 0$ ), the Power-up Timer disabled ( $\text{PWRTE} = 0$ ) and the internal oscillator selected, the device will execute code immediately. Since this may prevent entry, VPP-First Entry mode is strongly recommended as it prevents user code from changing EEPROM contents or driving pins to affect Test mode entry. See the timing diagram in [Figure 3-1](#).

##### 3.1.1.2 VDD – First Entry Mode

To enter Program/Verify mode via the VDD-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on  $\overline{\text{MCLR}}$  from VDD or below to  $V_{\text{IH}}H$ .

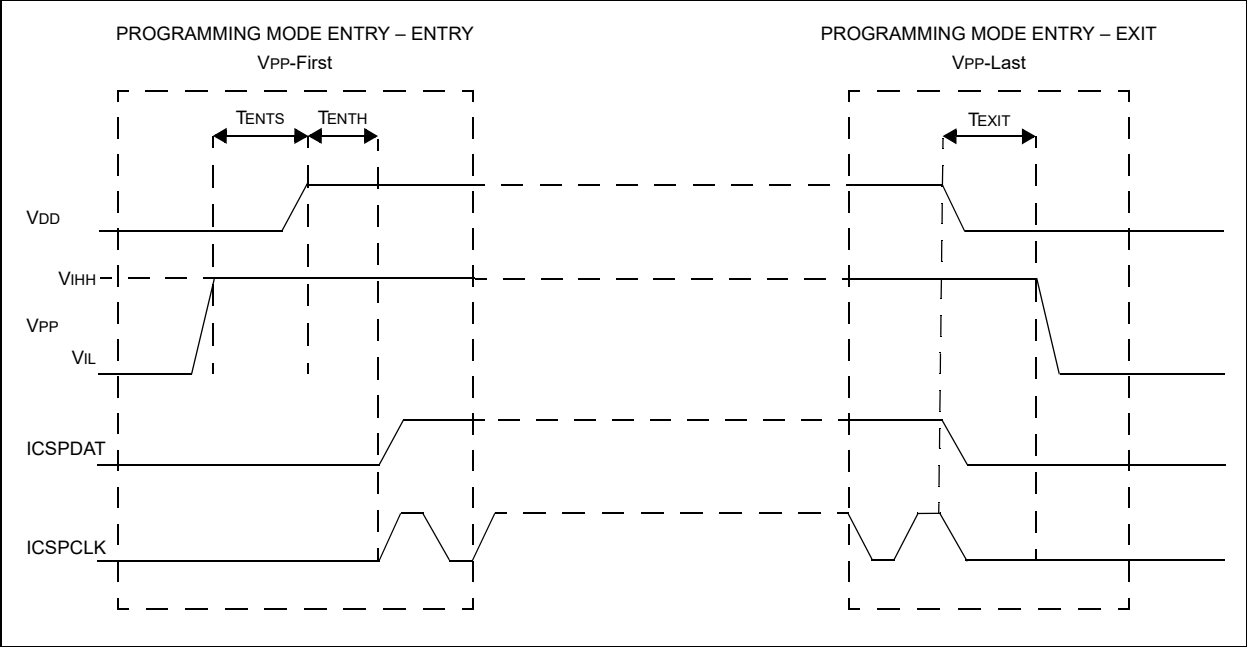
The VDD-First Entry mode is useful for programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in [Figure 3-2](#).

##### 3.1.1.3 Program/Verify Mode Exit

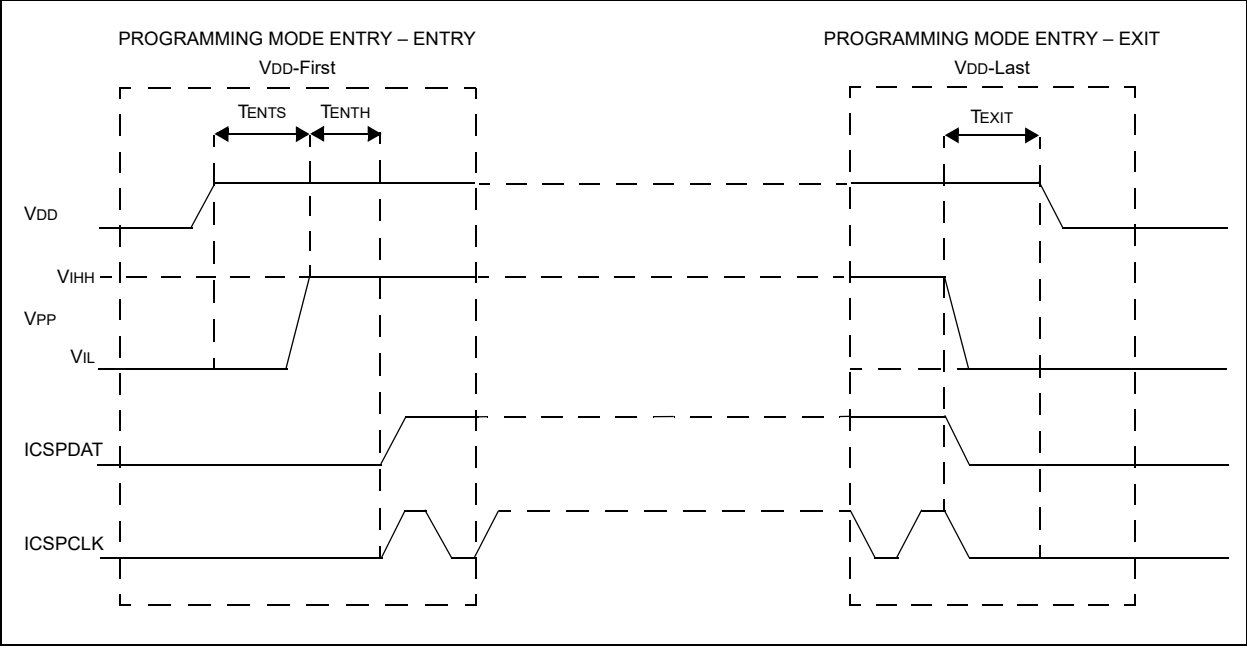
To exit Program/Verify mode, lower  $\overline{\text{MCLR}}$  from  $V_{\text{IH}}H$  or lower ( $V_{\text{IL}}$ ). VPP-First Entry mode should use VPP-Last Exit mode (see [Figure 3-1](#)). VDD-First Entry mode should use VDD-Last Exit mode (see [Figure 3-2](#)).

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**FIGURE 3-1: PROGRAMMING ENTRY AND EXIT MODES – VPP-First AND Last**



**FIGURE 3-2: PROGRAMMING ENTRY AND EXIT MODES – VDD-First AND Last**





## 3.1.2 LOW-VOLTAGE PROGRAMMING (LVP) MODE

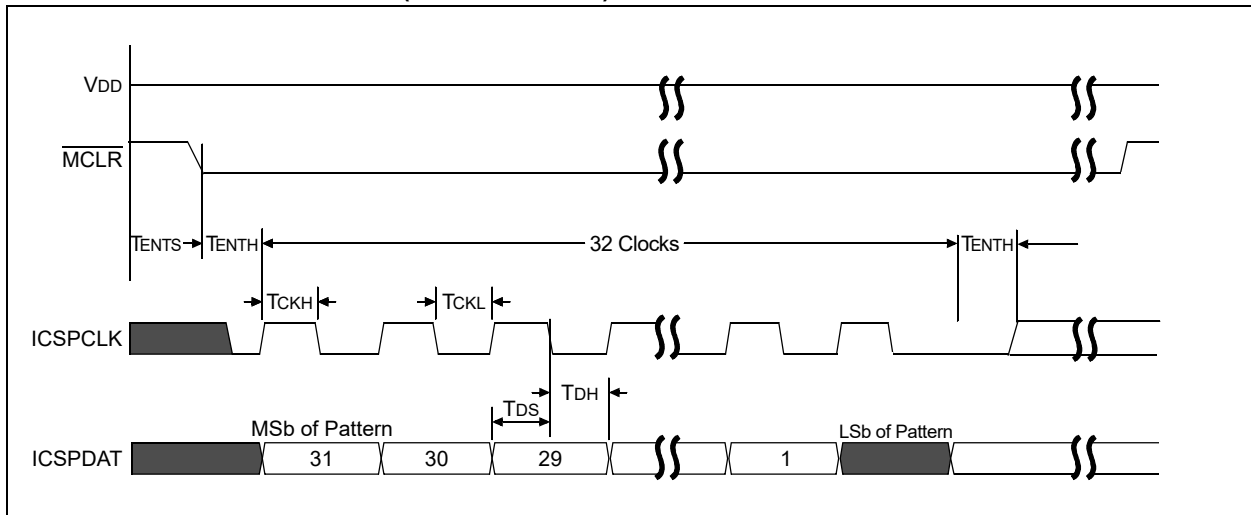
The Low-Voltage Programming mode allows the devices to be programmed using VDD only, without high voltage. When the LVP bit of the Configuration Word 4 register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

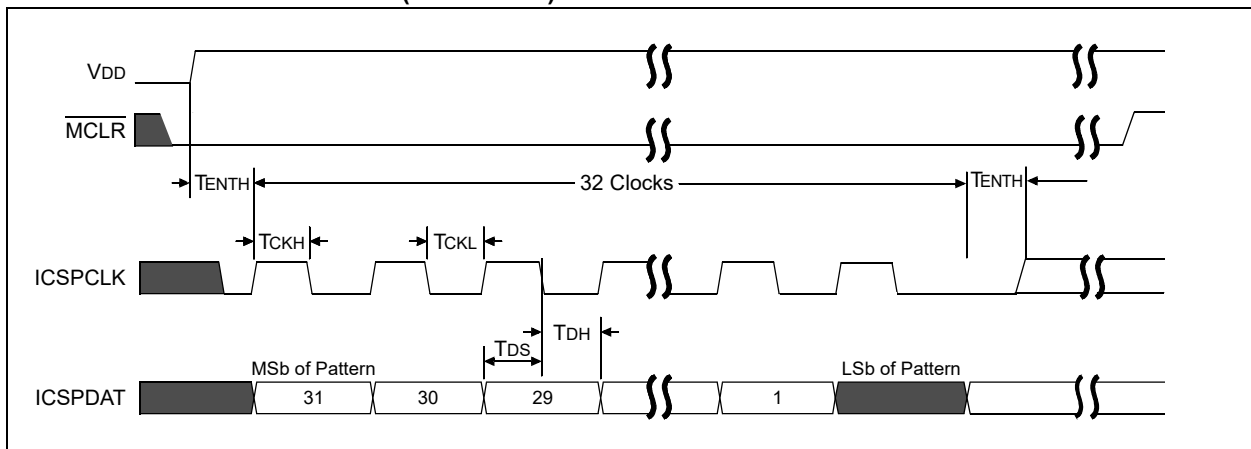
1.  $\overline{\text{MCLR}}$  is brought to VIL.
2. A **32-bit key sequence** is presented on ICSPDAT. The LSb of the pattern is a "don't care x". The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant nibble must be shifted in first. Once the key sequence is complete,  $\overline{\text{MCLR}}$  must be held at VIL for as long as Program/Verify mode is to be maintained. For Low-Voltage Programming timing, see [Figure 3-3](#) and [Figure 3-4](#).

**FIGURE 3-3: LVP ENTRY (POWERING UP)**



**FIGURE 3-4: LVP ENTRY (POWERED)**



Exiting Program/Verify mode is done by raising  $\overline{\text{MCLR}}$  from below VIL to VIH level (or higher, up to VDD).

**Note:** To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

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## 3.1.3 PROGRAM/VERIFY COMMANDS

Once a device has entered ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue six commands to the microcontroller, each eight bits in length. The commands are summarized in [Table 3-1](#). The commands are used to erase or program the device based on the location of the Program Counter (PC).

Some of the 8-bit commands also have a data payload associated with it (such as Load PC Address and Read Data from NVM).

If the programming host device issues an 8-bit command byte that has a data payload associated with it, the host device is responsible for sending an additional 24 clock pulses (for example, three 8-bit bytes) in order to send or receive the payload data associated with the command.

The payload field size is used so as to be compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, followed by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted, Most Significant bit (MSb) first.

When the programming device issues a command that involves a host to microcontroller payload (for example, Load PC Address), the Start, Stop and Pad bits should all be driven by the programmer to '0'. When the programming host device issues a command that involves microcontroller to host payload data (for example, Read Data from NVM), the Start, Stop and Pad bits should be treated as "don't care" bits and the values should be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host should wait a minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

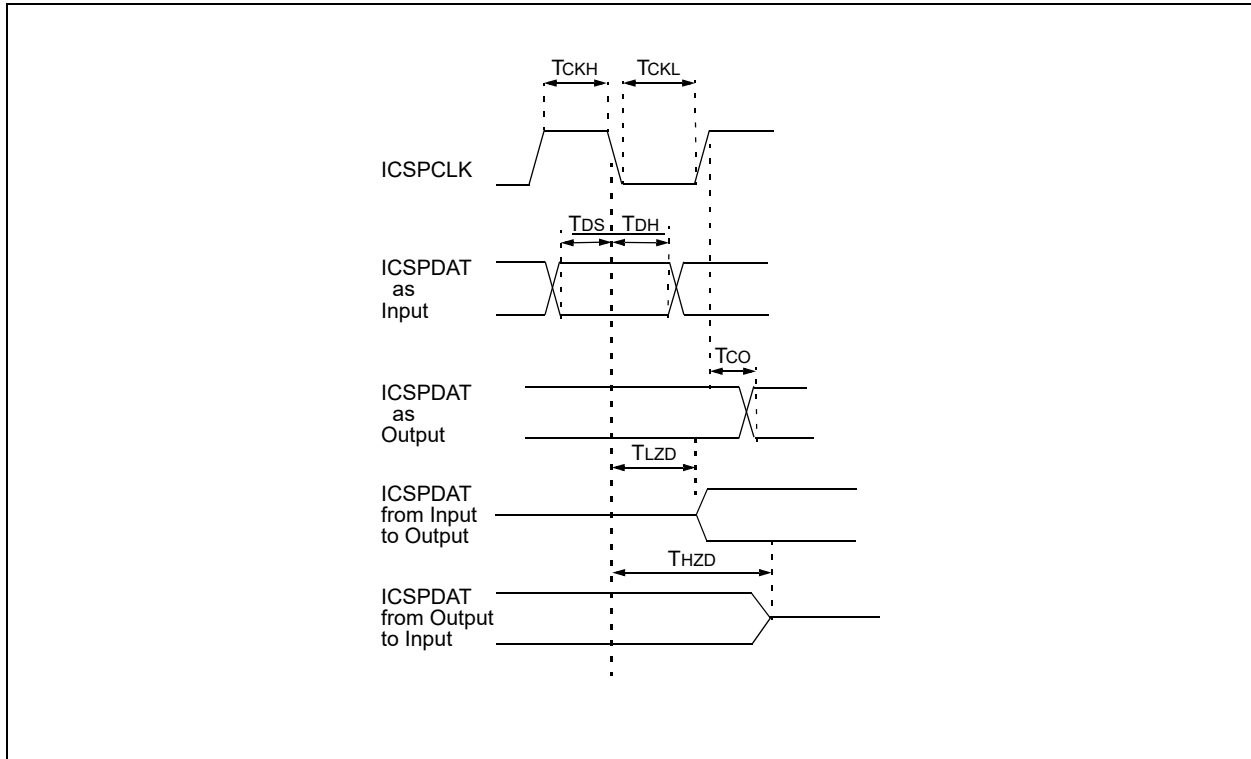
**TABLE 3-1: ICSP™ COMMAND SET SUMMARY<sup>(1)</sup>**

| Command Name                | Command Value        |       | Payload Expected | Delay after Command | Data/Note                                                                                                                |
|-----------------------------|----------------------|-------|------------------|---------------------|--------------------------------------------------------------------------------------------------------------------------|
|                             | Binary (MSb ... LSB) | Hex   |                  |                     |                                                                                                                          |
| Load PC Address             | 1000 0000            | 80    | Yes              | TDLY                | Payload Value = PC                                                                                                       |
| Bulk Erase Program Memory   | 0001 1000            | 18    | No               | TERAB               | Depending on the current value of the PC, one or more memory regions                                                     |
| Sector Erase Program Memory | 1111 0000            | F0    | No               | TERAS               | The sector addressed by the MSBs of the PC is erased; LSbs are ignored                                                   |
| Read Data from NVM          | 1111 11J0            | FC/FE | Yes              | TDLY                | Data output '0' if code-protect is enabled:<br>J = 0: PC is unchanged<br>J = 1: PC = PC + n <sup>(2)</sup> after reading |
| Increment Address           | 1111 1000            | F8    | No               | TDLY                | PC = PC + n <sup>(2)</sup>                                                                                               |
| Program Data                | 11J0 0000            | C0/E0 | Yes              | TPROG               | Payload value = Data Word<br>J = 0: PC is unchanged<br>J = 1: PC = PC + 2 after writing                                  |

**Note 1:** All clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller should latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T<sub>DS</sub> before the falling edges of ICSPCLK and should remain valid for a minimum of T<sub>DH</sub> after the falling edge of ICSPDAT. See [Figure 3-5](#).

**2:** PC is incremented by n = 1 for data memory and n = 2 for all other regions.

**FIGURE 3-5: CLOCK AND DATA TIMING**

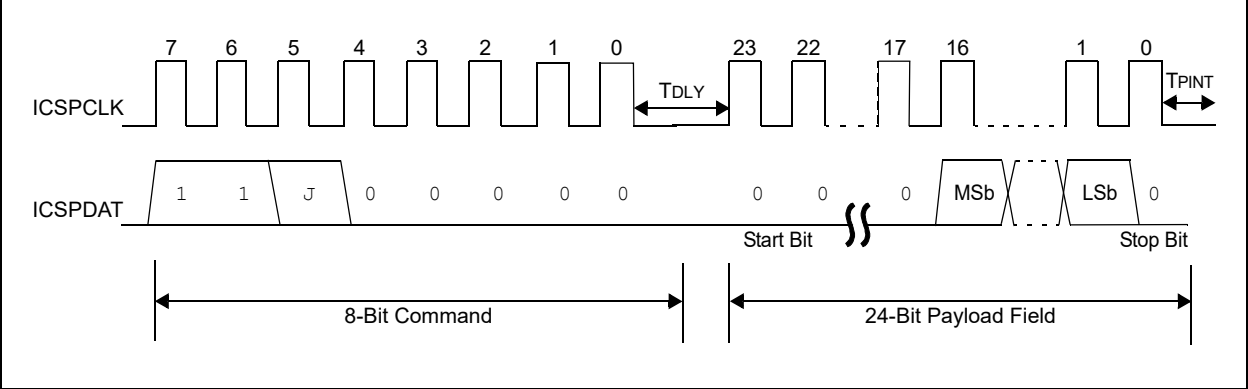


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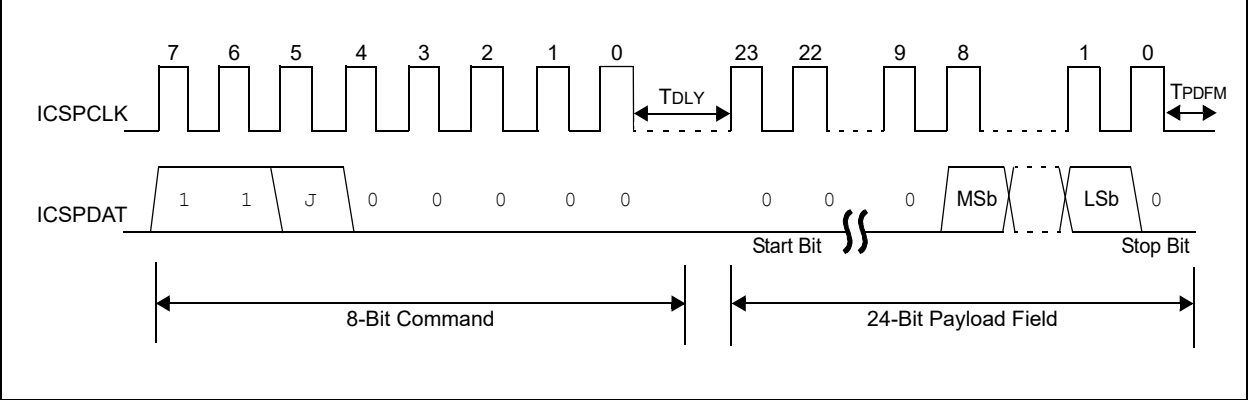
## 3.1.3.1 Program Data

The Program Data command is used to program one NVM word (for example, one 16-bit instruction word for program memory/configuration memory/User ID memory or one 8-bit data for a Data EEPROM Memory address). The payload data is written into program or EEPROM memory immediately after the Programming Data command is issued (see [Section 3.2 “Programming Algorithms”](#)). Depending on the value of bit 5 of the command, the PC may or may not be incremented (see [Table 3-1](#)).

**FIGURE 3-6: PROGRAM DATA (PROGRAM MEMORY, USER ID AND CONFIGURATION)**



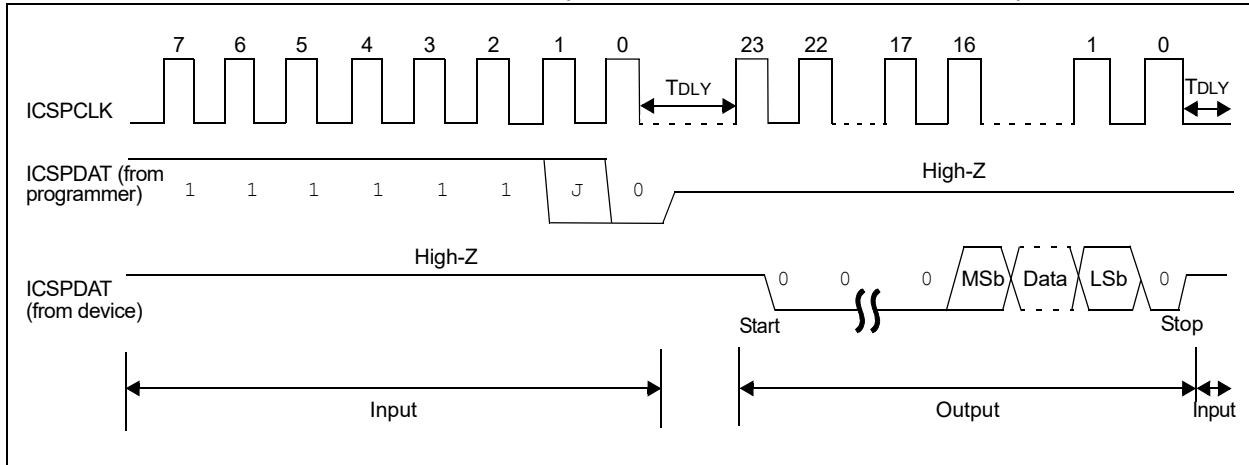
**FIGURE 3-7: PROGRAM DATA (DATA EEPROM)**



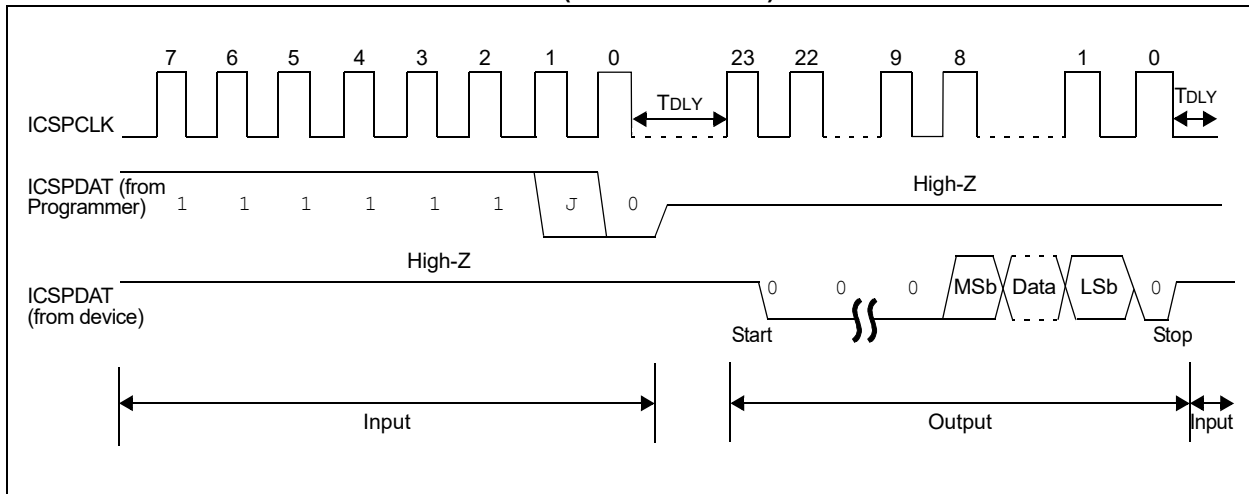
## 3.1.3.2 Read Data from NVM

The Read Data from NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of the ICSP data payload clock and it will revert to Input mode (high-impedance) after the 24th falling edge of the ICSP data payload clock. The Start and Stop bits are only one-half of a bit time wide; therefore, they should be ignored by the host programmer device, since the latched value may be indeterminate. Additionally, the host programmer device should only consider the MSb to LSb payload bits as valid and should ignore the values of the Pad bits. If the memory region is code-protected ( $\overline{CP}$  or  $\overline{DP}$ ), the data will be read as zeros (see [Figure 3-8](#) and [Figure 3-9](#)). Depending on the value of bit[1] of the command, the PC may or may not be incremented (see [Table 3-1](#)). The Read Data from NVM command can be used to read data for Program Flash Memory (see [Figure 3-8](#)) or the Data EEPROM Memory (see [Figure 3-9](#)).

**FIGURE 3-8: READ DATA FROM NVM (PFM OR CONFIGURATION WORDS)**



**FIGURE 3-9: READ DATA FROM NVM (DATA EEPROM)**

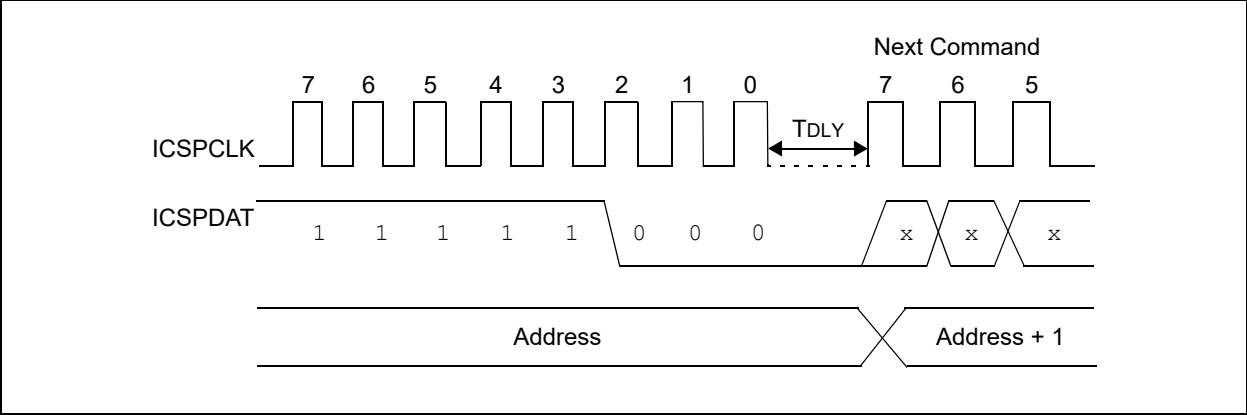


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### 3.1.3.3 Increment Address

The address is incremented when this command is received. Depending on the current value of the Program Counter, the increment varies. If the PC points to PFM, then the PC is incremented by 2; if the PC points to data EEPROM, then it is incremented by 1. It is not possible to decrement the address. To reset this counter, the user must use the Load PC Address command.

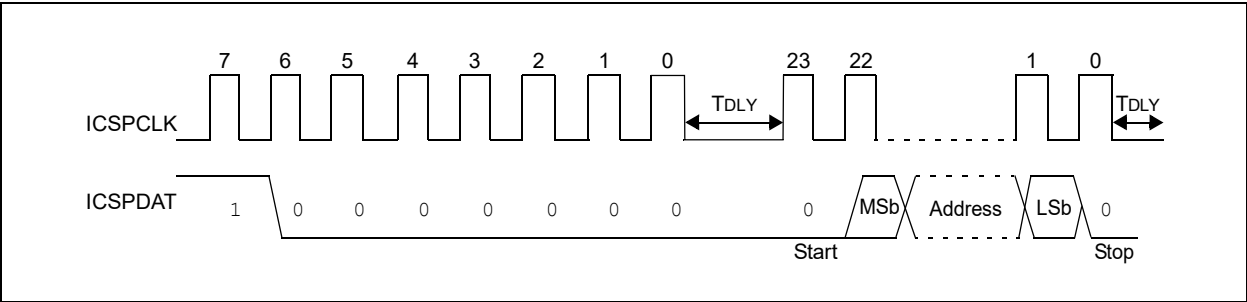
FIGURE 3-10: INCREMENT ADDRESS



### 3.1.3.4 Load PC Address

The PC value is set using the supplied data. The address implies the memory panel (PFM or Data EEPROM Memory) to be accessed (see [Figure 3-11](#)).

FIGURE 3-11: LOAD PC ADDRESS



## 3.1.3.5 Bulk Erase Program Memory

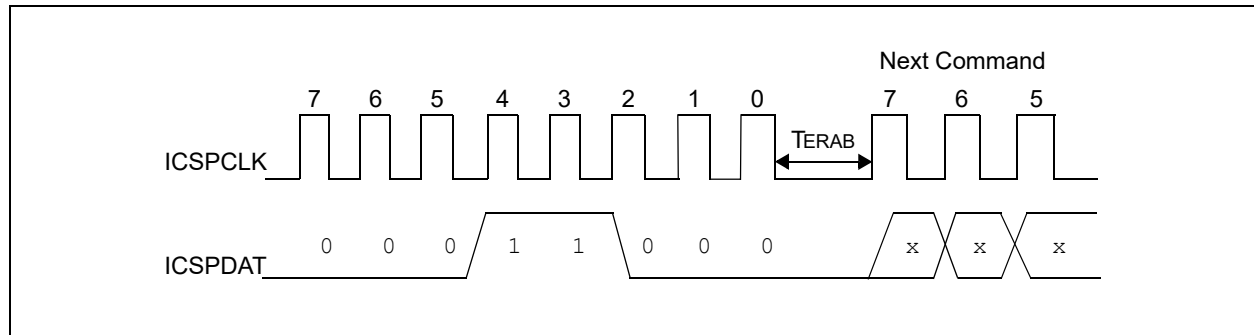
The Bulk Erase Program Memory command affects specific portions of the memory depending on the initial value of the Program Counter. Whenever a Bulk Erase command is executed, the device will erase all bytes within the regions listed in [Table 3-2](#).

**TABLE 3-2: BULK ERASE**

| Address           | Area(s) Erased                                               |                                                                             |
|-------------------|--------------------------------------------------------------|-----------------------------------------------------------------------------|
|                   | $\overline{CP} = 1$ and $\overline{CPD} = 1$ (both disabled) | $\overline{CP} = x$ or $\overline{CPD} = x$ (either enabled)                |
| 00 0000h-01 FFFFh | Program Flash Memory<br>Configuration Words                  | Program Flash Memory<br>Data EEPROM<br>Configuration Words                  |
| 20 0000h-20 00FFh | Program Flash Memory<br>User ID Words<br>Configuration Words | Program Flash Memory<br>Data EEPROM<br>User ID Words<br>Configuration Words |
| 30 0000h-30 00FFh | Program Flash Memory<br>User ID Words<br>Configuration Words | Program Flash Memory<br>Data EEPROM<br>User ID Words<br>Configuration Words |
| 31 0000h-3F FFFFh | Data EEPROM Only                                             | Data EEPROM Only                                                            |

After receiving the Bulk Erase Program Memory command, the erase will not complete until the time interval,  $T_{ERAB}$ , has expired (see [Figure 3-12](#)). The programming host device should not issue another 8-bit command until after the  $T_{ERAB}$  interval has fully elapsed.

**FIGURE 3-12: BULK ERASE MEMORY**



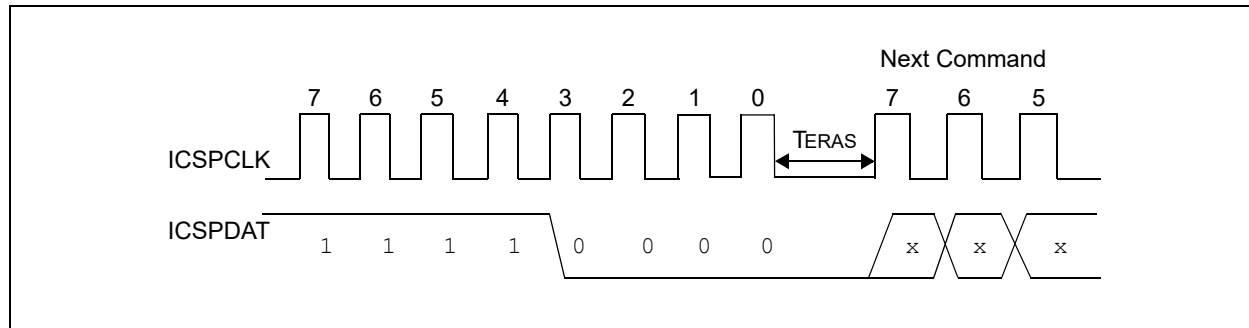
# PIC18F2X/4XQ10

## 3.1.3.6 Sector Erase Program Memory

The Sector Erase Program Memory command will erase an individual sector based on the current address of the Program Counter. If the program memory is code-protected, the Sector Erase Memory command will be ignored. The Bulk Erase command must be used to erase code-protected memory.

The Flash memory sector defined by the current PC will be erased. The user must wait T<sub>ERAS</sub> for erasing to complete (see [Figure 3-13](#)). Sector Erase should be used for program memory and User ID regions only. Configuration and data regions should be erased with the Bulk Erase method.

**FIGURE 3-13: SECTOR ERASE MEMORY**

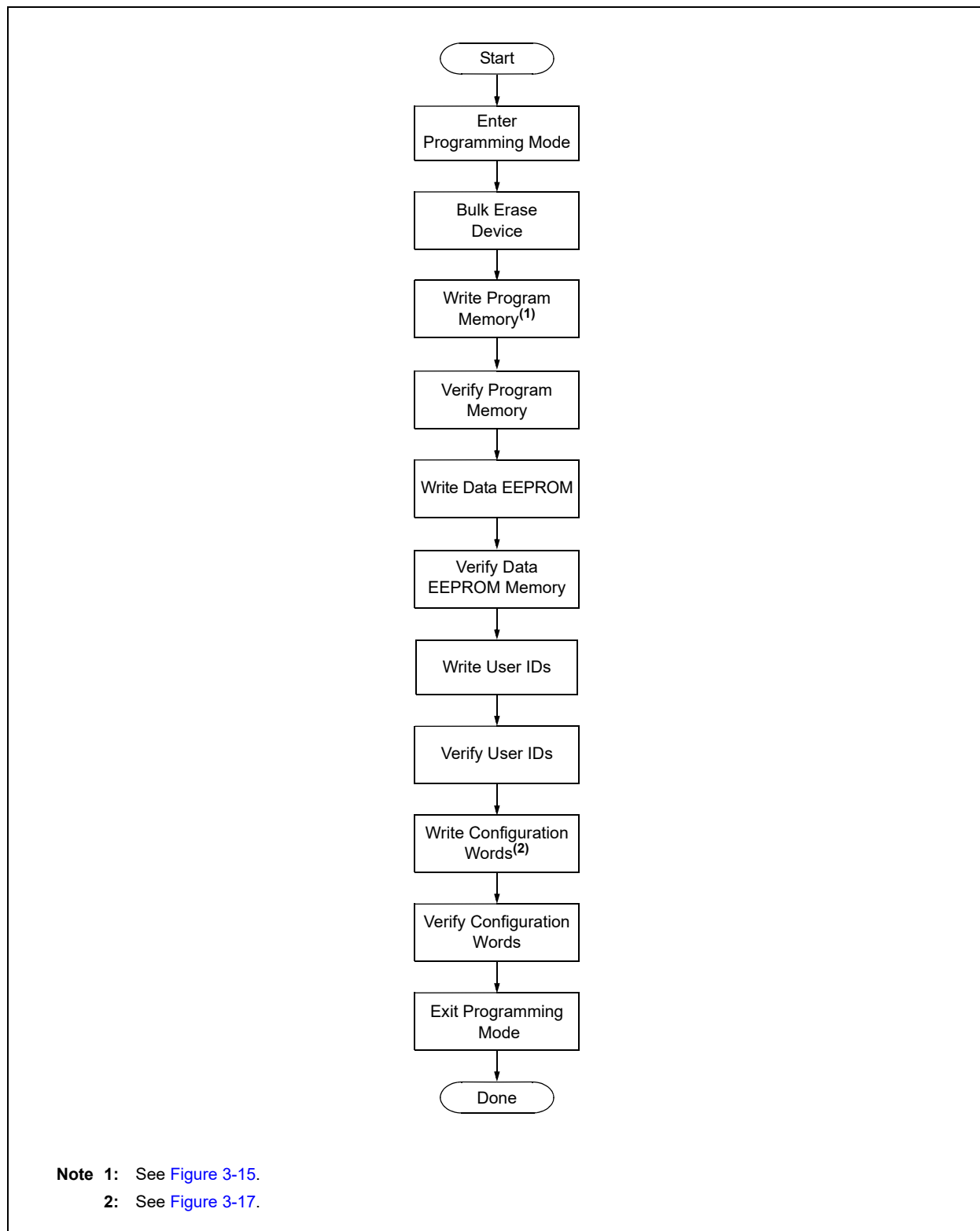




## 3.2 Programming Algorithms

The Program Flash Memory, User ID and Configuration Word regions are programmed one word at a time (Figure 3-15). The EEPROM memory is programmed one byte at a time.

**FIGURE 3-14: DEVICE PROGRAM/VERIFY FLOWCHART**



# PIC18F2X/4XQ10

FIGURE 3-15: PROGRAM MEMORY FLOWCHART

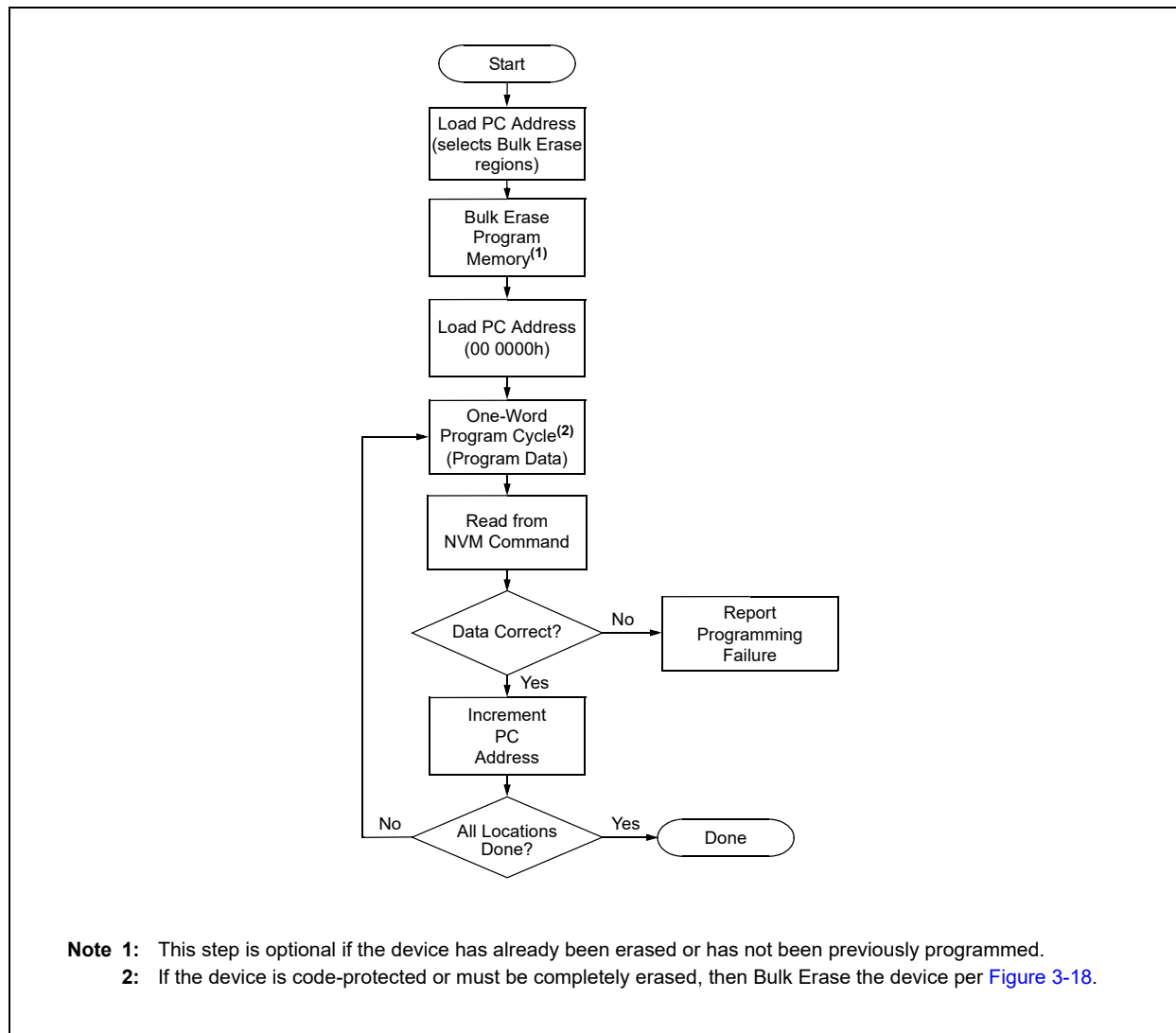
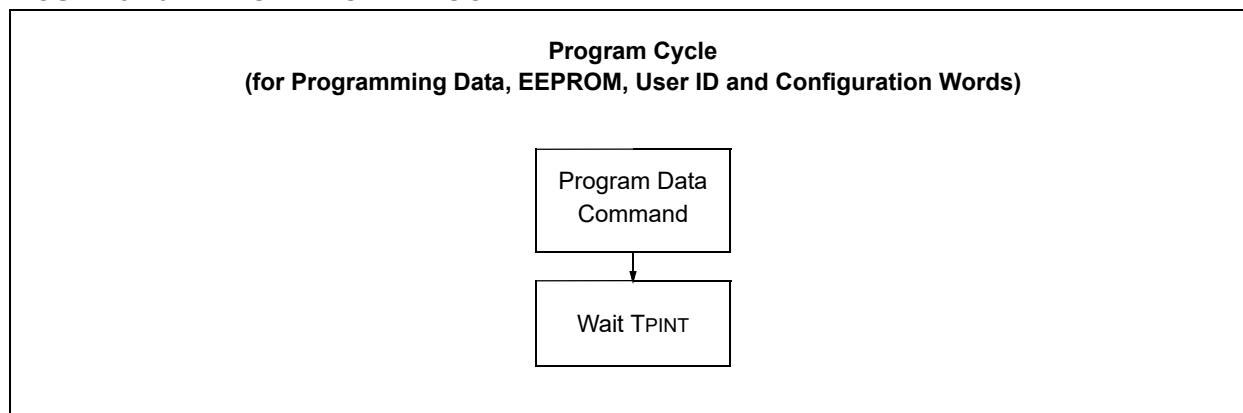
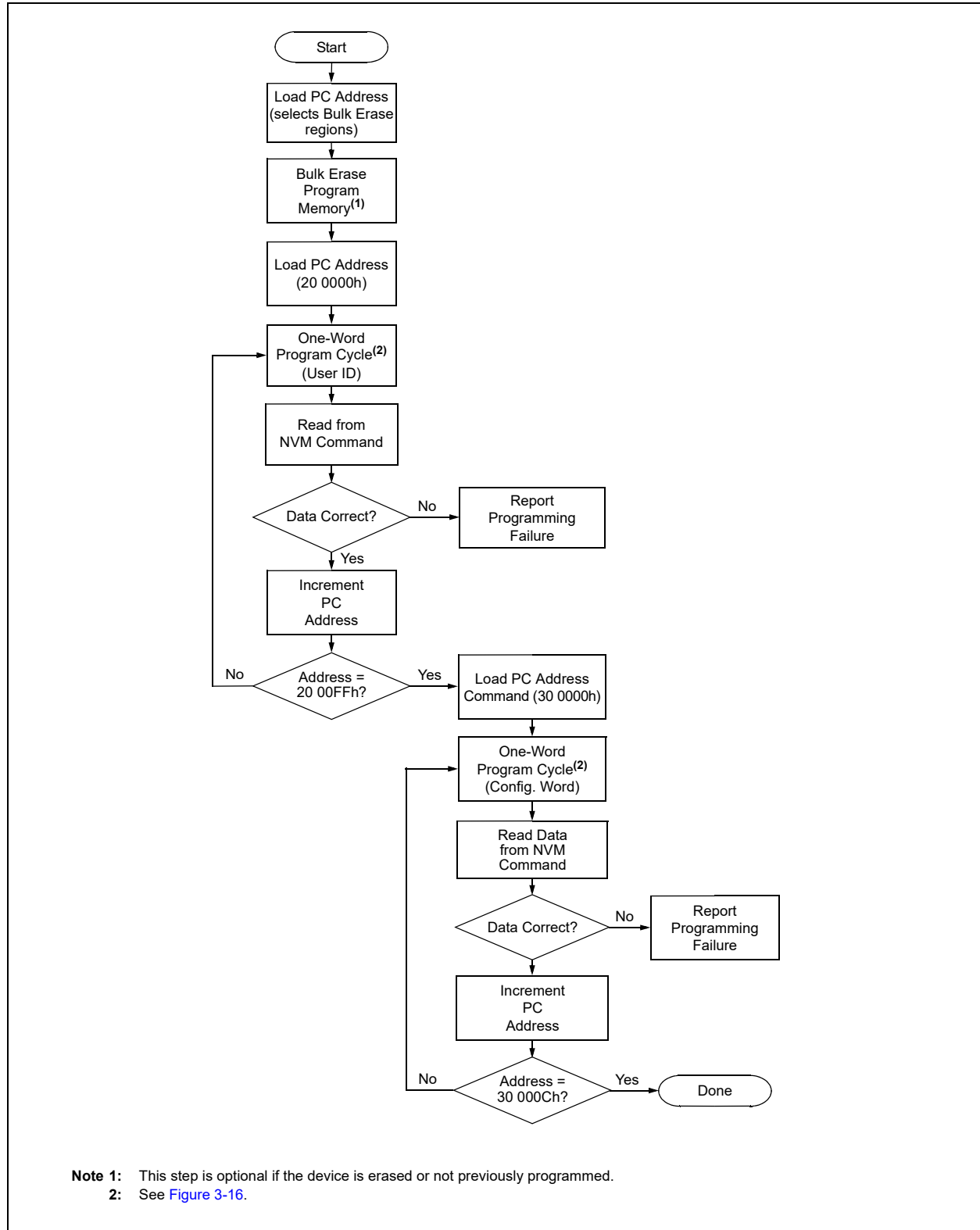


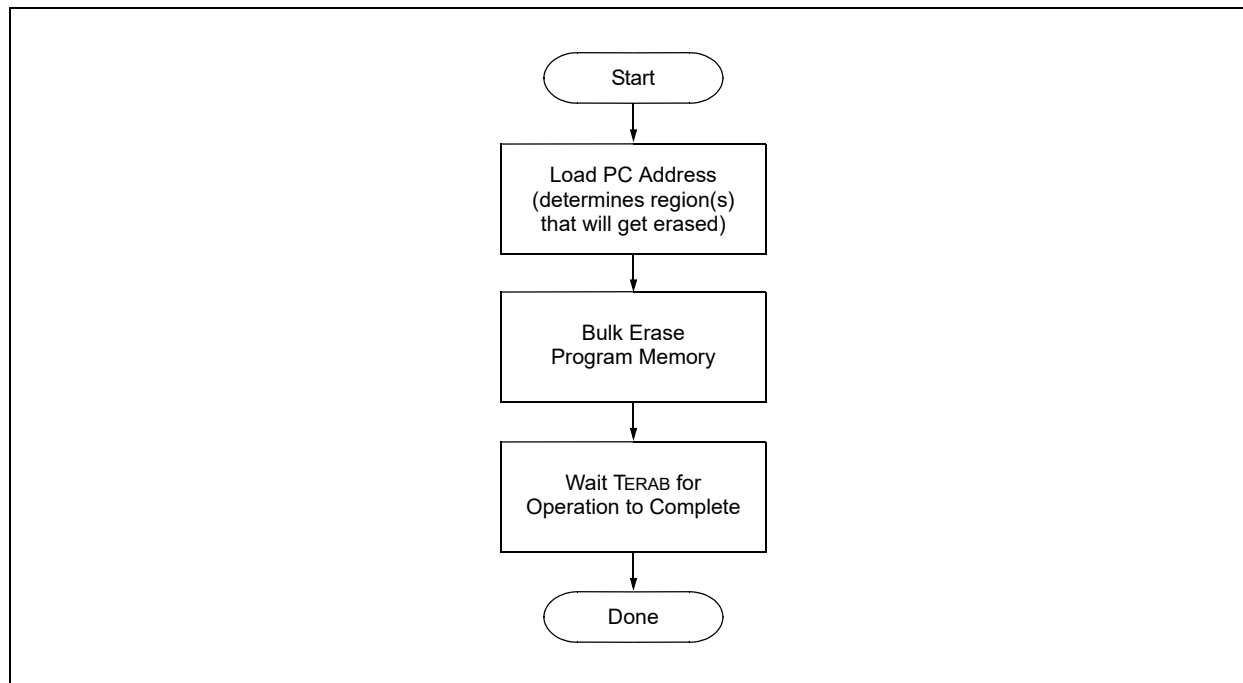
FIGURE 3-16: ONE-WORD PROGRAM CYCLE



**FIGURE 3-17: USER ID AND CONFIGURATION MEMORY PROGRAM FLOWCHART**



**FIGURE 3-18: BULK ERASE FLOWCHART**



## 3.3 Code Protection

Code protection is controlled using the  $\overline{CP}$  bit. When code protection is enabled, all program memory locations read as '0'. Further programming is disabled for the program memory until the next Bulk Erase operation is performed. Program memory can still be programmed and read during program execution.

The User ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

### 3.3.1 PROGRAM MEMORY

Code protection is enabled by programming the  $\overline{CP}$  bit to '0'. The only way to disable code protection is to use the Bulk Erase Program Memory command (with the PC set to an address so as to Bulk Erase all program Flash contents).

### 3.3.2 DATA EEPROM MEMORY

Data EEPROM Memory protection is enabled by programming the  $\overline{CPD}$  bit to '0'. The only way to disable code protection is to use the Bulk Erase Program Memory command.

## 3.4 Hex File Usage

### 3.4.1 EMBEDDING CONFIGURATION WORD INFORMATION IN THE HEX FILE

To allow portability of code, a programmer is required to read the Configuration Word locations from the Hex file. If Configuration Word information is not present in the Hex file, then a simple warning message should be issued. Similarly, while saving a Hex file, all Configuration Word information must be included. An option to not include the Configuration Word information may be provided. When embedding Configuration Word information in the Hex file, it should start at address, 300000h.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

### 3.4.2 EMBEDDING DATA EEPROM INFORMATION IN THE HEX FILE

To allow portability of code, a programmer is required to read the data EEPROM information from the Hex file. If data EEPROM information is not present, a simple warning message should be issued. Similarly, when saving a Hex file, all data EEPROM information must be included. An option to not include the data EEPROM information may be provided. When embedding data EEPROM information in the Hex file, it should start at address, 310000h.

Microchip Technology Inc. believes that this feature is important for the benefit of the end customer.

## 3.5 Checksum Computation

The checksum is calculated by two different methods, dependent on the setting of the  $\overline{\text{CP}}$  Configuration bit. Refer to [Appendix B: "PIC18F2X/4XQ10 Device ID, Checksums and Pinout Descriptions"](#) for checksum computation examples.

### 3.5.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data, starting at address, 00 0000h, up to the maximum user-addressable location (e.g., 00 FFFFh for the PIC18F46Q10 device). Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

### 3.5.2 PROGRAM CODE PROTECTION ENABLED

When the MPLAB® IDE check box for "File->Project Properties->Conf:->Building->Insert unprotected checksum in User ID memory" is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the User ID. The unprotected checksum is distributed, one nibble per ID location. Each nibble is right justified. All other User ID locations are cleared to 0x0000.

The checksum of a code-protected device is computed in the following manner:

- All of the User ID locations are added to create the sum ID
- The sum ID is then added to the Configuration bits
- All unimplemented Configuration bits are masked to '0'

**Note:** The checksum calculation differs depending on the code-protect setting. Since the code memory locations read out differently, depending on the code-protect setting, the examples in [Appendix B: "PIC18F2X/4XQ10 Device ID, Checksums and Pinout Descriptions"](#) describe how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Word and ID locations can always be read.

# PIC18F2X/4XQ10

## 4.0 ELECTRICAL SPECIFICATIONS

Refer to the device specific data sheet for absolute maximum ratings.

**TABLE 4-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE**

| AC/DC CHARACTERISTICS                           |                                                                                                        | Standard Operating Conditions<br>Production tested at +25°C |      |           |       |                        |
|-------------------------------------------------|--------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|------|-----------|-------|------------------------|
| Sym.                                            | Characteristics                                                                                        | Min.                                                        | Typ. | Max.      | Units | Conditions/Comments    |
| <b>Programming Supply Voltages and Currents</b> |                                                                                                        |                                                             |      |           |       |                        |
| VDD                                             | Supply Voltage (VDDMIN, VDDMAX)                                                                        | 1.80                                                        | —    | 5.50      | V     | (Note 1)               |
| VPEW                                            | Read/Write and Sector Erase Operations                                                                 | VDDMIN                                                      | —    | VDDMAX    | V     |                        |
| VBE                                             | Bulk Erase Operations                                                                                  | VBORMAX                                                     | —    | VDDMAX    | V     | (Note 2)               |
| IDDI                                            | Current on VDD, Idle                                                                                   | —                                                           | —    | 1.0       | mA    |                        |
| IDDP                                            | Current on VDD, Programming                                                                            | —                                                           | —    | 10        | mA    |                        |
| <b>VPP</b>                                      |                                                                                                        |                                                             |      |           |       |                        |
| IPP                                             | Current on $\overline{\text{MCLR}}$ /VPP                                                               | —                                                           | —    | 600       | μA    |                        |
| VIHH                                            | High Voltage on $\overline{\text{MCLR}}$ /VPP for Program/Verify Mode Entry                            | 7.9                                                         | —    | 9.0       | V     |                        |
| TVHHR                                           | $\overline{\text{MCLR}}$ Rise Time (VIL to VIHH) for Program/Verify Mode Entry                         | —                                                           | —    | 1.0       | μs    |                        |
| <b>I/O Pins</b>                                 |                                                                                                        |                                                             |      |           |       |                        |
| VIH                                             | (ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}$ /VPP) Input High Level                                     | 0.8 VDD                                                     | —    | VDD       | V     |                        |
| VIL                                             | (ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}$ /VPP) Input Low Level                                      | VSS                                                         | —    | 0.2 VDD   | V     |                        |
| VOH                                             | ICSPDAT Output High Level                                                                              | VDD – 0.7                                                   | —    | —         | V     | IOH = 3 mA, VDD = 3.0V |
| VOL                                             | ICSPDAT Output Low Level                                                                               | —                                                           | —    | VSS + 0.6 | V     | IOL = 6 mA, VDD = 3.0V |
| <b>Programming Mode Entry and Exit</b>          |                                                                                                        |                                                             |      |           |       |                        |
| TENTS                                           | Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before VDD or $\overline{\text{MCLR}}$ ↑ | 100                                                         | —    | —         | ns    |                        |
| TENTH                                           | Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time after VDD or $\overline{\text{MCLR}}$ ↑    | 1                                                           | —    | —         | ms    |                        |
| <b>Serial Program/Verify</b>                    |                                                                                                        |                                                             |      |           |       |                        |
| TCKL                                            | Clock Low Pulse Width                                                                                  | 100                                                         | —    | —         | ns    |                        |
| TCKH                                            | Clock High Pulse Width                                                                                 | 100                                                         | —    | —         | ns    |                        |
| TDS                                             | Data in Setup Time before Clock↓                                                                       | 100                                                         | —    | —         | ns    |                        |
| TDH                                             | Data in Hold Time after Clock↓                                                                         | 100                                                         | —    | —         | ns    |                        |
| Tco                                             | Clock↑ to Data Out Valid (during a Read Data command)                                                  | 0                                                           | —    | 80        | ns    |                        |

- Note 1:** Bulk Erased devices default to Brown-out Reset enabled with BORV = 'b11 (low trip point). VDDMIN is the VBOR threshold (with BORV = 'b11) when performing Low-Voltage Programming on a Bulk Erased device to ensure that the device is not held in Brown-out Reset.
- 2:** In high voltage test mode entry, the hardware requires VDD to be above the lowest available BOR threshold, ~1.9V nominal setting, in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the VBOR level.
- 3:**  $n$  = number of bytes in the data memory. Bulk Erase of data memory includes an additional write of FFh for each byte in the data memory.

**TABLE 4-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE (CONTINUED)**

| AC/DC CHARACTERISTICS |                                                                                                    | Standard Operating Conditions<br>Production tested at +25°C |      |      |       |                        |
|-----------------------|----------------------------------------------------------------------------------------------------|-------------------------------------------------------------|------|------|-------|------------------------|
| Sym.                  | Characteristics                                                                                    | Min.                                                        | Typ. | Max. | Units | Conditions/Comments    |
| TLZD                  | Clock↓ to Data Low-Impedance (during a Read Data from NVM command)                                 | 0                                                           | —    | 80   | ns    |                        |
| THZD                  | Clock↓ to Data High-Impedance (during a Read Data from NVM command)                                | 0                                                           | —    | 80   | ns    |                        |
| TDLY                  | Data Input not Driven to Next Clock Input (delay required between command/data or command/command) | 1.0                                                         | —    | —    | μs    |                        |
| TERAB                 | Bulk Erase Cycle Time                                                                              | —                                                           | —    | 75   | ms    | Program, Config and ID |
| TERAS                 | Sector Erase Cycle Time                                                                            | —                                                           | —    | 11   | ms    |                        |
| TPDFM                 | Internally Timed DFM (EEPROM) Programming Operation Time                                           | —                                                           | —    | 11   | ms    | EEPROM memory          |
| TPINT                 | Internally Timed Programming Operation Time                                                        | —                                                           | —    | 65   | μs    | Program memory         |
| TEXIT                 | Time Delay when Exiting Program/Verify Mode                                                        | 1                                                           | —    | —    | μs    |                        |

- Note 1:** Bulk Erased devices default to Brown-out Reset enabled with BORV = 'b11 (low trip point). VDDMIN is the VBOR threshold (with BORV = 'b11) when performing Low-Voltage Programming on a Bulk Erased device to ensure that the device is not held in Brown-out Reset.
- 2:** In high voltage test mode entry, the hardware requires VDD to be above the lowest available BOR threshold, ~1.9V nominal setting, in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the VBOR level.
- 3:** *n* = number of bytes in the data memory. Bulk Erase of data memory includes an additional write of FFh for each byte in the data memory.

# PIC18F2X/4XQ10

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## APPENDIX A: REVISION HISTORY

### Revision G (3/2019)

Updated Examples B-3 and B-4; and Section 3.5.2.

### Revision F (10/2018)

Updated Table 3-3 - TPINT.

### Revision E (5/2018)

Updated Table B-1.

### Revision D (4/2018)

Updated Figure 2-1; Register B-1; and Tables 2-1, 3-1, 3-2, B-1, B-2 and B-3.

### Revision C (11/2017)

Updated Figures 3-3 and 3-4 and Table 3-3.

### Revision B (08/2017)

Updated Figure 3-7. Updated Table 3-3; adding TPDFM.

### Revision A (02/2017)

Initial release of the document.



**APPENDIX B: PIC18F2X/4XQ10 DEVICE ID, CHECKSUMS AND PINOUT DESCRIPTIONS****TABLE B-1: CONFIGURATION WORD AND MASK**

| Device      | Device ID | Config. 1L |            | Config. 1H |            | Config. 2L |            | Config. 2H |            | Config. 3L |            | Config. 3H |            | Config. 4L |            | Config. 4H |            | Config. 5L  |                |            | Config. 5H  |                |            | Config. 6L |            | Config. 6H |            |
|-------------|-----------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|----------------|------------|-------------|----------------|------------|------------|------------|------------|------------|
|             |           | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Word (Hex) | Mask (Hex) | Unprotected | Code-Protected | Mask (Hex) | Unprotected | Code-Protected | Mask (Hex) | Word       | Mask (Hex) | Word       | Mask (Hex) |
| PIC18F46Q10 | 7120h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | 0F         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | 0F         | FF         | 02         |
| PIC18F45Q10 | 7140h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | 0F         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | 0F         | FF         | 02         |
| PIC18F26Q10 | 7180h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | 0F         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | 0F         | FF         | 02         |
| PIC18F25Q10 | 71A0h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | 0F         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | 0F         | FF         | 02         |
| PIC18F24Q10 | 71C0h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | 03         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | 03         | FF         | 02         |
| PIC18F27Q10 | 7100h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | FF         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | FF         | FF         | 02         |
| PIC18F47Q10 | 70E0h     | FF         | 77         | FF         | 29         | FF         | E3         | FF         | BF         | FF         | 7F         | FF         | 3F         | FF         | FF         | FF         | 37         | FF          | FE             | 03         | FF          | FF             | 00         | FF         | FF         | FF         | 02         |

# PIC18F2X/4XQ10

**TABLE B-2: CHECKSUM VALUES**

| Device      | Checksum    |                                |                |                                 |
|-------------|-------------|--------------------------------|----------------|---------------------------------|
|             | Unprotected |                                | Code-Protected |                                 |
|             | Blank       | 0AAh at First and Last Address | Blank          | 00AAh at First and Last Address |
| PIC18F46Q10 | 035A        | 02B0                           | 036B           | 0366                            |
| PIC18F45Q10 | 835A        | 82B0                           | 0373           | 036E                            |
| PIC18F26Q10 | 035A        | 02B0                           | 036B           | 0366                            |
| PIC18F25Q10 | 835A        | 82B0                           | 0373           | 036E                            |
| PIC18F24Q10 | C342        | C298                           | 0356           | 0360                            |
| PIC18F27Q10 | 053A        | 0490                           | 054B           | 0546                            |
| PIC18F47Q10 | 053A        | 0490                           | 054B           | 0546                            |

**EXAMPLE B-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED:  
PIC18F24Q10, BLANK DEVICE**

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                             |                       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|-----------------------|
| <b>PIC18F24Q10</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Sum of Memory Addresses from 0000h to 3FFFh | C000h (4000h * 00FFh) |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 1L                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 1L Mask                  | 77h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 1H                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 1H Mask                  | 29h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 2L                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 2L Mask                  | E3h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 2H                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 2H Mask                  | BFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 3L                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 3L Mask                  | 7Fh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 3H                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 3H Mask                  | 3Fh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 4L                       | 03h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 4L Mask                  | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 4H                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 4H Mask                  | 37h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 5L Unprotected           | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 5L Mask                  | 03h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 5H Unprotected           | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 5H Mask                  | 00h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 6L                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 6L Mask                  | 03h                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 6H                       | FFh                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Configuration Word 6H Mask                  | 02h                   |
| $\begin{aligned} \text{Checksum} &= \text{C000h} + (\text{FFh AND } 77\text{h}) + (\text{FFh AND } 29\text{h}) + (\text{FFh AND } \text{E3h}) + (\text{FFh AND } \text{BFh}) + \\ &\quad (\text{FFh AND } 7\text{Fh}) + (\text{FFh AND } 3\text{Fh}) + (\text{FFh AND } 03\text{h}) + (\text{FFh AND } 37\text{h}) + \\ &\quad (\text{FFh AND } 03\text{h}) + (\text{FFh AND } 00\text{h}) + (\text{FFh AND } 03\text{h}) + (\text{FFh AND } 02\text{h}) \\ &= \text{C000h} + 77\text{h} + 29\text{h} + \text{E3h} + \text{BFh} + 7\text{Fh} + 3\text{Fh} + 03\text{h} + 37\text{h} + 03\text{h} + 00\text{h} + 03\text{h} + 02\text{h} \\ &= \text{C342h} \end{aligned}$ |                                             |                       |

# PIC18F2X/4XQ10

## EXAMPLE B-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED: PIC18F24Q10, 00AAh AT FIRST AND LAST ADDRESS

|                                                                                                                                                                                                                                                                                                                          |                                             |                                     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|-------------------------------------|
| <b>PIC18F24Q10</b>                                                                                                                                                                                                                                                                                                       | Sum of Memory Addresses from 0000h to 3FFFh | BF56h (AAh + (3FFEh * 00FFh) + AAh) |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 1L                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 1L Mask                  | 77h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 1H                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 1H Mask                  | 29h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 2L                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 2L Mask                  | E3h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 2H                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 2H Mask                  | BFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 3L                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 3L Mask                  | 7Fh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 3H                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 3H Mask                  | 3Fh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 4L                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 4L Mask                  | 03h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 4H                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 4H Mask                  | 37h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 5L Unprotected           | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 5L Mask                  | 03h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 5H Unprotected           | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 5H Mask                  | 00h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 6L                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 6L Mask                  | 03h                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 6H                       | FFh                                 |
|                                                                                                                                                                                                                                                                                                                          | Configuration Word 6H Mask                  | 02h                                 |
| <br>Checksum = BF56h + (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh) +<br>(FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 03h) + (FFh AND 37h) +<br>(FFh AND 03h) + (FFh AND 00h) + (FFh AND 03h) + (FFh AND 02h)<br>= BF56h + 77h + 29h + E3h + BFh + 7Fh + 3Fh + 03h + 37h + 03h + 00h + 03h + 02h<br>= C298h |                                             |                                     |

**EXAMPLE B-3: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED:  
PIC18F24Q10, BLANK DEVICE**

|                    |                                 |     |
|--------------------|---------------------------------|-----|
| <b>PIC18F24Q10</b> | Configuration Word 1L           | FFh |
|                    | Configuration Word 1L Mask      | 77h |
|                    | Configuration Word 1H           | FFh |
|                    | Configuration Word 1H Mask      | 29h |
|                    | Configuration Word 2L           | FFh |
|                    | Configuration Word 2L Mask      | E3h |
|                    | Configuration Word 2H           | FFh |
|                    | Configuration Word 2H Mask      | BFh |
|                    | Configuration Word 3L           | FFh |
|                    | Configuration Word 3L Mask      | 7Fh |
|                    | Configuration Word 3H           | FFh |
|                    | Configuration Word 3H Mask      | 3Fh |
|                    | Configuration Word 4L           | FFh |
|                    | Configuration Word 4L Mask      | 03h |
|                    | Configuration Word 4H           | FFh |
|                    | Configuration Word 4H Mask      | 37h |
|                    | Configuration Word 5L Protected | FEh |
|                    | Configuration Word 5L Mask      | 03h |
|                    | Configuration Word 5H Protected | FFh |
|                    | Configuration Word 5H Mask      | 00h |
|                    | Configuration Word 6L           | FFh |
|                    | Configuration Word 6L Mask      | 03h |
|                    | Configuration Word 6H           | FFh |
|                    | Configuration Word 6H Mask      | 02h |

Checksum = (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh) +  
 (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 03h) + (FFh AND 37h) +  
 (FEh AND 03h) + (FFh AND 00h) + (FFh AND 03h) + (FFh AND 02h) + SUM\_ID  
 = 77h + 29h + E3h + BFh + 7Fh + 3Fh + 03h + 37h + 02h + 00h + 03h + 02h + 0015h  
 = 0356h

SUM\_ID = Bitwise sum of lower four bits of all User ID locations

SUM\_ID = 000Ch + 0003h + 0004h + 0002h + 0000h + 0000h + ... + 0000h + 0000h = 0015h

# PIC18F2X/4XQ10

## EXAMPLE B-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED: PIC18F24Q10, 00AAh AT FIRST AND LAST ADDRESS

|                    |                                                                                                                                                                                                                                                                                                                       |     |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| <b>PIC18F24Q10</b> | Configuration Word 1L                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 1L Mask                                                                                                                                                                                                                                                                                            | 77h |
|                    | Configuration Word 1H                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 1H Mask                                                                                                                                                                                                                                                                                            | 29h |
|                    | Configuration Word 2L                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 2L Mask                                                                                                                                                                                                                                                                                            | E3h |
|                    | Configuration Word 2H                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 2H Mask                                                                                                                                                                                                                                                                                            | BFh |
|                    | Configuration Word 3L                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 3L Mask                                                                                                                                                                                                                                                                                            | 7Fh |
|                    | Configuration Word 3H                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 3H Mask                                                                                                                                                                                                                                                                                            | 3Fh |
|                    | Configuration Word 4L                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 4L Mask                                                                                                                                                                                                                                                                                            | 03h |
|                    | Configuration Word 4H                                                                                                                                                                                                                                                                                                 | FFh |
|                    | Configuration Word 4H Mask                                                                                                                                                                                                                                                                                            | 37h |
|                    | Configuration Word 5L Protected                                                                                                                                                                                                                                                                                       | FEh |
|                    | Configuration Word 5L Mask                                                                                                                                                                                                                                                                                            | 03h |
|                    | Configuration Word 5H Protected                                                                                                                                                                                                                                                                                       | FFh |
|                    | Configuration Word 5H Mask                                                                                                                                                                                                                                                                                            | 00h |
|                    | Configuration Word 6L Protected                                                                                                                                                                                                                                                                                       | FFh |
|                    | Configuration Word 6L Mask                                                                                                                                                                                                                                                                                            | 03h |
|                    | Configuration Word 6H Protected                                                                                                                                                                                                                                                                                       | FFh |
|                    | Configuration Word 6H Mask                                                                                                                                                                                                                                                                                            | 02h |
|                    | Checksum = (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh) +<br>(FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 03h) + (FFh AND 37h) +<br>(FEh AND 03h) + (FFh AND 00h) + (FFh AND 03h) + (FFh AND 02h) + SUM_ID<br>= 77h + 29h + E3h + BFh + 7Fh + 3Fh + 03h + 37h + 02h + 00h + 03h + 02h + 001Fh<br>= 0360h |     |
|                    | SUM_ID = Bitwise sum of lower four bits of all User ID locations                                                                                                                                                                                                                                                      |     |
|                    | SUM_ID = 000Ch + 0002h + 0009h + 0008h + 0000h + 0000h + ... + 0000h + 0000h = 001Fh                                                                                                                                                                                                                                  |     |

**TABLE B-3: PROGRAMMING PIN LOCATIONS BY PACKAGE TYPE**

| Device      | Package      | Package Code | Package Drawing Number <sup>(1)</sup> | VDD   | VSS   | MCLR |      | ICSPCLK |      | ICSPDAT |      |
|-------------|--------------|--------------|---------------------------------------|-------|-------|------|------|---------|------|---------|------|
|             |              |              |                                       | PIN   | PIN   | PIN  | PORT | PIN     | PORT | PIN     | PORT |
| PIC18F24Q10 | 28-Pin SPDIP | (SP)         | C04-070                               | 20    | 19,8  | 1    | RE3  | 27      | RB6  | 28      | RB7  |
| PIC18F25Q10 | 28-Pin SOIC  | (SO)         | C04-052                               | 20    | 19,8  | 1    | RE3  | 27      | RB6  | 28      | RB7  |
| PIC18F26Q10 | 28-Pin SSOP  | (SS)         | C04-073                               | 20    | 19,8  | 1    | RE3  | 27      | RB6  | 28      | RB7  |
| PIC18F27Q10 | 28-Pin VQFN  | (STX)        | C04-456                               | 17    | 16,5  | 26   | RE3  | 24      | RB6  | 25      | RB7  |
| PIC18F45Q10 | 40-Pin PDIP  | (P)          | C04-016                               | 32,11 | 31,12 | 1    | RE3  | 39      | RB6  | 40      | RB7  |
| PIC18F46Q10 | 40-Pin QFN   | (MP)         | C04-047                               | 26,7  | 27,6  | 16   | RE3  | 14      | RB6  | 15      | RB7  |
| PIC18F47Q10 | 44-Pin TQFP  | (PT)         | C04-076                               | 28,7  | 29,6  | 18   | RE3  | 16      | RB6  | 17      | RB7  |

**Note 1:** The most current package drawings can be found in the Microchip Packaging Specification, DS00000049, found at <http://www.microchip.com/packaging>. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

TABLE B-4: SUMMARY OF CONFIGURATION WORDS

| Address  | Name      | Bit 7  | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2    | Bit 1    | Bit 0    | Default/<br>Unprogrammed<br>Value |
|----------|-----------|--------|---------|---------|---------|---------|----------|----------|----------|-----------------------------------|
| 30 0000h | CONFIG 1L | —      | RSTOSC2 | RSTOSC1 | RSTOSC0 | —       | FEXTOSC2 | FEXTOSC1 | FEXTOSC0 | 1111 1111                         |
| 30 0001h | CONFIG 1H | —      | —       | FCMEN   | —       | CSWEN   | —        | —        | CLKOUTEN | 1111 1111                         |
| 30 0002h | CONFIG 2L | BOREN1 | BOREN0  | LPBOREN | —       | —       | —        | PWRTE    | MCLRE    | 1111 1111                         |
| 30 0003h | CONFIG 2H | XINST  | —       | DEBUG   | STVREN  | PPS1WAY | ZCDDIS   | BORV1    | BORV0    | 1111 1111                         |
| 30 0004h | CONFIG 3L | —      | WDTE1   | WDTE0   | WDTCP4  | WDTCP3  | WDTCP2   | WDTCP1   | WDTCP0   | 1111 1111                         |
| 30 0005h | CONFIG 3H | —      | —       | WDTCCS2 | WDTCCS1 | WDTCCS0 | WDTCCS2  | WDTCCS1  | WDTCCS0  | 1111 1111                         |
| 30 0006h | CONFIG 4L | WRT7   | WRT6    | WRT5    | WRT4    | WRT3    | WRT2     | WRT1     | WRT0     | 1111 1111                         |
| 30 0007h | CONFIG 4H | —      | —       | LVP     | SCANE   | —       | WRD      | WRTB     | WRTC     | 1111 1111                         |
| 30 0008h | CONFIG 5L | —      | —       | —       | —       | —       | —        | CPD      | CP       | 1111 1111                         |
| 30 000Ah | CONFIG 6L | EBTR7  | EBTR6   | EBTR5   | EBTR4   | EBTR3   | EBTR2    | EBTR1    | EBTR0    | 1111 1111                         |
| 30 000Bh | CONFIG 6H | —      | —       | —       | —       | —       | —        | EBTRB    | —        | 1111 1111                         |



## REGISTER B-1: CONFIGURATION WORD 1L (30 0000h) – OSCILLATORS

| U-1   | R/W-1   | R/W-1   | R/W-1   | U-1   | R/W-1    | R/W-1    | R/W-1    |
|-------|---------|---------|---------|-------|----------|----------|----------|
| —     | RSTOSC2 | RSTOSC1 | RSTOSC0 | —     | FEXTOSC2 | FEXTOSC1 | FEXTOSC0 |
| bit 7 |         |         |         | bit 0 |          |          |          |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '1'

-n = Value for blank device

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '1'

bit 6-4 **RSTOSC[2:0]:** Power-up Default Value for COSC bits

This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

111 = EXTOSC operating per FEXTOSC[2:0] bits (device manufacturing default)

110 = HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1

101 = LFINTOSC

100 = SOSC

011 = Reserved

010 = EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC[2:0] bits

001 = Reserved

000 = HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1; resets COSC/NOSC to 3'b110

bit 3 **Unimplemented:** Read as '1'

bit 2-0 **FEXTOSC[2:0]:** FEXTOSC External Oscillator Mode Selection bits

111 = EC (External Clock) above 8 MHz; PFM set to high power (device manufacturing default)

110 = EC (External Clock) for 500 kHz to 8 MHz; PFM set to medium power

101 = EC (External Clock) below 500 kHz; PFM set to low power

100 = Oscillator is not enabled

011 = Reserved (do not use)

010 = HS (crystal oscillator) above 8 MHz; PFM set to high power

001 = XT (crystal oscillator) above 500 kHz, below 8 MHz; PFM set to medium power

000 = LP (crystal oscillator) optimized for 32.768 kHz; PFM set to low power

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## REGISTER B-2: CONFIGURATION WORD 1H (30 0001h) – OSCILLATORS

| U-1   | U-1 | R/W-1 | U-1 | R/W-1 | U-1 | U-1 | R/W-1    |
|-------|-----|-------|-----|-------|-----|-----|----------|
| —     | —   | FCMEN | —   | CSWEN | —   | —   | CLKOUTEN |
| bit 7 |     |       |     |       |     |     | bit 0    |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '1'  
 -n = Value for blank device        '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7-6        **Unimplemented:** Read as '1'
- bit 5        **FCMEN:** Fail-Safe Clock Monitor Enable bit  
               1 = FSCM timer is enabled  
               0 = FSCM timer is disabled
- bit 4        **Unimplemented:** Read as '1'
- bit 3        **CSWEN:** Clock Switch Enable bit  
               1 = Writing to NOSC and NDIV is allowed  
               0 = The NOSC and NDIV bits cannot be changed by user software
- bit 2-1      **Unimplemented:** Read as '1'
- bit 0        **CLKOUTEN:** Clock Out Enable bit  
               If FEXTOSC[2:0] = EC (high, mid or low) or Not Enabled:  
               1 = CLKOUT function is disabled; I/O or oscillator function on OSC2  
               0 = CLKOUT function is enabled; Fosc/4 clock appears at OSC2  
               Otherwise:  
               This bit is ignored.

## REGISTER B-3: CONFIGURATION WORD 2L (30 0002h) – SUPERVISOR

| R/W-1  | R/W-1  | R/W-1                              | U-1 | U-1 | U-1 | R/W-1                            | R/W-1 |
|--------|--------|------------------------------------|-----|-----|-----|----------------------------------|-------|
| BOREN1 | BOREN0 | $\overline{\text{LPBOR}}\text{EN}$ | —   | —   | —   | $\overline{\text{PWRT}}\text{E}$ | MCLRE |
| bit 7  |        |                                    |     |     |     | bit 0                            |       |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '1'

-n = Value for blank device

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

**BOREN[1:0]:** Brown-out Reset Enable bits

When enabled, Brown-out Reset Voltage (VBOR) is set by the BORV[1:0] bits.

11 = Brown-out Reset is enabled, SBOREN bit is ignored

10 = Brown-out Reset is enabled while running, disabled in Sleep; SBOREN is ignored

01 = Brown-out Reset is enabled according to SBOREN

00 = Brown-out Reset is disabled

bit 5

**LPBOR**EN: Low-Power BOR Enable bit

1 = ULPBOR is disabled

0 = ULPBOR is enabled

bit 4-2

**Unimplemented:** Read as '1'

bit 1

**PWRT**E: Power-up Timer Enable bit

1 = PWRT is disabled

0 = PWRT is enabled

bit 0

**MCLR**E: Master Clear ( $\overline{\text{MCLR}}$ ) Enable bit

If LVP = 1:

RE3 pin function is  $\overline{\text{MCLR}}$ .

If LVP = 0:

1 =  $\overline{\text{MCLR}}$  pin is  $\overline{\text{MCLR}}$

0 =  $\overline{\text{MCLR}}$  pin function is a port-defined function

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## REGISTER B-4: CONFIGURATION WORD 2H (30 0003h) – SUPERVISOR

| R/W-1        | U-1 | R/W-1        | R/W-1  | R/W-1   | R/W-1  | R/W-1                | R/W-1                |
|--------------|-----|--------------|--------|---------|--------|----------------------|----------------------|
| <u>XINST</u> | —   | <u>DEBUG</u> | STVREN | PPS1WAY | ZCDDIS | BORV1 <sup>(1)</sup> | BORV0 <sup>(1)</sup> |
| bit 7        |     |              |        |         |        |                      | bit 0                |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '1'  
 -n = Value for blank device            '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7            **XINST**: Extended Instruction Set Enable bit  
                   1 = Extended instruction set and Indexed Addressing mode are disabled (Legacy mode)  
                   0 = Extended instruction set and Indexed Addressing mode are enabled
- bit 6            **Unimplemented**: Read as '1'
- bit 5            **DEBUG**: Debugger Enable bit  
                   1 = Background debugger is disabled  
                   0 = Background debugger is enabled
- bit 4            **STVREN**: Stack Overflow/Underflow Reset Enable bit  
                   1 = Stack overflow or underflow will cause a Reset  
                   0 = Stack overflow or underflow will not cause a Reset
- bit 3            **PPS1WAY**: PPSLOCK One-Way Set Enable bit  
                   1 = PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle  
                   0 = PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)
- bit 2            **ZCDDIS**: ZCD Disable bit  
                   1 = ZCD is disabled; ZCD can be enabled by setting the ZCDSEN bit of the ZCDCON register  
                   0 = ZCD is always enabled
- bit 1-0        **BORV[1:0]**: Brown-out Reset Voltage Selection bits  
                   11 = Brown-out Reset Voltage (VBOR) is set to 1.90V  
                   10 = Brown-out Reset Voltage (VBOR) is set to 2.45V  
                   01 = Brown-out Reset Voltage (VBOR) is set to 2.7V  
                   00 = Brown-out Reset Voltage (VBOR) is set to 2.85V

## REGISTER B-5: CONFIGURATION WORD 3L (30 0004h) – WINDOWED WATCHDOG TIMER

| U-1   | R/W-1 | R/W-1 | R/W-1   | R/W-1   | R/W-1   | R/W-1   | R/W-1   |
|-------|-------|-------|---------|---------|---------|---------|---------|
| —     | WDTE1 | WDTE0 | WDTCP54 | WDTCP53 | WDTCP52 | WDTCP51 | WDTCP50 |
| bit 7 |       |       |         |         |         |         | bit 0   |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '1'

-n = Value for blank device

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

**Unimplemented:** Read as '1'

bit 6-5

**WDTE[1:0]:** WDT Operating Mode bits

00 = WDT is disabled, SWDTEN is ignored

01 = WDT is enabled/disabled by the SWDTEN bit in WDTCON0

10 = WDT is enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN is ignored

11 = WDT is enabled regardless of Sleep; SWDTEN is ignored

bit 4-0

**WDTCP5[4:0]:** WDT Period Select bits

| WDTCP5[4:0] | WDTPS at POR |               |                 |                                             | Software Control of WDTPS? |
|-------------|--------------|---------------|-----------------|---------------------------------------------|----------------------------|
|             | Value        | Divider Ratio |                 | Typical Time-out (F <sub>IN</sub> = 31 kHz) |                            |
| 00000       | 00000        | 1:32          | 2 <sup>5</sup>  | 1 ms                                        | No                         |
| 00001       | 00001        | 1:64          | 2 <sup>6</sup>  | 2 ms                                        |                            |
| 00010       | 00010        | 1:128         | 2 <sup>7</sup>  | 4 ms                                        |                            |
| 00011       | 00011        | 1:256         | 2 <sup>8</sup>  | 8 ms                                        |                            |
| 00100       | 00100        | 1:512         | 2 <sup>9</sup>  | 16 ms                                       |                            |
| 00101       | 00101        | 1:1024        | 2 <sup>10</sup> | 32 ms                                       |                            |
| 00110       | 00110        | 1:2048        | 2 <sup>11</sup> | 64 ms                                       |                            |
| 00111       | 00111        | 1:4096        | 2 <sup>12</sup> | 128 ms                                      |                            |
| 01000       | 01000        | 1:8192        | 2 <sup>13</sup> | 256 ms                                      |                            |
| 01001       | 01001        | 1:16384       | 2 <sup>14</sup> | 512 ms                                      |                            |
| 01010       | 01010        | 1:32768       | 2 <sup>15</sup> | 1s                                          |                            |
| 01011       | 01011        | 1:65536       | 2 <sup>16</sup> | 2s                                          |                            |
| 01100       | 01100        | 1:131072      | 2 <sup>17</sup> | 4s                                          |                            |
| 01101       | 01101        | 1:262144      | 2 <sup>18</sup> | 8s                                          |                            |
| 01110       | 01110        | 1:524299      | 2 <sup>19</sup> | 16s                                         |                            |
| 01111       | 01111        | 1:1048576     | 2 <sup>20</sup> | 32s                                         |                            |
| 10000       | 10000        | 1:2097152     | 2 <sup>21</sup> | 64s                                         |                            |
| 10001       | 10001        | 1:4194304     | 2 <sup>22</sup> | 128s                                        |                            |
| 10010       | 10010        | 1:8388608     | 2 <sup>23</sup> | 256s                                        |                            |
| 10011       | 10011        | 1:32          | 2 <sup>5</sup>  | 1 ms                                        | No                         |
| ...         | ...          |               |                 |                                             |                            |
| 11110       | 11110        | 1:65536       | 2 <sup>16</sup> | 2s                                          | Yes                        |
| 11111       | 01011        |               |                 |                                             |                            |

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## REGISTER B-6: CONFIGURATION WORD 3H (30 0005h) – WINDOWED WATCHDOG TIMER

|       |     |         |         |         |         |         |         |       |
|-------|-----|---------|---------|---------|---------|---------|---------|-------|
| U-1   | U-1 | R/W-1   | R/W-1   | R/W-1   | R/W-1   | R/W-1   | R/W-1   |       |
| —     | —   | WDTCCS2 | WDTCCS1 | WDTCCS0 | WDTCWS2 | WDTCWS1 | WDTCWS0 |       |
| bit 7 |     |         |         |         |         |         |         | bit 0 |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '1'  
 -n = Value for blank device           '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-6                      **Unimplemented:** Read as '1'

bit 5-3                      **WDTCCS[2:0]:** WDT Input Clock Selector bits

If WDTE[1:0] Fuses = 2'b00:

This bit is ignored.

Otherwise:

000 = WDT reference clock is the 31.0 kHz LFINTOSC (default value)

001 = WDT reference clock is the 31.25 kHz HFINTOSC (MFINTOSC)

010 = Reserved (default to LFINTOSC)

•

•

•

110 = Reserved (default to LFINTOSC)

111 = Software control

bit 2-0                      **WDTCWS[2:0]:** WDT Window Select bits

| WDTCWS[2:0] | Window at POR |                              |                                | Software Control of Window | Keyed Access Required? |
|-------------|---------------|------------------------------|--------------------------------|----------------------------|------------------------|
|             | Value         | Window Delay Percent of Time | Window Opening Percent of Time |                            |                        |
| 000         | 000           | 87.5                         | 12.5                           | No                         | Yes                    |
| 001         | 001           | 75                           | 25                             |                            |                        |
| 010         | 010           | 62.5                         | 37.5                           |                            |                        |
| 011         | 011           | 50                           | 50                             |                            |                        |
| 100         | 100           | 37.5                         | 62.5                           |                            |                        |
| 101         | 101           | 25                           | 75                             |                            |                        |
| 110         | 111           | n/a                          | 100                            |                            |                        |
| 111         | 111           | n/a                          | 100                            | Yes                        | No                     |

## REGISTER B-7: CONFIGURATION WORD 4L (30 0006h) – MEMORY WRITE PROTECTION

| R/W-1               | R/W-1               | R/W-1               | R/W-1               | R/W-1               | R/W-1               | R/W-1               | R/W-1               |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| WRT7 <sup>(1)</sup> | WRT6 <sup>(1)</sup> | WRT5 <sup>(1)</sup> | WRT4 <sup>(1)</sup> | WRT3 <sup>(1)</sup> | WRT2 <sup>(1)</sup> | WRT1 <sup>(1)</sup> | WRT0 <sup>(1)</sup> |
| bit 7               |                     |                     |                     |                     |                     |                     | bit 0               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '1'

-n = Value for blank device

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **WRTn:** User NVM Self-Write Protection bits<sup>(1)</sup>

0 = Memory Block *n* is write-protected

1 = Memory Block *n* is NOT write-protected

**Note 1:** Refer to [Table 2-1](#) for details on implementation of the individual WRTx bits.

## REGISTER B-8: CONFIGURATION WORD 4H (30 0007h) – MEMORY WRITE PROTECTION

| U-1   | U-1 | R/W-1 | R/W-1 | U-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-----|-------|-------|-----|-------|-------|-------|
| —     | —   | LVP   | SCANE | —   | WRTD  | WRTB  | WRTC  |
| bit 7 |     |       |       |     |       |       | bit 0 |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '1'

-n = Value for blank device

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '1'

bit 5 **LVP:** Low-Voltage Programming Enable bit

0 = High voltage on MCLR/VPP pin must be used for programming

1 = Low-Voltage Programming is enabled; MCLR/VPP pin function is MCLR, MCLRE Configuration bit is ignored

The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode or accidentally eliminating LVP mode from the configuration state.

bit 4 **SCANE:** Scanner Enable bit

1 = Scanner module is available for use, SCANMD bit enables the module

0 = Scanner module is NOT available for use, SCANMD bit is ignored

bit 3 **Unimplemented:** Read as '1'

bit 2 **WRTD:** Data EEPROM Write Protection bit

0 = Data EEPROM is write-protected

1 = Data EEPROM is NOT write-protected

bit 1 **WRTB:** Boot Block Write Protection bit

0 = Boot block is write-protected

1 = Boot block is NOT write-protected

bit 0 **WRTC:** Configuration Register Write Protection bit

0 = Configuration register is write-protected

1 = Configuration register is NOT write-protected

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## REGISTER B-9: CONFIGURATION WORD 5L (30 0008h) – CODE PROTECTION

|       |     |     |     |     |     |       |       |
|-------|-----|-----|-----|-----|-----|-------|-------|
| U-1   | U-1 | U-1 | U-1 | U-1 | U-1 | R/W-1 | R/W-1 |
| —     | —   | —   | —   | —   | —   | CPD   | CP    |
| bit 7 |     |     |     |     |     | bit 0 |       |

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '1'  
 -n = Value for blank device      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 7-2      **Unimplemented:** Read as '1'  
 bit 1      **CPD:** Data NVM Memory Code Protection bit  
             1 = Data NVM code protection is disabled  
             0 = Data NVM code protection is enabled  
 bit 0      **CP:** User NVM Program Memory Code Protection bit  
             1 = User NVM code protection is disabled  
             0 = User NVM code protection is enabled

## REGISTER B-10: CONFIGURATION WORD 6L (30 000Ah) – MEMORY READ PROTECTION

|                      |                      |                      |                      |                      |                      |                      |                      |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| R/W-1                | R/W-1                | R/W-1                | R/W-1                | R/W-1                | R/W-1                | R/W-1                | R/W-1                |
| EBTR7 <sup>(1)</sup> | EBTR6 <sup>(1)</sup> | EBTR5 <sup>(1)</sup> | EBTR4 <sup>(1)</sup> | EBTR3 <sup>(1)</sup> | EBTR2 <sup>(1)</sup> | EBTR1 <sup>(1)</sup> | EBTR0 <sup>(1)</sup> |
| bit 7                |                      |                      |                      |                      |                      |                      | bit 0                |

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '1'  
 -n = Value for blank device      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 7-0      **EBTRn:** Table Read Protection bits<sup>(1)</sup>  
             0 = Memory Block *n* is protected from Table Reads executed in other blocks  
             1 = Memory Block *n* is NOT protected from Table Reads executed in other blocks

**Note 1:** Refer to [Table 2-1](#) for details on implementation of the individual EBTRx bits.

## REGISTER B-11: CONFIGURATION WORD 6H (30 000Bh) – MEMORY READ PROTECTION

|       |     |     |     |     |     |       |     |
|-------|-----|-----|-----|-----|-----|-------|-----|
| U-1   | U-1 | U-1 | U-1 | U-1 | U-1 | R/W-1 | U-1 |
| —     | —   | —   | —   | —   | —   | EBTRB | —   |
| bit 7 |     |     |     |     |     | bit 0 |     |

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '1'  
 -n = Value for blank device      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 7-2      **Unimplemented:** Read as '1'  
 bit 1      **EBTRB:** Table Read Protection bit  
             0 = Memory boot block is protected from Table Reads executed in other blocks  
             1 = Memory boot block is NOT protected from Table Reads executed in other blocks  
 bit 0      **Unimplemented:** Read as '1'



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