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Platinum-rated AC/DC Reference Design Using the dsPIC® DSC

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ENERGY STAR® AND THE CLIMATE SAVERS COMPUTING INITIATIVE (CSCI)

Today, “Green Power” is one of the hottest topics in the development of power supplies. To meet the latest “green” standards in all fields of industry, including automotive and consumer applications, it is necessary to design for increased efficiency and reliability.

One of the key players in the green movement is the ENERGY STAR Program (www.energystar.gov). ENERGY STAR is an international standard for energy-efficient consumer products. The organization was started in the United States, but has been adopted by many countries worldwide. To earn the right to display a ENERGY STAR logo, devices must meet strict energy-usage specifications.

Another key player is the Climate Savers Computing Initiative (CSCI), www.climatesaverscomputing.org, a non-profit organization that was spearheaded by Google Inc. and Intel. CSCI is a partner to ENERGY STAR, using their specifications for desktops, laptops, and workstation computers in an effort to encourage manufacturers to improve the efficiency of a computer’s power delivery, while reducing the energy consumed when the computer is in a Stand-by or Idle state. CSCI rates products as base, bronze, silver, gold; and now, the latest specification, platinum.

This application note presents a fully digital-controlled 720W AC-to-DC (AC/DC) power supply, which meets all CSCI Platinum Specifications, as well as providing a variety of additional, application-specific features and functions.

The CSCI Platinum-level efficiency specification shown in Figure 1 applies to single-phase AC input power-supply units with a power range from 500W to 1kW, measured at 230 VAC input voltage. Along with efficiency, the CSCI Platinum Specification also defines Power Factor as a function of load, as shown in Figure 2.

FIGURE 1: CSCI EFFICIENCY LEVELS

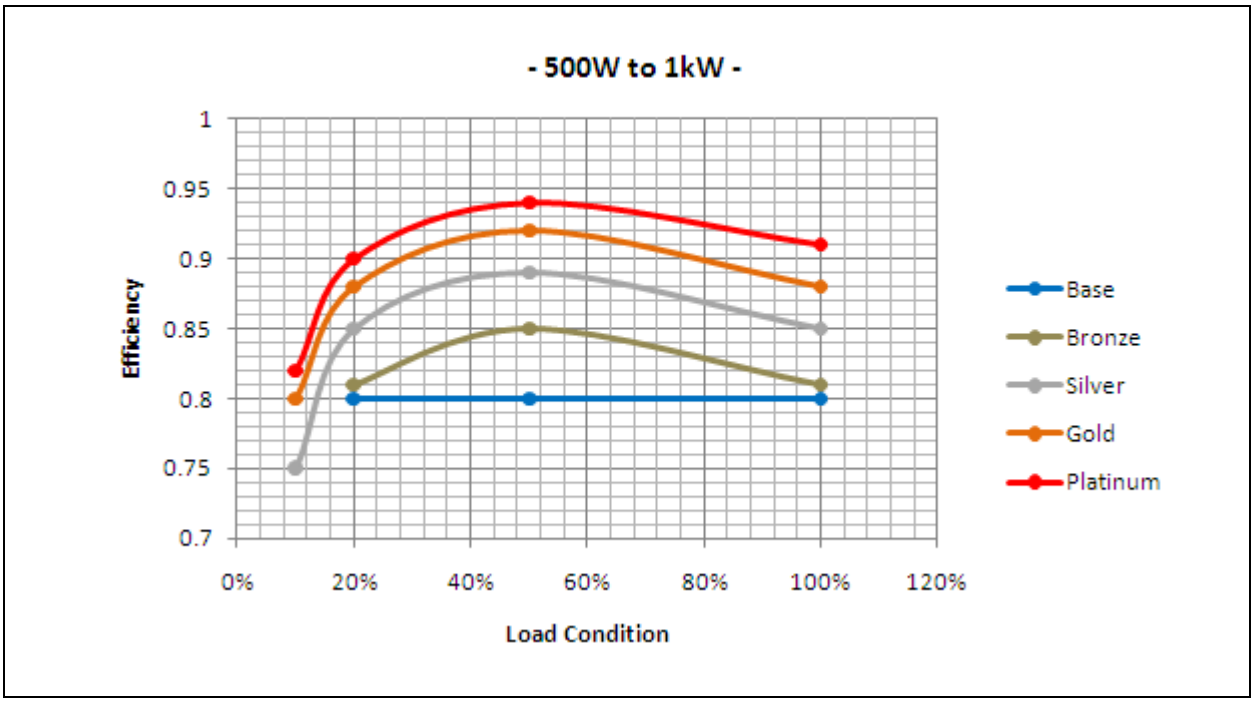
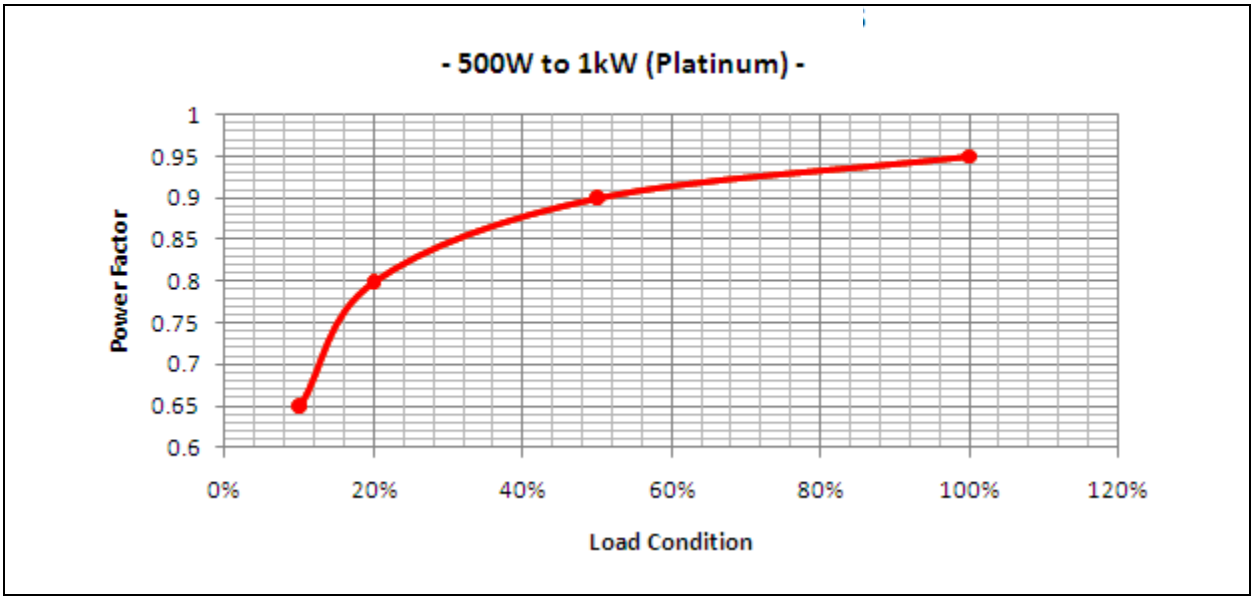


FIGURE 2: CSCI POWER FACTOR LEVELS



PLATINUM-RATED AC/DC REFERENCE DESIGN FEATURES

Microchip's Platinum-rated AC/DC Reference Design works with universal input voltage and produces a regulated output voltage of 12 VDC. The continuous output power rating of the reference design is 720W.

This reference design supports the following features:

- Standardized form factor: 1U
- Wide-range AC input (90-264 VAC @ 50/60 Hz)
- 20 ms minimum hold-up time to compensate drop-outs during UPS step-in
- Parallel operation, including load/current sharing capabilities
- Hot-plug capability for easy maintenance during operation
- MTBF > 50,000h @ 40°C
- EMI/EMC, which satisfies EN55022, Class B
- Under voltage lock-out
- Over-voltage protection
- Sustained short-circuit protection
- Overtemperature shutdown
- Fan failure monitoring and detection
- Monitoring and control interface
- I^2C™-based communication for enhanced power management

Hardware Overview

Interleaving topologies offer significant advantages when high efficiency, reliability, and power density are required. Splitting each topology in two parallel phases and interleaving their operation by a 180° phase shift significantly reduces the current ripple. The decreased current peak-to-peak values in interleaved topologies result in lower operating temperatures, which also equates to reduced losses. Since each phase needs to carry only half of the total current, the conduction losses in capacitors, the copper of the printed circuit board (PCB), and the magnetics, are reduced by a factor of four; as the current appears as a squared value in the losses computation equations.

In addition to reduced losses, another advantage of interleaved topologies is the halved current rating for each phase, which results in a smaller overall size for the chokes and/or transformers, and reduced size of the PCB traces, MOSFETs, heat sinks and diodes.

In this reference design, both the Power Factor Correction (PFC) boost stage and the two-switch forward converter have been designed in a two-phase interleaved architecture. Figure 3 shows a high-level block diagram of the reference design. This section will discuss the following power stages in more detail:

- Input stage
- 2-Phase Interleaved Power Factor Correction (IPFC) boost converter
- 2-Phase interleaved two-switch forward DC-to-DC (DC/DC) converter
- Synchronous rectifier
- Output stage

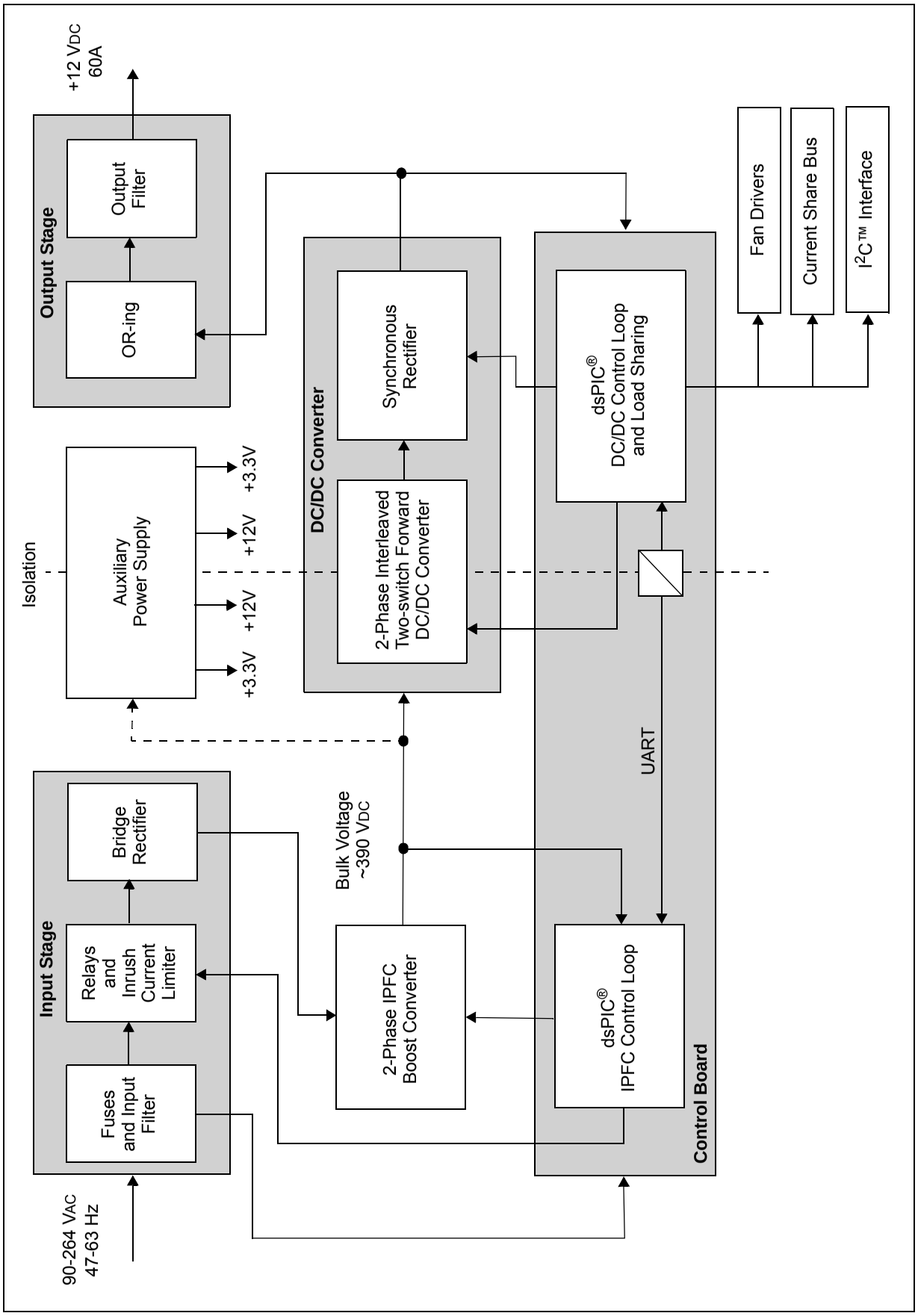


FIGURE 3: HIGH-LEVEL BLOCK DIAGRAM

INPUT STAGE

The very first components, placed at the mains terminals, are a filter choke and a 1 µF capacitor across the terminals for Electromagnetic Interference (EMI) suppression. The EMI filter choke is followed by two fuses, one in the line and one additional in the neutral. The sockets have been chosen to carry fuses that meet Underwriters Laboratories Inc. (UL) and International Electrotechnical Commission (IEC) standards. A 470V varistor across the mains terminals adds additional protection against transient voltage spikes.

The input filter stage uses two further filters consisting of a common mode choke, two Y-capacitors connected to earth ground, and a metalized polypropylene film interference suppression capacitor (X-capacitor) connected across the line and neutral.

After the input filter, a Negative Temperature Coefficient (NTC), with a zero power resistance of 10Ω at 25°C, is used to limit the inrush current below 40A (20A typical). This NTC will be bypassed by a relay as soon as the bulk voltage has stabilized and the controller starts to ramp-up the system.

The input voltage is connected to a bridge rectifier with a voltage rating of 1,300V and a current rating of 43A. Across the output of this bridge rectifier, another varistor and an interference suppression capacitor have been placed for transient protection.

2-PHASE IPFC BOOST CONVERTER

The IPFC converter uses two identical boost converters, that are parallel coupled and are operated 180° out-of-phase with respect to each other. Figure 4 shows a high-level block diagram of the IPFC stage indicating the different currents, voltages, and Pulse-Width Modulation (PWM) control signals.

The IPFC stage is an AC/DC converter, which converts the AC input supply voltage to a regulated high-voltage DC output. Along with boosting the rectified AC voltage to a regulated DC output voltage, the PFC stage also shapes the inductor current similar to that of the rectified AC voltage to maintain a high power factor and low total harmonic distortion. The PFC stage is designed to operate in Continuous Conduction Mode (CCM) to reduce harmonic content in the input current. Figure 5 shows the operational waveforms of the IPFC converter when operating in CCM.

FIGURE 4: INTERLEAVED POWER FACTOR CORRECTION BOOST STAGE

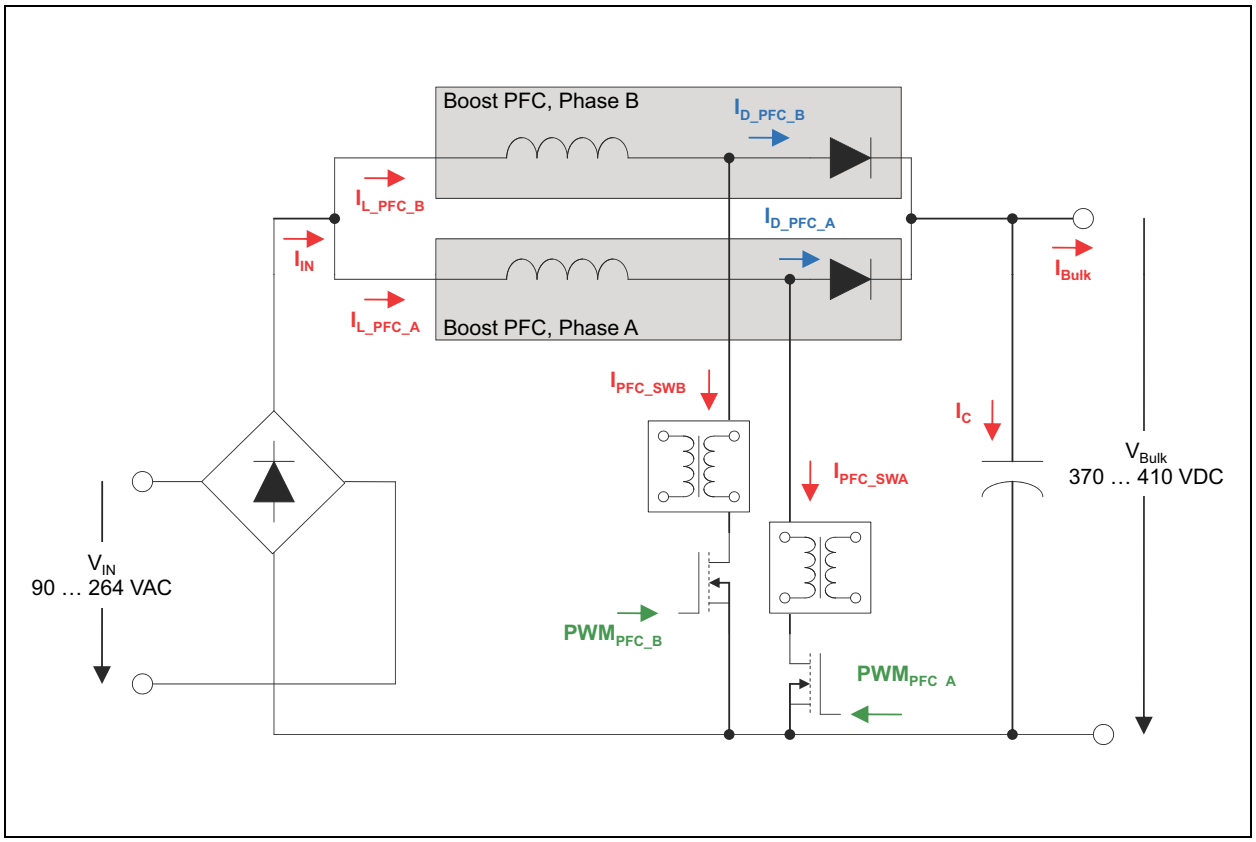
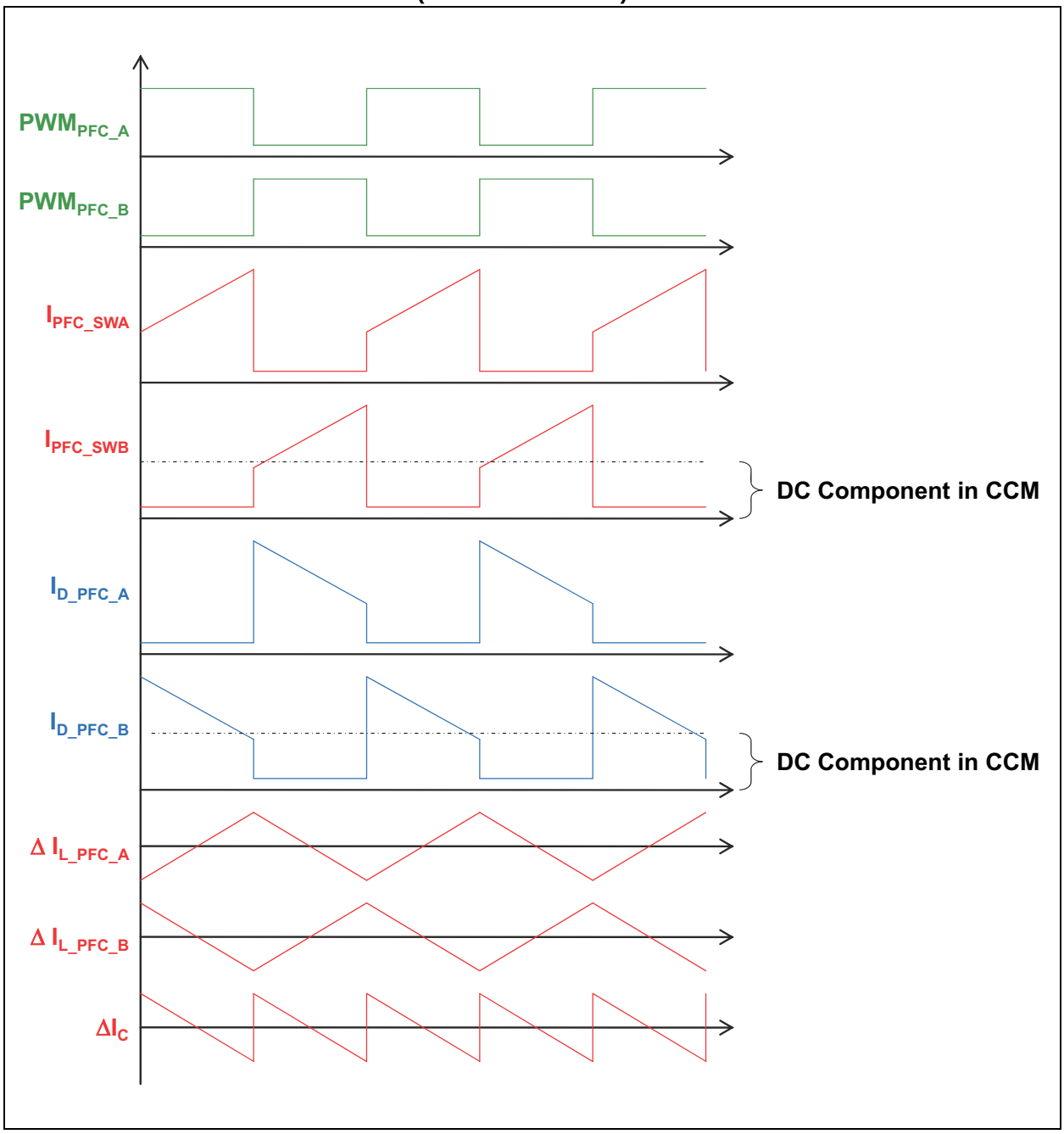


FIGURE 5: IDEAL WAVEFORMS OF THE INTERLEAVED POWER FACTOR CORRECTION BOOST CONVERTER (50% DUTY CYCLE)



The boost PFC topology requires only a single low-side MOSFET to be driven. The Microchip MCP14E4 two-channel MOSFET driver, with CMOS push-pull outputs capable of sourcing and sinking 3.5A @ 12V, has been selected to drive both phases.

Two current sense transformers (CT) with a turns ratio of 50:1 were used for current sensing. The current transformers are placed on the drain side of the low-side MOSFETs instead of the source side to gain better feedback with reduced switching noise.

The current output is converted into a voltage signal by a 15Ω burden resistor. A four resistor series-parallel network (with two 15Ω resistors in series and two 15Ω resistors in parallel) was used for this CT burden to minimize the relative tolerances of the shunt to gain higher accuracy. The series connection is also used to divide the voltage by two for the comparator inputs of the dsPIC® Digital Signal Controller (DSC).

The selection of the PFC MOSFET depends on the specified output voltage of the IPFC stage, as well as the maximum current (inductor current) that will pass through the MOSFET. The drain-to-source rating of the MOSFET should be greater than the output voltage with some 20-30% headroom, while the inductor current should be lower than the drain current (I_D) of the MOSFET. The MOSFET selection will also depend on the thermal characteristics of the package and the internal ON-state resistance (R_{DSON}). The lower the ON-state resistance, the less conduction losses observed. For this design, the MOSFET selected is the 600V CoolMOS™ C6 Power Transistor (IPW60R160C6) from Infineon Technologies.

The selected IPFC diode is the Z-Rec™ Rectifier (C3D20060D), which is a silicon carbide Schottky diode from CREE, Inc. This diode was selected for its reverse voltage rating, forward current rating, low forward voltage drop, and extremely fast switching capabilities. The reverse recovery losses typically form a significant percentage of the boost converter power losses. These losses are minimized by using silicon carbide diodes, because there is almost no reverse recovery time associated with them.

INTERLEAVED TWO-SWITCH FORWARD CONVERTER WITH SYNCHRONOUS RECTIFICATION

Figure 6 shows the basic topology with its current paths and voltages in the interleaved two-switch forward converter design. In contrast to a flyback converter topology, forward converters use voltage transformers to pass energy to the output during the ON-time of the MOSFETs.

2-Phase Interleaved Two-Switch Forward Converter

In a two-switch forward converter, a high-side and low-side MOSFET are used to apply voltage across the primary winding. Both MOSFETs are switched ON and OFF simultaneously. As soon as voltage is applied across the primary winding, all windings go positive. When MOSFET Q3 is switched ON, the current in the secondary winding will build up.

As current may still be flowing through L1 and C1, the load and the return path through D3, the current will build up until its value reaches and exceeds the current through D3. At this moment, the forward current through D3 will stop and the voltage V_S across the secondary winding will be applied to the start of L1. Once this occurs, the choke L1 and the output capacitor C1 will be charged and power is delivered to the output.

When the MOSFETs Q1 and Q2 are switched OFF, the voltages on all windings will reverse. The flyback effect during this process would result in high voltage levels across the primary winding of the transformer. These peaks are clamped by the parallel diodes, D1 and D2. These diodes will feed the energy stored in the magnetic field back into the supply lines. As the charging and discharging process will take the same amount of time (approximately), the duty ratio must not exceed 50%, as this would result in a staircase saturation of the transformer core.

When the voltage on the secondary side reverses, MOSFET Q3 is switched OFF and the choke L1 will continue driving the current into C1 and the load causing D3 to become forward-biased.

In an interleaved architecture, phase A and phase B are commutated with a 180° phase shift. As the maximum duty ratio is limited to 50%, the total time in which the output current is driven through L1, C1, and D3, becomes very small. Figure 7 and Figure 8 show the operational waveforms during Discontinuous Conduction Mode (DCM) and CCM, respectively.

FIGURE 6: INTERLEAVED TWO-SWITCH FORWARD CONVERTER

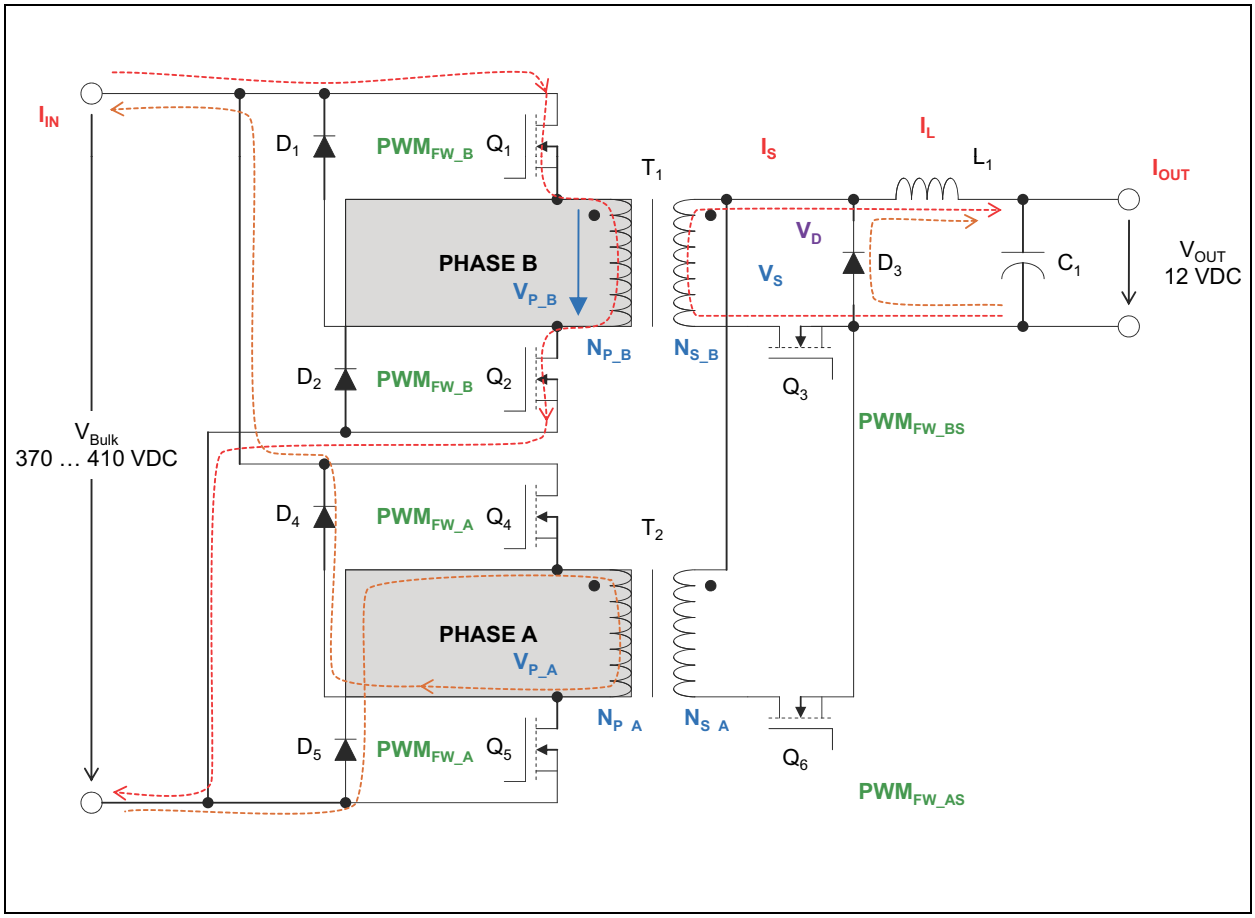


FIGURE 7: TYPICAL WAVEFORMS OF THE INTERLEAVED TWO-SWITCH FORWARD CONVERTER IN DCM

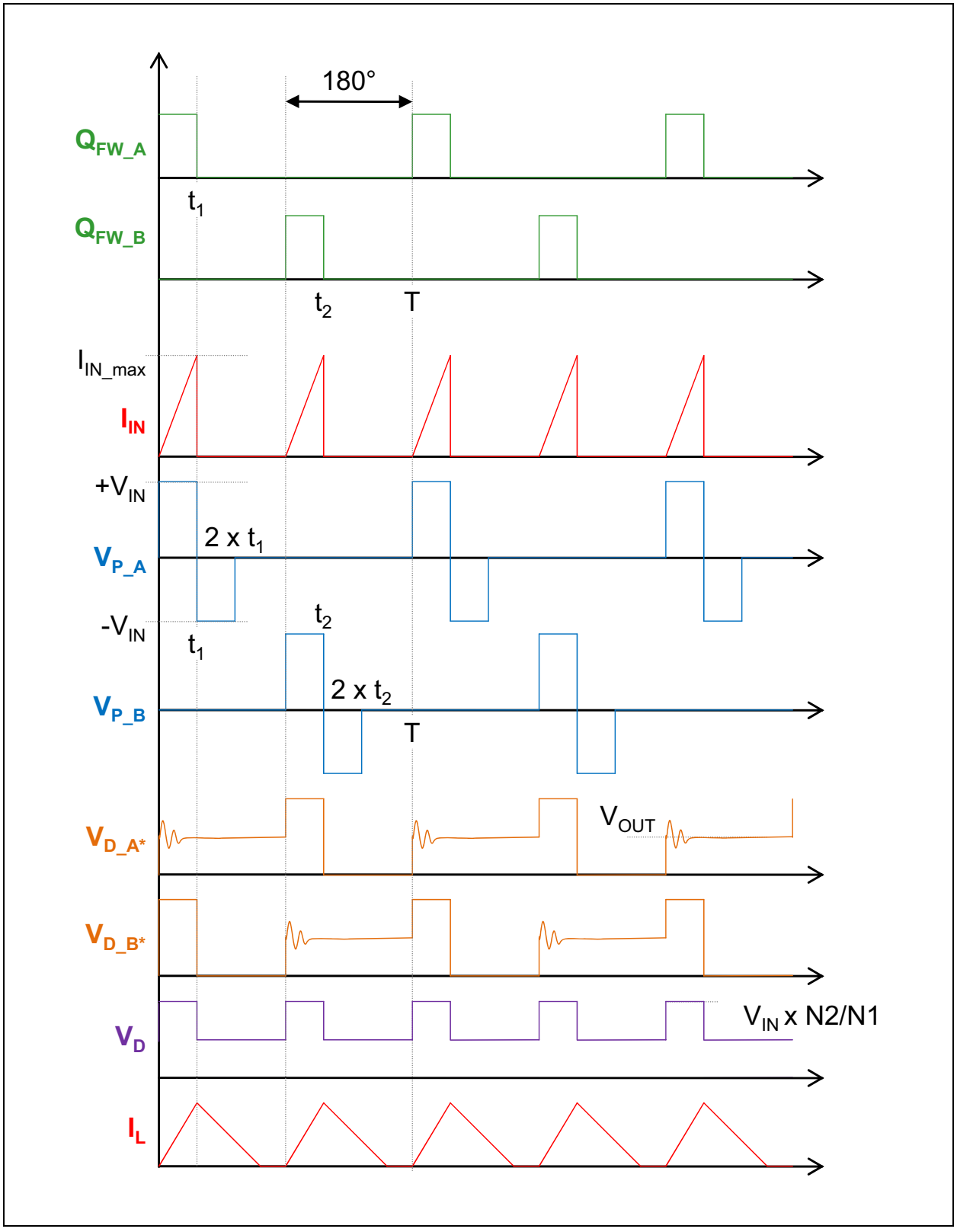
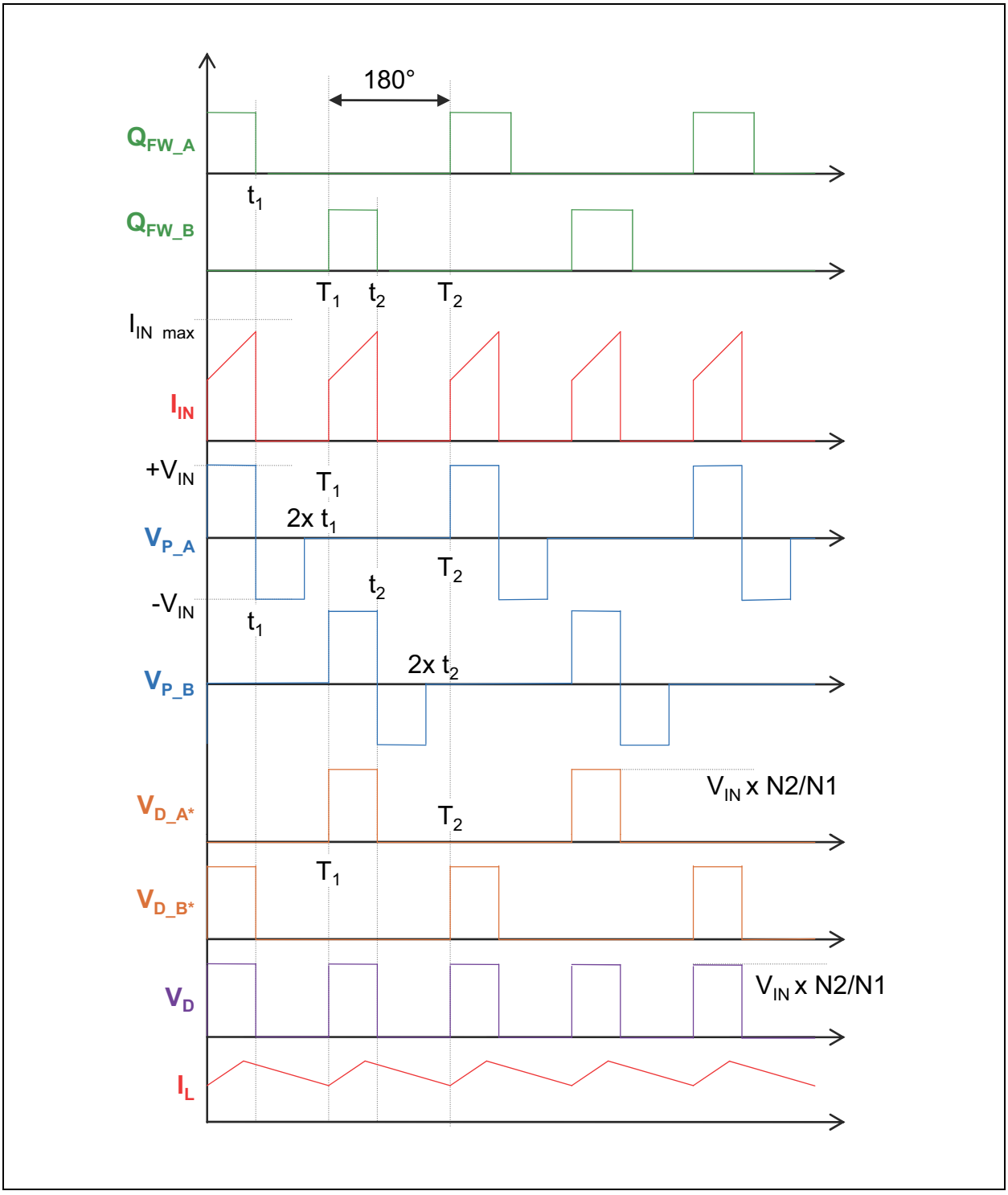


FIGURE 8: TYPICAL WAVEFORMS OF THE INTERLEAVED TWO-SWITCH FORWARD CONVERTER IN CCM



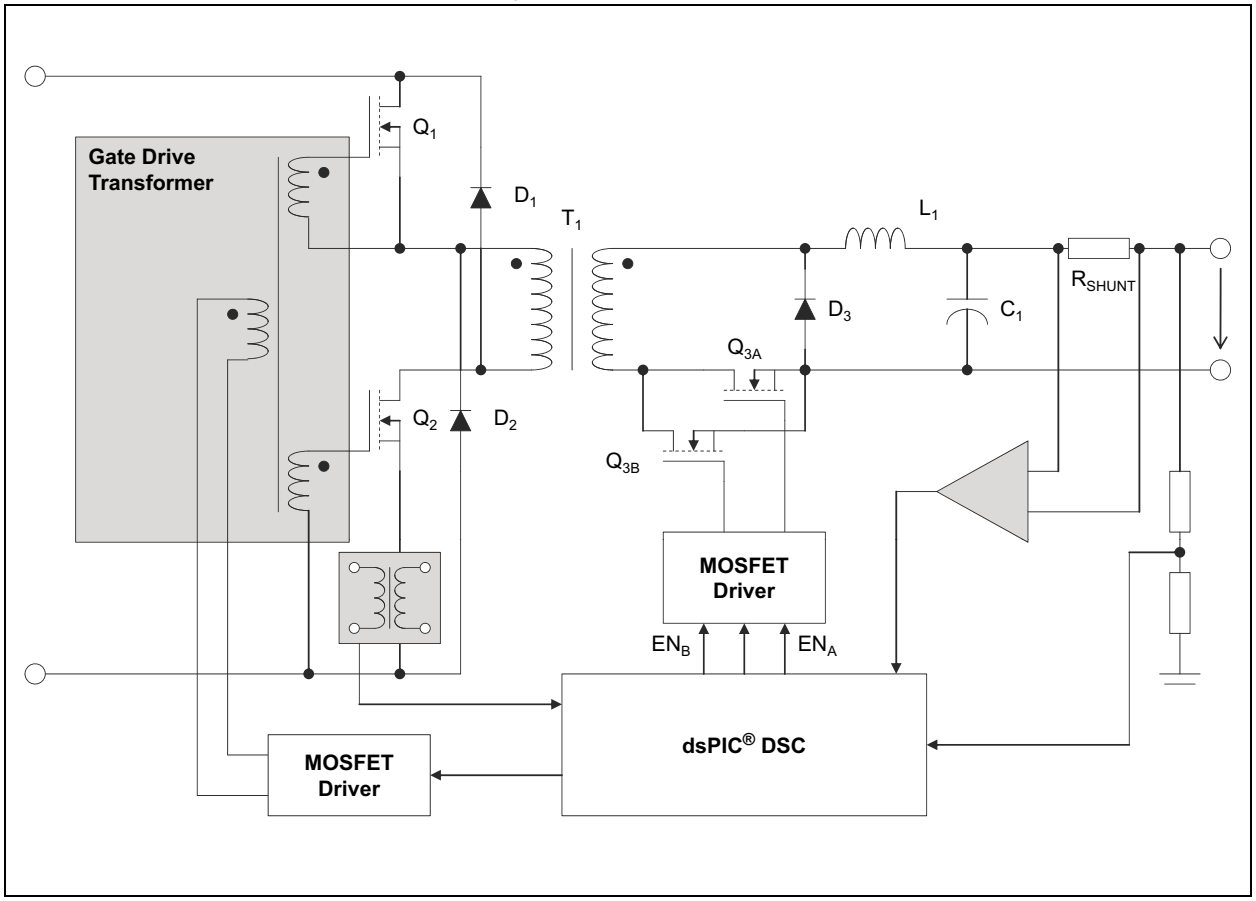
As mentioned previously, both MOSFETs of the two-switch forward converter are turned ON and OFF simultaneously, and both MOSFETs can be driven by the same signal using one gate drive transformer with a single primary and two secondary windings. Although a gate driver circuit could also be designed using a direct drive for the low-side and an additional gate drive transformer for the high-side, this might result in timing variations between both switches, resulting in decreased efficiency and higher component stress. Therefore, it is easier to use one gate drive transformer with an equal number of turns for the secondary windings, as shown in Figure 9.

For this reference design, the selected MOSFETs for the two-switch forward converter are 600V CoolMOS C6 Power Transistors (IPW60R280C6) from Infineon Technologies. The criteria for selecting these MOSFETs is similar to that of the PFC MOSFETs (i.e., low switching and conduction losses, high drain-to-source voltage rating and high continuous drain current). The selected clamping diode(s) for the two-switch forward converter is the STTH310 High Voltage Ultrafast Rectifier Diode from STMicroelectronics, with a breakdown voltage of 1000 VDC, a forward current of 3A, and a forward voltage of less than 1.7V.

As shown in Figure 9, the current in the primary winding is sensed with a CT. The CT is placed between the low-side switch and the ground of each converter phase. As transformers are used to drive the gates on the primary side as well, the control and feedback interface of the two-switch forward converter is completely isolated. The controller is placed on the secondary side. This simplifies the output feedback paths and the interface to the MOSFET drivers of the synchronous rectifiers. Similar to the PFC burden resistor network, the DC/DC burden resistor is comprised of four resistors; two series-connected 27Ω resistors connected in parallel with two series-connected 150Ω resistors. The series connection is also used to divide the voltage down for the comparator inputs of the dsPIC DSC.

To achieve high bandwidth feedback to provide maximum performance, a high-side shunt resistor was used for the output current feedback. This resistor is placed between the output capacitors and the output filter to detect load steps as soon as possible. To minimize the losses caused by the resistance of this shunt resistor, two 500 µΩ resistors were used in parallel. A high-side current monitor using the Microchip MCP6H02 op-amp was used to provide the feedback.

FIGURE 9: GATE DRIVER CIRCUIT, CURRENT AND VOLTAGE FEEDBACK



Synchronous Rectifier

Normally, forward converters are designed with one rectifying diode and one free-wheeling diode. However, in this reference design, the rectifier diode has been replaced by a MOSFET to increase efficiency and to compensate for signal delays that are caused by the leakage inductance of the secondary transformer winding. This effect becomes more and more significant the lower the output voltage and the higher the output current rating. In this design with a 12V output voltage providing up to 60A output current, this effect is significant.

A fully synchronous rectifier would also replace the freewheel diode D3, shown in Figure 9, by a MOSFET. However, the major aspect is to compensate for propagation delays from the primary to the secondary side. Replacing diode D3 will have very little effect, but would bring more complexity into the design, and the required energy to drive the gate of the additional switch would exceed the savings. Therefore, a parallel rectifier was used to minimize the losses.

Due to the high currents, the MOSFET Q3 has been split into two parallel MOSFETs, Q3A and Q3B, to minimize the losses caused by the on-resistance at high loads. Below 50% load, the amount of energy required to drive the gates exceeds the savings by the parallel operation. In this state, only one switch is used by disabling one of the driver channels. This feature was implemented using the Microchip MCP14E4 MOSFET driver, which offers two independent, parallel driver outputs, each with a separated enable input. To increase efficiency at very light loads, the MOSFETs are completely disabled utilizing the body diodes of the MOSFETs.

For this design, the selected synchronous MOSFETs are the HEXFET® Power MOSFET (IRFP4368PbF) from International Rectifier. These MOSFETs were selected for their extremely low ON-state resistance (typically 1.4 mΩ) and their continuous current capabilities.

Load Balancing in Parallel Operation of Multiple Power Supply Units

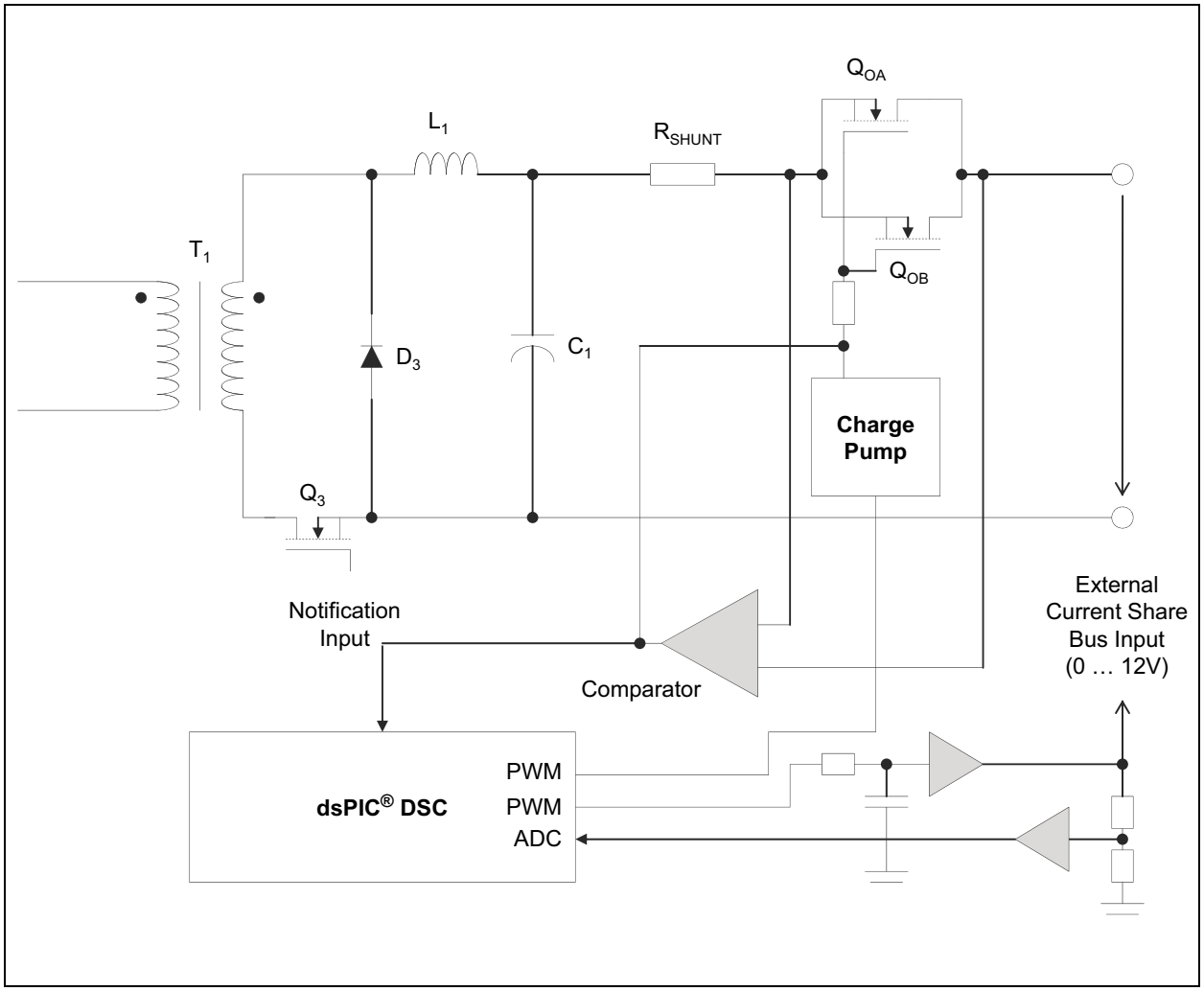
This power supply supports parallel operation with multiple power supply units (PSUs). When more than one power supply is used, the output voltage of each unit is never exactly the same. The result would be that the power supply providing the highest output voltage would provide more current until it reaches its current limit, while all other power supplies would decrease their output power accordingly. To establish equalized output power of each PSU, a low bandwidth current share bus interconnects each unit. An output protection circuit is required to prevent current from being fed into the output. Figure 10 shows a block diagram of the reverse current protection and the current share bus implementation.

The current share bus is a single wire bus providing a 0 to +12V voltage signal, which is directly proportional to the maximum single output power of one of the paralleled devices. Each PSU has to provide a voltage signal, which represents the average output power as a percentage of its maximum output power rating. The resulting voltage, which can be measured on the bus, represents the highest output power ratio of any of the paralleled units. When the controller detects a voltage on the current share bus, that exceeds that produced by the controller itself, the controller increases its own power supply output voltage. It is expected that this must result in an increase of the output current as well, which should result in a decrease of the visible maximum output current of the “leading” unit. Conversely, when a lower or equal voltage is detected on the bus, the output voltage, and so the output current, is decreased until the measured bus voltage exceeds the controller’s own generated voltage, assuming that the other paralleled PSUs have increased their output voltages and one of them takes the next lead. This technique allows the paralleling of power supplies with different power rating, e.g., running two power supplies, one with 300W and the other with 700W in parallel.

As this technique has a high risk for oscillations, some precautions have to be taken. First, the range in which the output voltage can be adjusted is very small (±1% typical). This is implemented by clamping the adjustment range to certain, programmable minimum and maximum values. Second, the bandwidth has to be very small. The control frequency is typically between 2 Hz and 5 Hz.

When multiple PSUs are operated in parallel, the case might appear that current could be fed into the output. In case of an internal short circuit, the bus voltage would be pulled to ground, causing a total system breakdown. To support redundant parallel operation of multiple units, a so-called OR-ing protection circuit has been implemented. This circuit consists of a switch in the high-line and a comparator, which shuts down the gate voltage as soon as the voltage level at the source output exceeds the voltage at the drain input. In this reference design, the OR-ing MOSFET has been split into two parallel FETs to minimize the on-resistance losses. As there is no requirement for fast switching, a discrete low-power charge pump circuit is used to generate the gate voltage. The comparator across this switch simply shortcuts the gate voltage to ground when the voltage at the source output exceeds the voltage at the drain input. The comparator output is monitored by the controller to detect the shutdown event.

FIGURE 10: BLOCK DIAGRAM OF THE CURRENT SHARE BUS IMPLEMENTATION



SOFTWARE OVERVIEW

The reference design is controlled using two Microchip dsPIC DSCs, as shown in Figure 3 in the **"Hardware Overview"** section.

The dsPIC33FJ16GS502 device on the primary side controls the IPFC boost converters, while the dsPIC33FJ16GS504 device on the secondary side controls the interleaved two-switch forward converter.

dsPIC® DSC System Resources

Table 1 and Table 2 highlight key resources that are essential for the IPFC and DC/DC stages. These tables highlight the required number of ADC channels, Comparators, and PWMs that are used to implement both topologies.

TABLE 1: PRIMARY SIDE dsPIC® DSC RESOURCES (dsPIC33FJ16GS502)

Description	Type of Signal	dsPIC® DSC Resource
PFC Phase 1 Current	Analog Input	AN0
PFC Phase 2 Current	Analog Input	AN2
Input Voltage (VAC)	Analog Input	AN4
Bulk Voltage	Analog Input	AN5
Primary Ambient Temperature	Analog Input	AN6
PFC Phase 1 Current	Comparator Input	CMP1B
PFC Phase 2 Current	Comparator Input	CMP2B
Bulk Voltage	Comparator Input	CMP3D
Boost1 MOSFET Gate Drive	Drive Output	PWM1H
Boost2 MOSFET Gate Drive	Drive Output	PWM2H
Inrush Relay	Drive Output	I/O
Primary-to-Secondary Communication	Communication	UART (TX/RX)

TABLE 2: SECONDARY SIDE dsPIC® DSC RESOURCES (dsPIC33FJ16GS504)

Description	Type of Signal	dsPIC® DSC Resource
Two-Switch Forward Phase1 Current	Analog Input	AN0
Two-Switch Forward Phase1 Current	Analog Input	AN2
High-Side Shunt Current	Analog Input	AN4
Output Voltage	Analog Input	AN5
Secondary Semiconductor Temperature	Analog Input	AN8
Secondary Ambient Temperature	Analog Input	AN10
Two-Switch Forward Phase 1 Current	Comparator Input	CMP1B
Two-Switch Forward Phase 2 Current	Comparator Input	CMP2B
Two-Switch Forward Phase 1 and Synch FETs	Drive Output	PWM1H/PWM1L
Two-Switch Forward Phase 2 and Synch FETs	Drive Output	PWM2H/PWM2L
Fan Drive	Drive Output	PWM3H
OR-ing Drive	Drive Output	PWM4L
Synch FETs Enable/Disable	Drive Output	I/O (2)
Primary-to-Secondary Communication	Communication	UART (TX/RX)
Secondary-to-PC Communication	Communication	I^2C™

Primary Side

HIGH-LEVEL SOFTWARE OVERVIEW

The primary side software is divided into the following categories.

- **Low Priority:** Initialization Routines, Main Loop and Serial I/O Routines
- **Medium Priority:** Voltage Control Loop and Advanced Algorithms
- **High Priority:** Current Control Loops

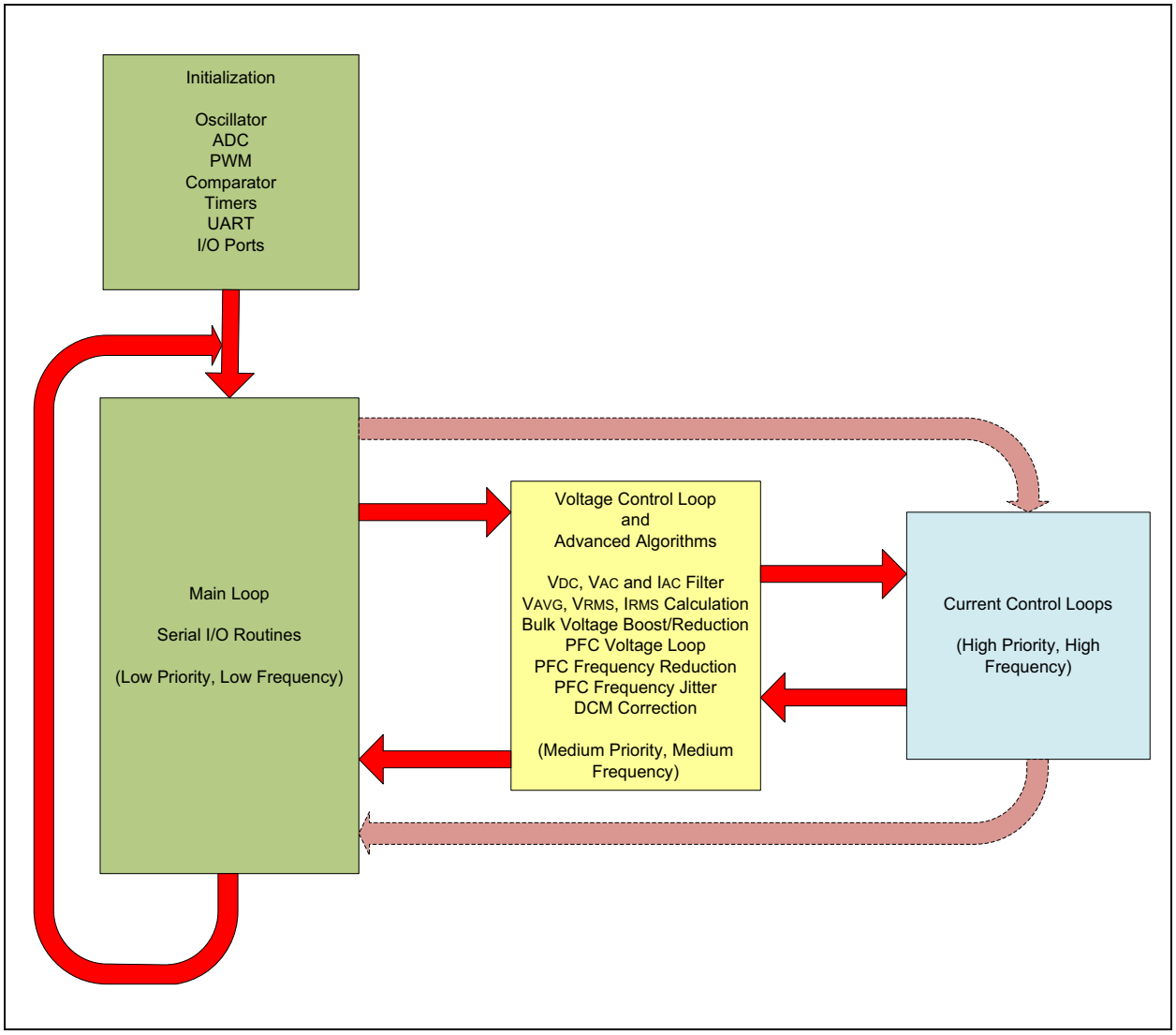
Each algorithm implemented on the system is arranged into one of these three priority levels. Figure 11 shows a high-level overview of the primary side software.

The dsPIC DSC features interrupt priority levels that allow critical algorithms to be executed at a deterministic rate without any software latencies. Code components are placed in a category based on the critical nature of the algorithm.

Highly time sensitive algorithms are generally categorized as high priority. The high priority is assigned to these critical algorithms through the variable interrupt priority levels of the dsPIC DSC. In addition to interrupt priority levels, these algorithms are also aided by smart scheduling of PWM triggers, ADC acquisitions and timer values for proper measurement and updates of system variables. This also facilitates proper CPU utilization between high and low priority algorithms.

For example, the current control loop for the PFC section is the most time-critical software component for the primary side software. By calling this routine from the highest priority Interrupt Service Routine (ISR), timing relationships for the control loop are maintained, and results of the control loop are applied to the hardware immediately when available.

FIGURE 11: PRIMARY SIDE SOFTWARE HIGH-LEVEL OVERVIEW



PFC FREQUENCY REDUCTION

To achieve the maximum efficiency for the system, the switching period of the PFC stage is modified when the system is operating in Steady state to minimize the switching losses. The switching frequency is adjusted dynamically, based on the current load condition. The different possible values for the PFC switching period are stored in a lookup table. The values from the lookup table are selected on the basis of the calculated current reference for the current control loop.

The PFC switching period is only modified for light load conditions, up to 50% load. If the load is found to be greater than 50% of the rated value, the switching period remains at the lowest value, or at the highest switching frequency.

When the system operates at light loads (i.e., < 50% load), the PFC switching frequency is compared to the value obtained from the lookup table. If the lookup table provides a period value greater than the existing value of the switching period, the existing value of the switching period is incremented in steps of 1 ns, thereby reducing the switching frequency. The slow increment of the period ensures that the period is reduced gradually, and does not interfere with the operation of the PFC control algorithms.

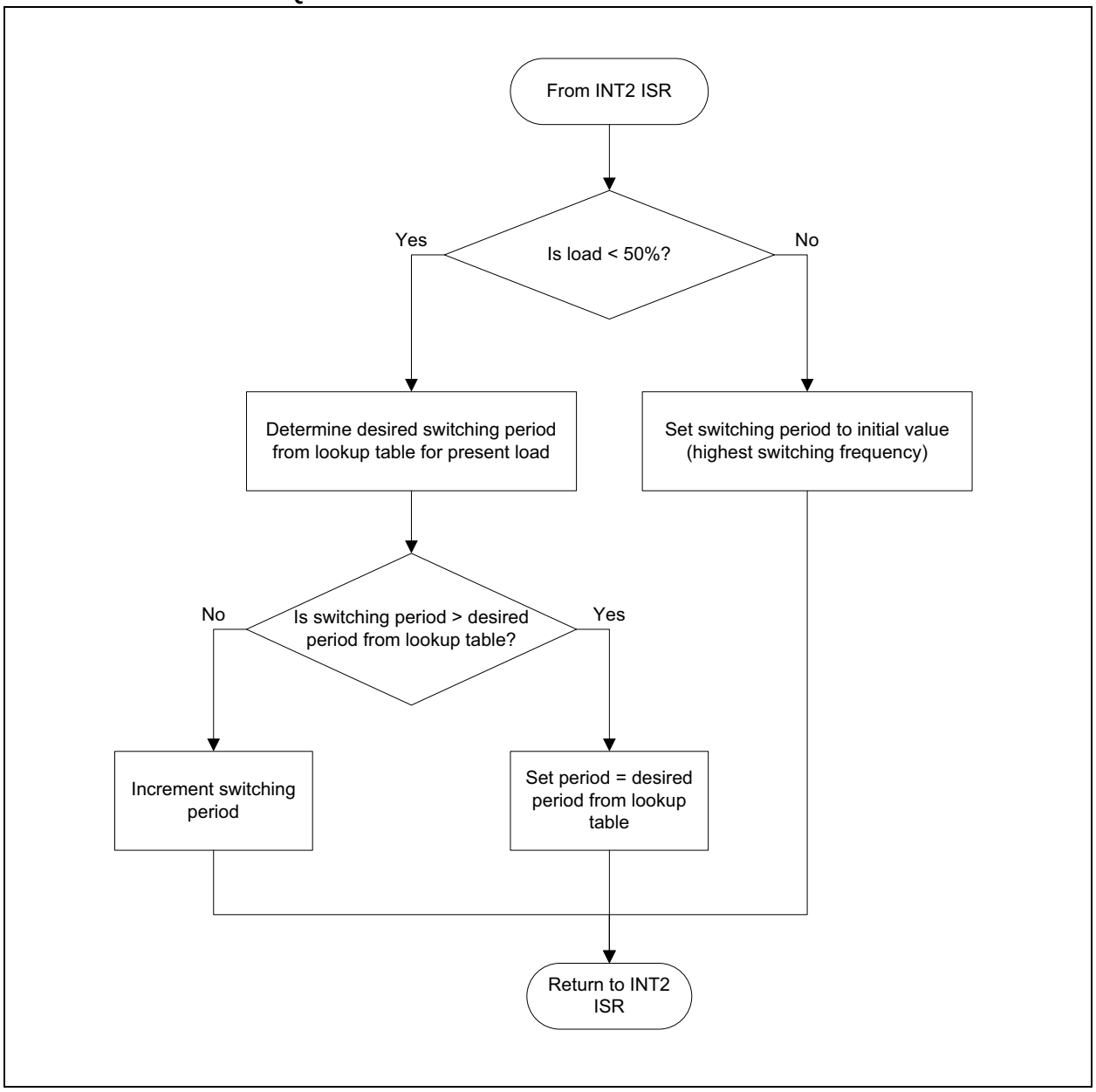
Conversely, if the value obtained from the PFC period lookup table corresponding to the measured current is lower than the existing PFC switching period, the PFC switching period is immediately changed to the lookup table value. This change is done to support any large transients that may have occurred since the last execution of the PFC frequency reduction algorithm. Figure 12 shows the flowchart of the PFC frequency reduction function.

The PFC control algorithms are based on a time domain approximation of the converter. Therefore, changing the switching frequency requires changes of the control loop output as well. This is done by multiplying the output of the current control loop, with the current period value. This ensures that the reduced sample frequency is compensated, irrespective of the switching period.

TABLE 3: TIMING INFORMATION

Algorithm	PFC Frequency Reduction
Calling function	INT2 ISR
Frequency of execution	150 Hz
Maximum instructions	90
CPU bandwidth utilization (@ 40 MIPS)	< 1 MIPS

FIGURE 12: PFC FREQUENCY REDUCTION



PFC FREQUENCY JITTER

A software frequency jitter algorithm is implemented to improve performance of EMI tests. The jitter algorithm achieves this by spreading the EMI noise generated by the system over a range of frequencies by triangular modulation of the switching frequency. The switching frequency is modulated within a range of approximately 8-10% of the current center frequency. As a result, the EMI generated by the system for a particular center frequency is detected to be lower than without the jitter algorithm.

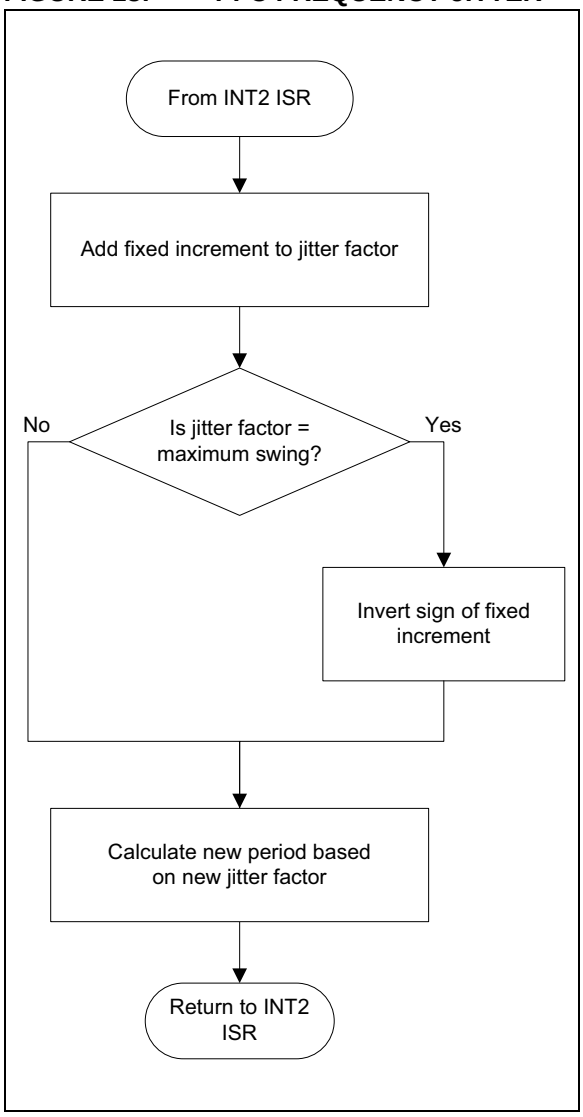
The jitter algorithm is located in the INT2 interrupt service routine which runs at a rate of 4800 Hz. Every time the algorithm is executed, a jitter factor is incremented or decremented by a fixed step size. The switching period is then scaled by the jitter factor to produce the frequency jitter. The jitter factor is incremented on every INT2 interrupt service routine until the maximum is reached, and then decremented until the minimum is reached. The jitter algorithm cycles through the increment and decrement of the jitter factor as long as the power supply is operating normally.

The jitter algorithm only allows for a small change in the switching period and is applied on top of the frequency reduction function discussed previously.

TABLE 4: TIMING INFORMATION

Algorithm	PFC Frequency Jitter
Calling function	INT2 ISR
Frequency of execution	4800 Hz
Max instructions	32
Approximate MIPS utilization	< 1 MIPS

FIGURE 13: PFC FREQUENCY JITTER



DCM CORRECTION

The interleaved PFC Boost converter is designed for continuous conduction mode (CCM). However, due to the sinusoidal modulation of the input current, the converter is forced into discontinuous conduction mode (DCM) near the zero crossings. This causes a change in the transfer function of the boost converter, and introduces distortion on the AC current waveform.

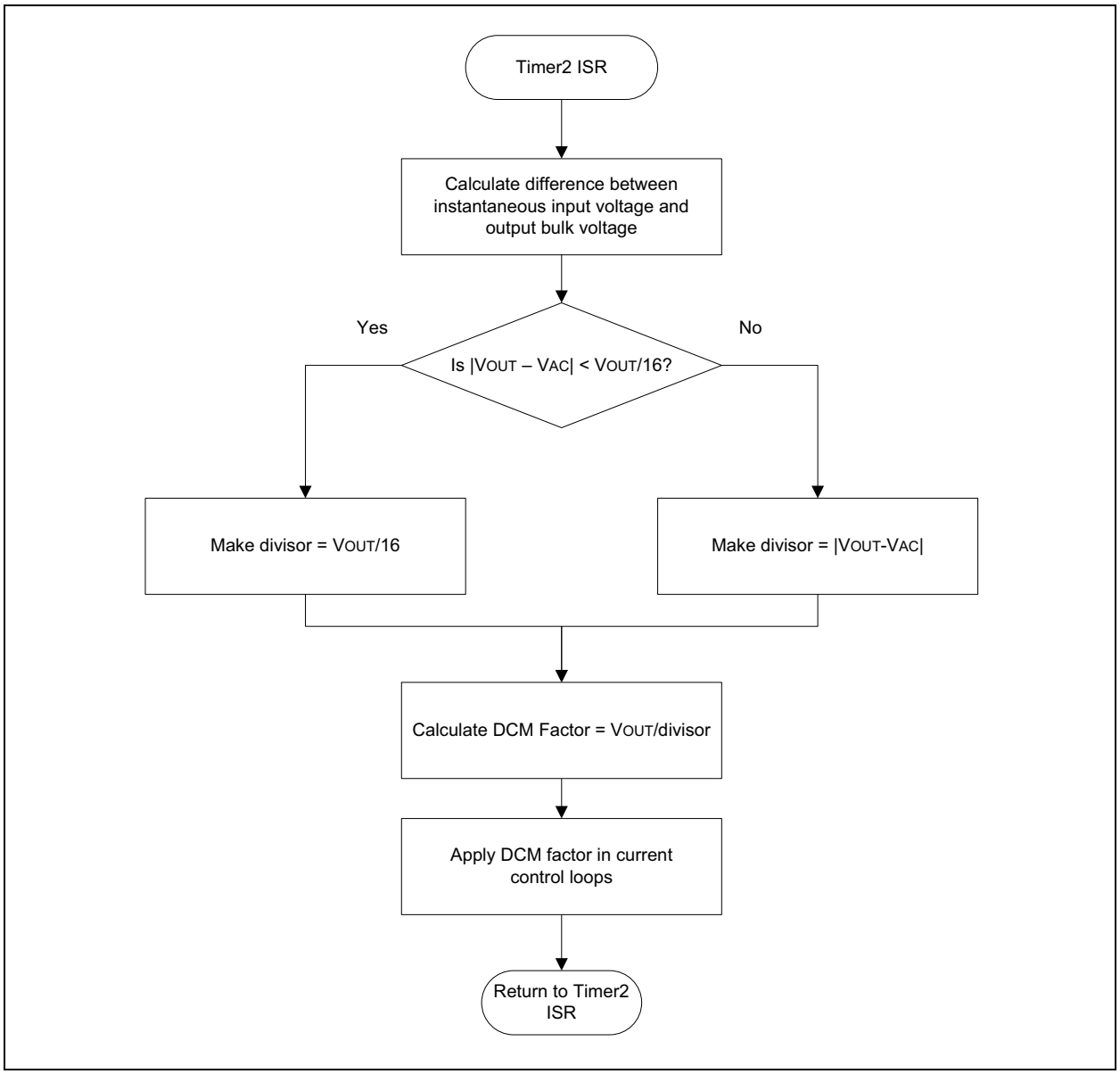
The primary side software adds a correction factor to the current control loop in the event of DCM operation. This correction factor is calculated as a ratio of the output bulk voltage to the difference between the output bulk voltage and the instantaneous input voltage. If the difference between these two parameters is smaller than a specific threshold, the DCM correction factor does not have any effect on the control loop.

The final output of the current control loop is multiplied by the DCM correction factor to produce the duty cycle for the PFC boost converter. The correction factor is applied equally to both interleaved stages of the converter.

TABLE 5: TIMING INFORMATION

Algorithm	DCM Correction
Calling function	Timer2 ISR
Frequency of execution	19200 Hz
Max instructions	55
CPU bandwidth utilization (@ 40 MIPS)	1 MIPS

FIGURE 14: DCM CORRECTION



BULK VOLTAGE REDUCTION AND BOOST FUNCTION

The output bulk voltage of the PFC stage is lowered under Steady state to improve the efficiency at light loads. This is directly controlled from the secondary side, by transmitting the load current information back to the primary side.

When the primary side receives the load current information, it uses a lookup table to determine what bulk voltage will be sufficient to maintain output voltage regulation on the secondary side. The primary side software then compares the value obtained from the lookup table to the current bulk voltage. If the value from the lookup table is lower than the present bulk voltage, the reference for the voltage loop is slowly decremented until it becomes equal to the voltage from the lookup table.

Conversely, if the voltage from the lookup table is higher than the present bulk voltage, the reference for the voltage control loop is increased instantly to the lookup value. This is done to account for any load transients that may have occurred on the secondary side, and the bulk voltage must be raised as quickly as possible to maintain regulation on the secondary side.

The bulk voltage boost function is used to increase the setpoint of the PFC output bulk voltage in the event of a large load transient on the secondary side. This function helps to improve the transient response characteristics of the DC/DC converter by providing advance indication of a load transient to the PFC controller. This function is also used to reset the switching frequency of the PFC stage, (see **"PFC Frequency Reduction"** for details).

The bulk voltage boost function is implemented through the serial communication channel between the primary and secondary sides. The secondary side transmits the desired bulk voltage based on load conditions. If this desired voltage is greater than the measured bulk voltage by 25V or more, the bulk voltage reference is replaced with the desired value obtained from the secondary side.

The bulk voltage boost function and the bulk voltage reduction function operate with conflicting objectives. However, the boost function is only applied during a transient condition, while the voltage reduction is applied at Steady state. The voltage boost function, if applied, takes priority over the operation of the bulk voltage reduction routine.

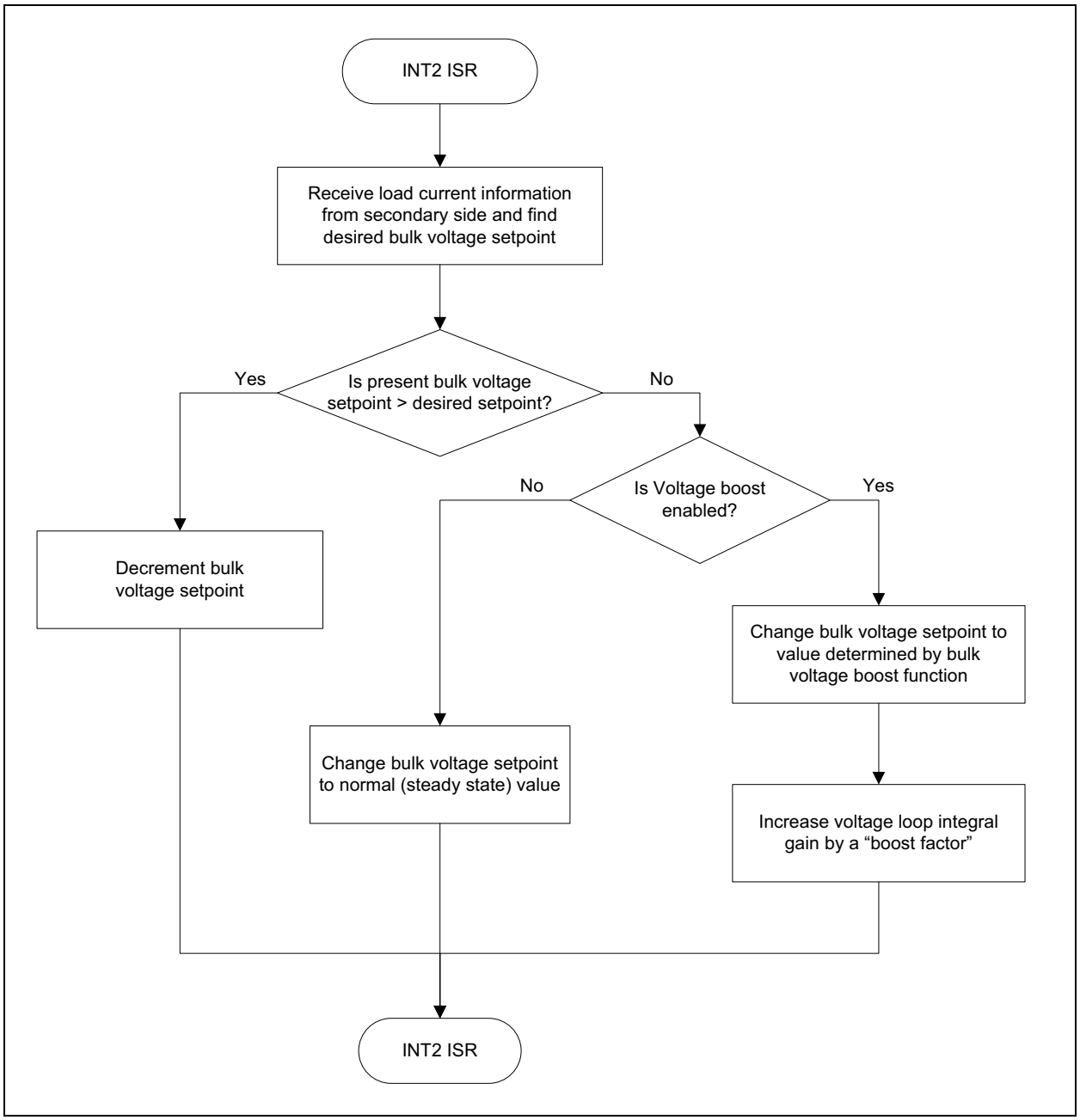
In addition to the instantaneous boost of the bulk voltage, the voltage control loop operation is also modified to counter large load transients. When a voltage undershoot of 25V or greater is detected, the integral term of the PI controller is increased by a "boost factor" to improve the response of the system.

Figure 15 illustrates the operation of the bulk voltage reduction and boost routine.

TABLE 6: TIMING INFORMATION

Algorithm	Bulk Voltage Reduction and Boost
Calling function	INT2 ISR
Frequency of execution	4800 Hz
Max instructions	84
Approximate MIPS utilization	< 1 MIPS

FIGURE 15: BULK VOLTAGE REDUCTION AND BOOST FUNCTION



PFC CONTROL LOOP IMPLEMENTATION

The PFC control loops are implemented as average current mode control, with the addition of a sine modulated current waveform. The outer voltage loop is executed in the INT2 interrupt service routine, that is triggered in software once every four Timer2 period rollovers. The effective execution rate for the voltage loop is 4800 Hz. The voltage control loop is implemented as a 32-bit Proportional-Integral (PI) type compensator.

The block diagram of the primary side control scheme is shown in Figure 16.

The output of the voltage control loop is an average current value, which is multiplied by the instantaneous rectified input line voltage, and divided by the square of the average rectified input voltage. This operation achieves three goals: 1) it causes the average current to be modulated into a sinusoidal shape, 2) removes the effects of magnitude of the input voltage, and 3) adds an input voltage feed-forward term to the control loop to improve line regulation. Finally, the sine modulated current is used as the reference for the inner current control loops for the interleaved PFC boost converter.

The inner current loops are implemented independently for each phase of the interleaved PFC boost converter. The current control loops are executed inside the ADC interrupt service routine to ensure that the measured current is processed as quickly as possible, as any additional delays will have a negative impact on the phase margin.

Information about advanced algorithms such as the bulk voltage reduction, switching frequency reduction and DCM correction is passed into the control loop structure and used during the execution of the respective control algorithms.

TABLE 7: TIMING INFORMATION

Algorithm	PFC Sine Modulation
Calling function	Timer 2 ISR
Frequency of execution	19200 Hz
Max instructions	56
CPU bandwidth utilization (@ 40 MIPS)	1 MIPS

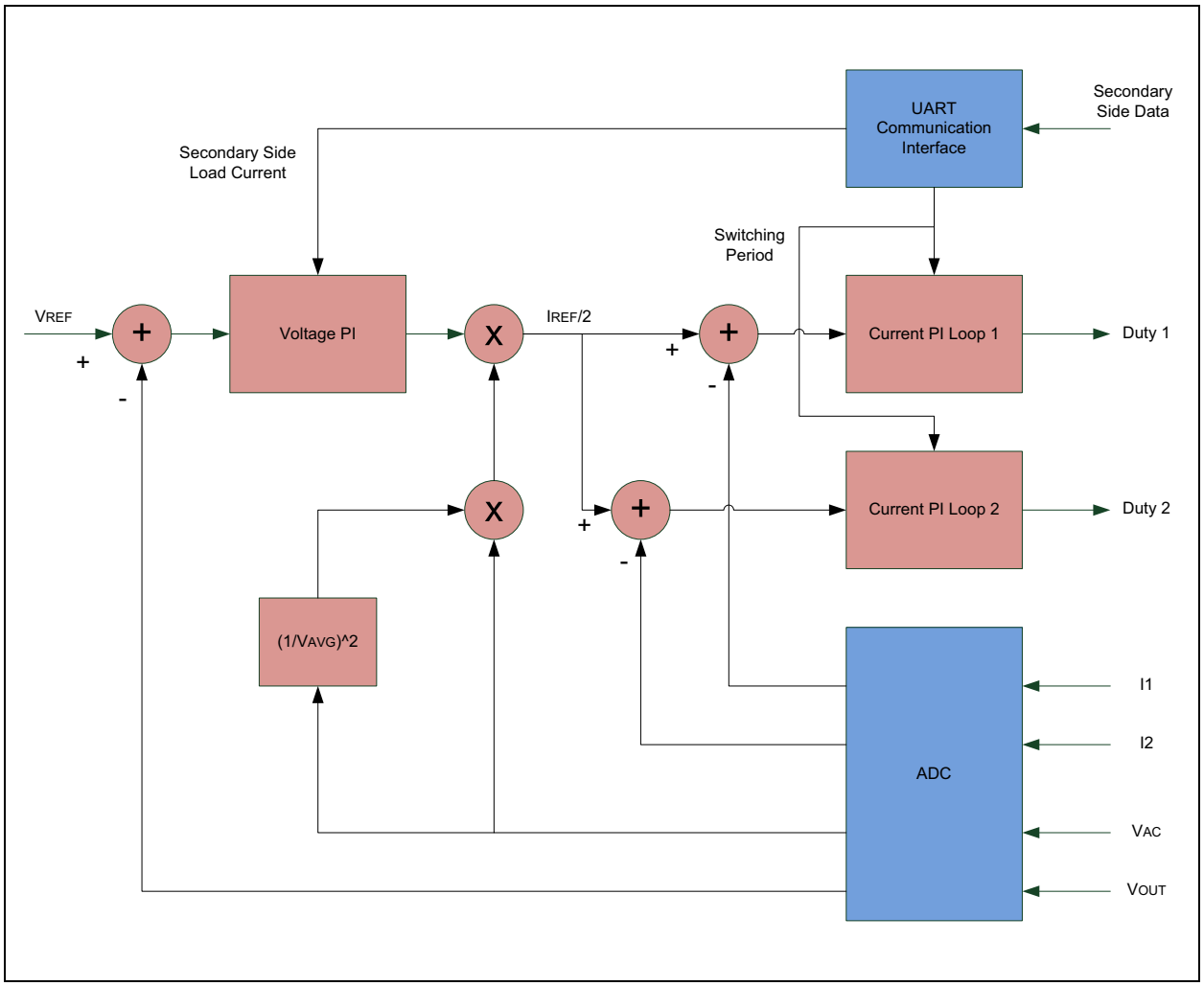
TABLE 8: TIMING INFORMATION

Algorithm	PFC Voltage PI Loop
Calling function	INT2 ISR
Frequency of execution	4800 Hz
Max instructions	34
CPU bandwidth utilization (@ 40 MIPS)	< 1 MIPS

TABLE 9: TIMING INFORMATION

Algorithm	PFC Current PI Loop (One Per Interleaved PFC Stage)
Calling function	ADCP0 ISR, ADCP1 ISR
Frequency of execution	96 kHz
Max instructions	105
CPU bandwidth utilization (@ 40 MIPS)	10 MIPS each (20 MIPS total)

FIGURE 16: PFC CONTROL LOOP



PRIMARY SIDE FAULT HANDLING

The Platinum-rated AC/DC Reference Design implements a number of Fault protections to minimize damage to the system and connected load, while at the same time minimizing down time for the power supply. The Fault handling routines are implemented in appropriate sections of the software. The following is a description of various Fault handling routines on the primary side:

- **PFC Overcurrent Limit:** The PFC over-current limit is implemented as a comparator threshold, to detect over-current conditions during the switching cycle. When the comparator input exceeds the programmed threshold, the PWM duty cycle will be truncated automatically. No system shutdown occurs if an over-current condition has been detected, but this fault prevents excessive current through the PFC MOSFETs. The maximum current limit is specified as the peak current value plus some margin at 110V input voltage.
- **Input Undervoltage/Overvoltage Shutdown:** This reference design is configured to operate as low as 40 VAC input voltage. However, any operation below 110V is derated for maximum power. If the input voltage drops below 40 VAC or exceeds 275 VAC, the output is turned OFF.
- **PFC Output Bulk Voltage Overvoltage/ Undervoltage Fault:** If the PFC output voltage falls below 375V or exceeds 408V, the output is shut down.

PRIMARY SIDE TIMING RELATIONSHIPS

Due to the multitasking nature of the system software, a number of important algorithms must be scheduled properly to maximize performance, and also efficiently utilize the available CPU bandwidth.

The primary side software is written in an interrupt-based format, where algorithms are divided into high, medium, and low priority tasks. The ADC ISRs are assigned the highest priority, during which the current control loops are executed and the PWM duty cycle is updated. The PWM trigger feature is utilized to generate analog-to-digital conversion requests. The PWM triggers enable the ADC sampling to take place synchronous to the PWM signal. The PWM trigger is adjusted on every switching period to the middle of the active duty cycle. In Continuous Conduction Mode, this technique averages the current ripple on top of its DC component, giving the average value directly without any need for further filtering. In Discontinuous Conduction Mode this technique gives the average current of the current on-time. However, the period where the current is zero adds to the result as a negative offset and is compensated by a correction factor as described previously in the **"DCM Correction"** section.

The medium priority tasks are executed in the Timer2 ISR, which is configured to generate an interrupt at a rate of 19200 Hz. Additional medium priority tasks are performed in the INT2 ISR, which is manually triggered in software once every four Timer2 ISRs. This results in an effective interrupt rate of 4800 Hz for the INT2 interrupt, and it enables algorithms running at different rates to be incorporated in the medium priority interrupts.

Finally, the low priority tasks are executed in the main loop, as they are not critical for the system operation. The low priority tasks are executed at any time when no high or medium priority interrupts are requested.

Figure 17 and Figure 18 describe the various timing relationships on the primary side software.

Note:	The timing diagrams are drawn showing relative trigger events. Block size does not represent actual algorithm duration.

FIGURE 17: PRIMARY SOFTWARE TIMING DIAGRAM (HIGH PRIORITY ALGORITHMS ONLY)

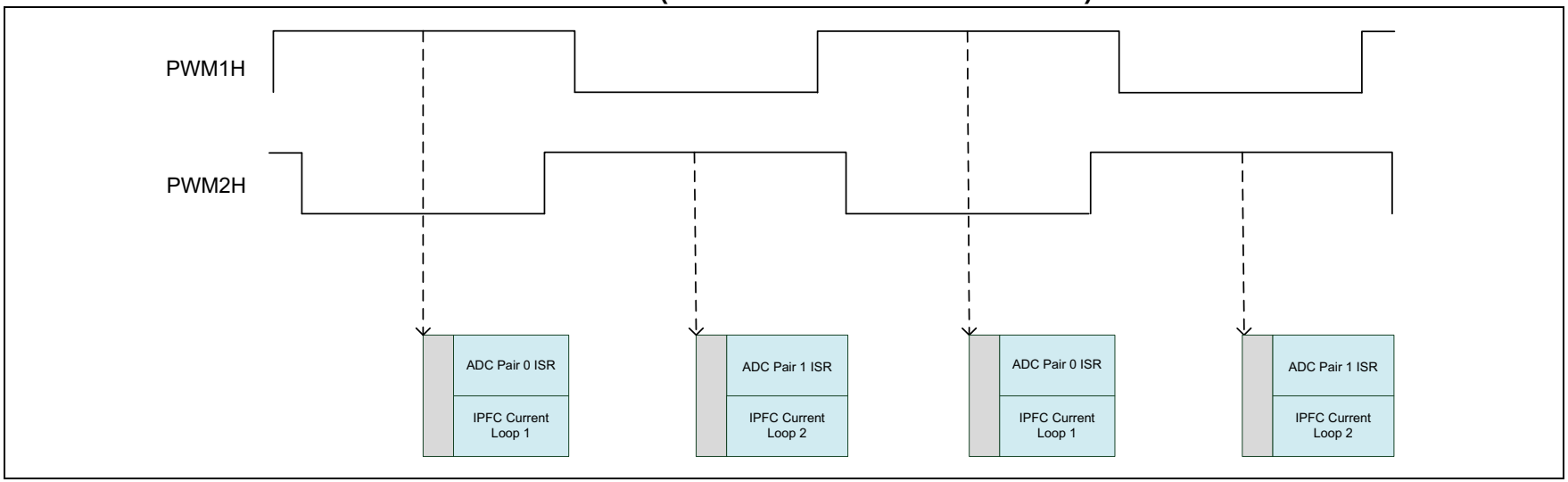
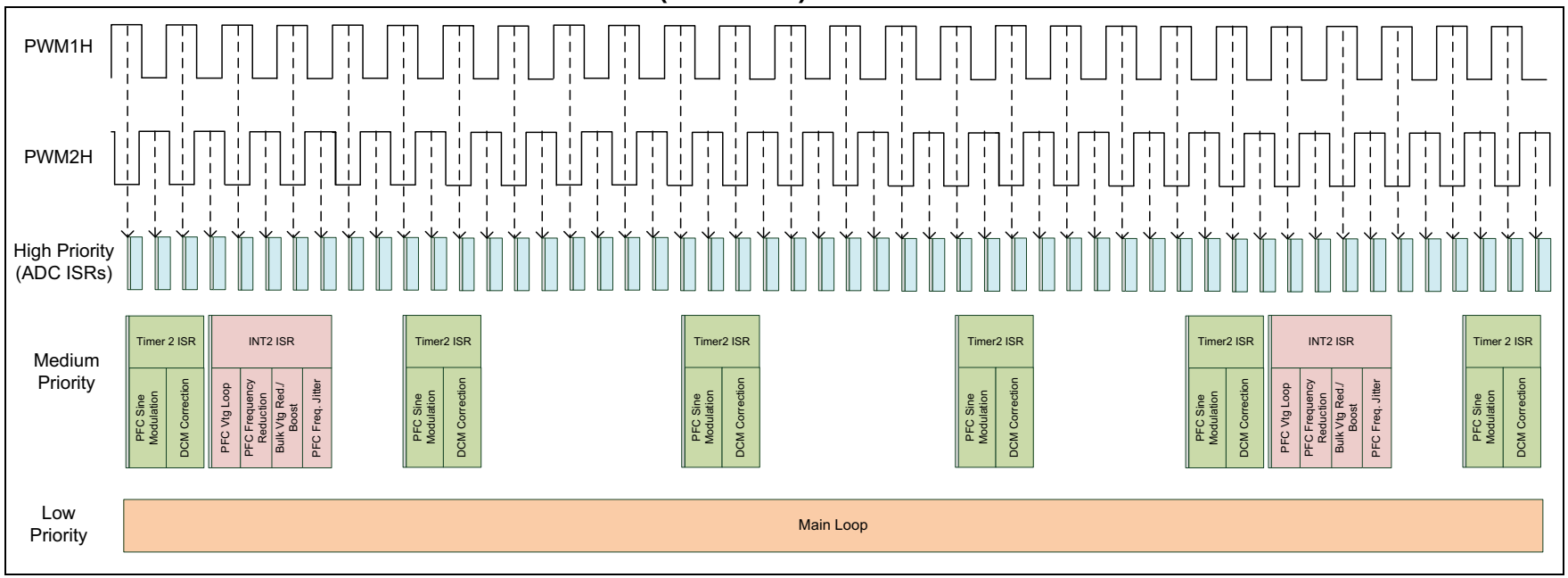


FIGURE 18: PRIMARY SOFTWARE TIMING DIAGRAM (COMPLETE)



Secondary Side

HIGH-LEVEL SOFTWARE OVERVIEW

The secondary side software is structured similar to the primary side. The code is divided into three main categories, as follows:

- **Low Priority:** Initialization Routines, Serial I/O Routines, Synchronous Rectifier Control, Power Derating Control, Fault Handling
- **Medium Priority:** Frequency Reduction, Frequency Jitter, Soft-start and Load Sharing
- **High Priority:** Voltage and Current Control Loops, Load Feed-forward

All high priority tasks are performed as a part of Interrupt Service Routines (ISRs). On the secondary side software, the power control algorithms are assigned the highest priority, as they directly affect the performance of the output.

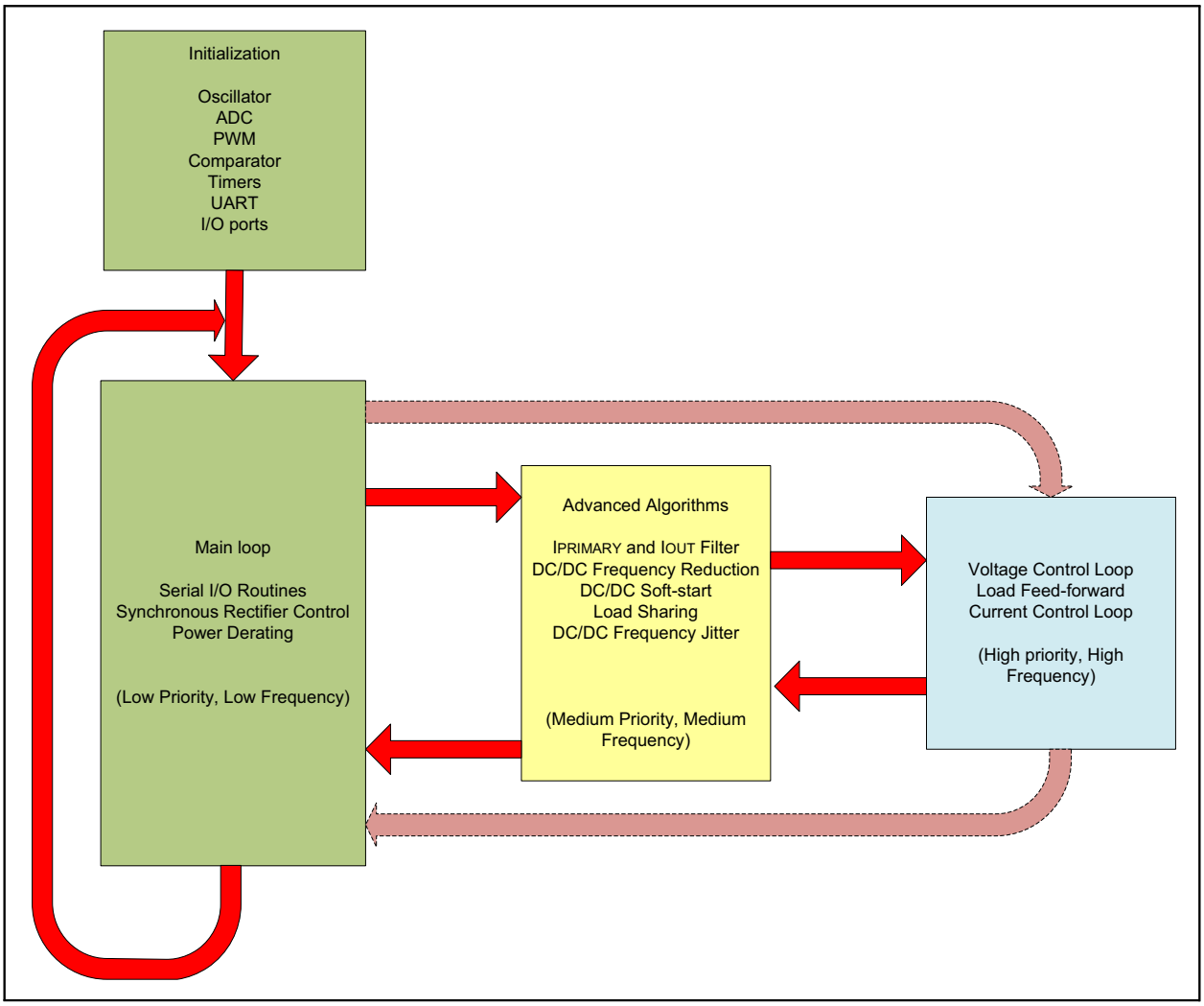
The power control algorithms consist of the voltage and current control loops, and both are executed as part of the PWM special event ISR. As a result, this interrupt is assigned the highest priority in the secondary side software.

The medium priority code comprises many advanced algorithms that are designed to improve a number of performance factors, including efficiency, transient response, and load sharing. These various algorithms are still interrupt-based, but are executed from medium priority ISRs. The Timer1 and Timer2 interrupts are utilized for executing the medium priority code. The timer rollover frequencies are specified as 5 Hz for Timer1 and 4800 Hz for Timer2.

All non-critical tasks are included in the low priority algorithms and are called from the main loop. These algorithms have no critical impact to the system, and are mainly used for status reporting or optimization of performance.

More detail on various algorithms is presented in subsequent sections.

FIGURE 19: SECONDARY SIDE SOFTWARE HIGH-LEVEL OVERVIEW



DC/DC FREQUENCY REDUCTION

The secondary side frequency reduction is implemented in a fashion similar to that of the primary side. In this case, the software relies on the load current measured. Based on the value of the load current, the desired switching period value is obtained from the period lookup table. Once the desired switching period is calculated, the period is updated before executing the current control loops for the DC/DC converter. The flowchart for the frequency reduction algorithm is shown in Figure 20. The switching frequency can only be modified in the range between 80 kHz and 96 kHz, due to physical limitations of the 2-switch forward converter.

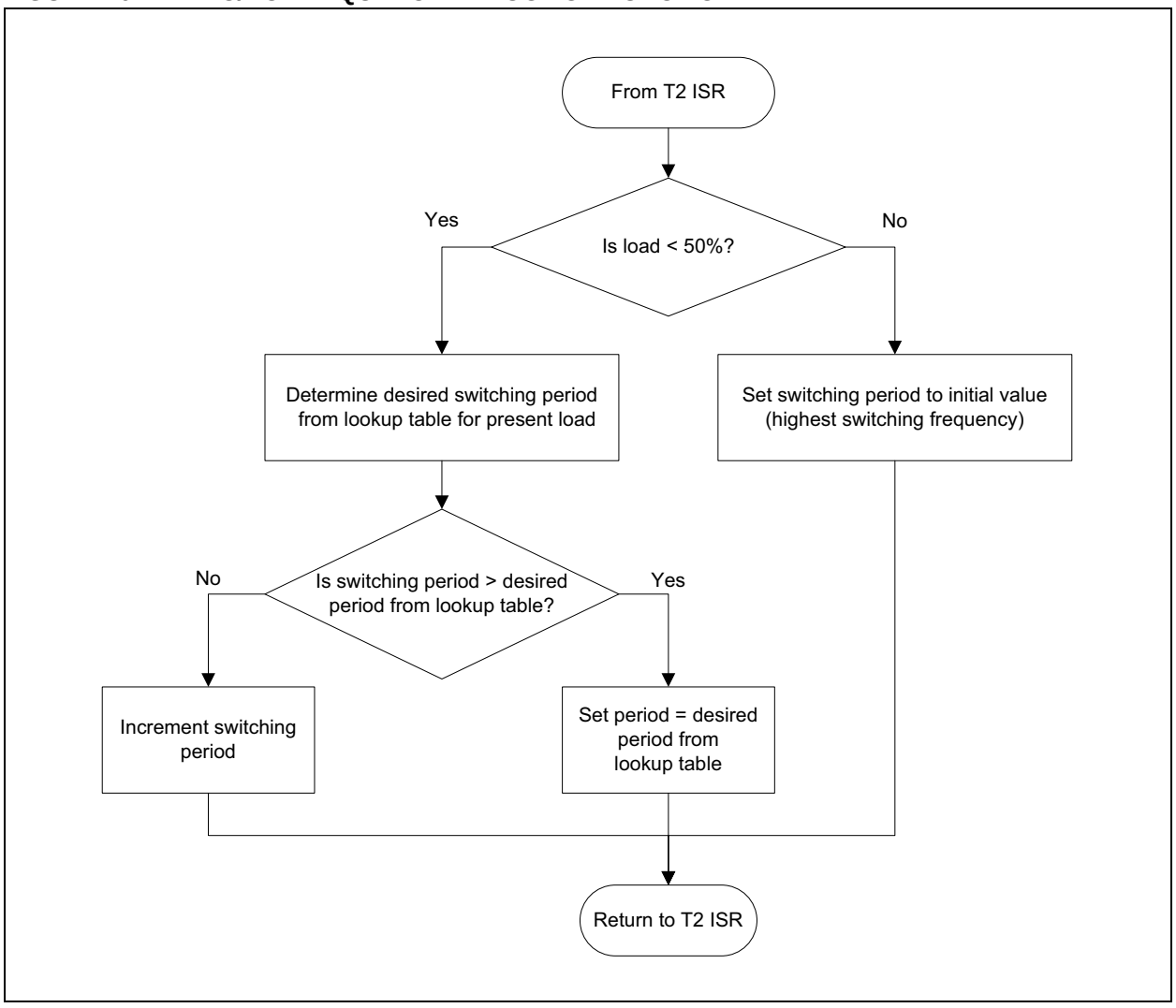
If the period value from the lookup table is found to be higher than the present switching period, the period is incremented slowly until it reaches the lookup period value.

If the period value obtained from the lookup table is lower than the present switching period, then the period is instantaneously changed to the desired value. This is required to maintain a good transient response.

TABLE 10: TIMING INFORMATION

Algorithm	DC/DC Frequency Reduction
Calling function	Timer2 ISR
Frequency of execution	4800 Hz
Max instructions	46
Approximate MIPS utilization	< 1 MIPS

FIGURE 20: DC/DC FREQUENCY REDUCTION FUNCTION



DC/DC FREQUENCY JITTER

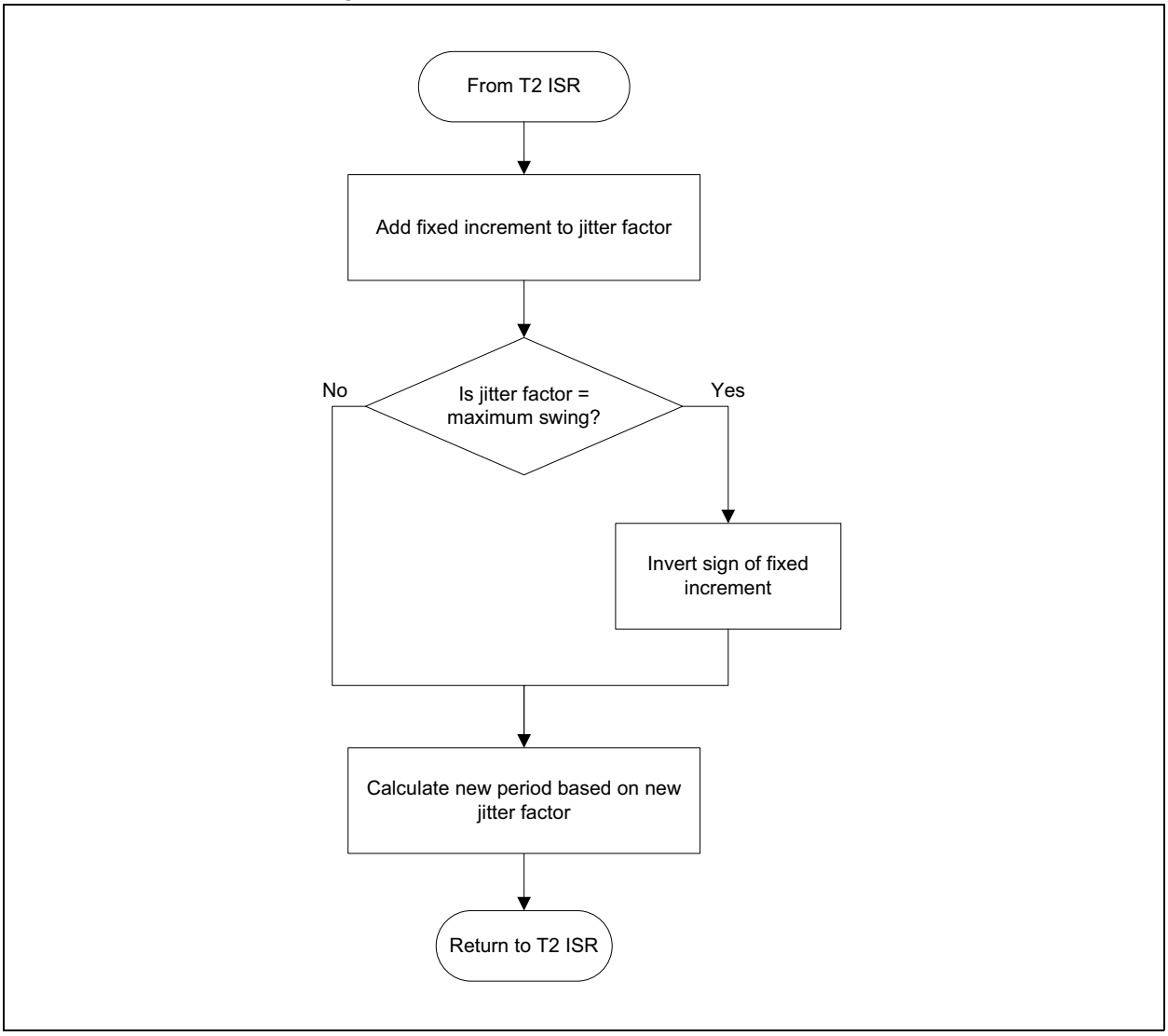
The frequency jitter algorithm on the DC/DC converter is identical to that on the primary side, described previously. The only differences are that for the DC/DC converter, the frequency jitter algorithm is executed as part of the Timer2 ISR. The minimum and maximum limits of the frequency swing are also adjusted based on the switching frequency of the DC/DC converter. The main aim of the frequency jitter algorithm is to improve the EMI performance of the system.

The flowchart for the DC/DC frequency jitter algorithm is shown in Figure 21.

TABLE 11: TIMING INFORMATION

Algorithm	DC-DC Frequency Jitter
Calling function	Timer2 ISR
Frequency of execution	4800 Hz
Max instructions	32
Approximate MIPS utilization	< 1 MIPS

FIGURE 21: DC/DC FREQUENCY JITTER



DC/DC CONTROL LOOP IMPLEMENTATION

The DC/DC control loops are implemented as average current mode control, with an inner current control loop and an outer voltage control loop. The execution of the control loops is scheduled in software using the PWM special event interrupt. Both the voltage and current loops are implemented as 32-bit Proportional-Integral (PI) type compensators. The voltage control loop also adds a load feed-forward term to improve response time. A block diagram of the control scheme for the DC/DC converter is shown in Figure 22.

The PWM switching for the interleaved DC-DC converters is configured to be 180° out of phase to minimize the ripple on the input and output current. The special event trigger is initialized to generate an interrupt at the beginning of the PWM period of the first interleaved DC/DC converter. In the first PWM special ISR, the voltage loop is executed and a load feed-forward term is also calculated. The voltage loop output and the feed-forward term are added together to provide a reference value for the current control loop. If a duty cycle value from the previous current loop execution is available, then the PWM duty cycle for one interleaved converter is updated.

At the end of the first ISR, the special event trigger is modified to the start of the interleaved PWM period, which is 180° out of phase. The current control loop is executed in this ISR using the current reference from the voltage control loop and the measured primary side current. The current control loop provides the duty cycle that is required to maintain regulation. The duty cycle for the second interleaved DC/DC converter is updated during this ISR.

TABLE 12: TIMING INFORMATION

Algorithm	DC-DC Current PI Loop
Calling function	PWM Special Event ISR
Frequency of execution	80 kHz
Maximum instructions	133
Approximate MIPS utilization	11 MIPS

TABLE 13: TIMING INFORMATION

Algorithm	DC-DC Voltage PI Loop and Load Feed-forward
Calling function	PWM Special Event ISR
Frequency of execution	80 kHz
Maximum instructions	182
Approximate MIPS utilization	15 MIPS

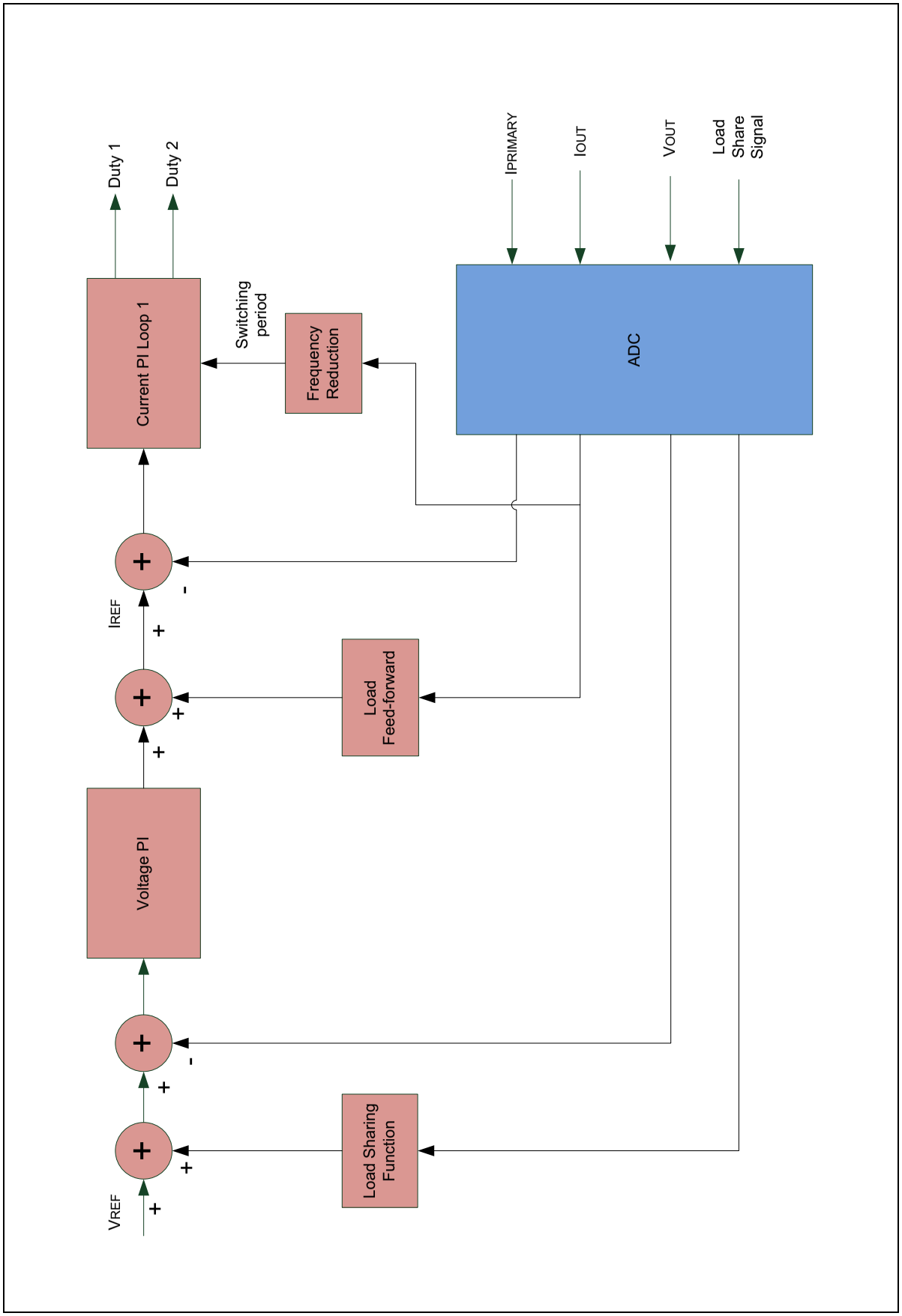


FIGURE 22: DC/DC CONTROL LOOP

SYNCHRONOUS RECTIFIER CONTROL

The synchronous rectifiers on the secondary side are controlled based on the load current to maximize efficiency of the system. At light loads, the switching losses in the synchronous rectifiers dominate compared to the conduction losses. Therefore, the switching of the synchronous rectifiers is turned OFF for loads below 8A, and the body diodes of the MOSFETs are utilized for the rectification.

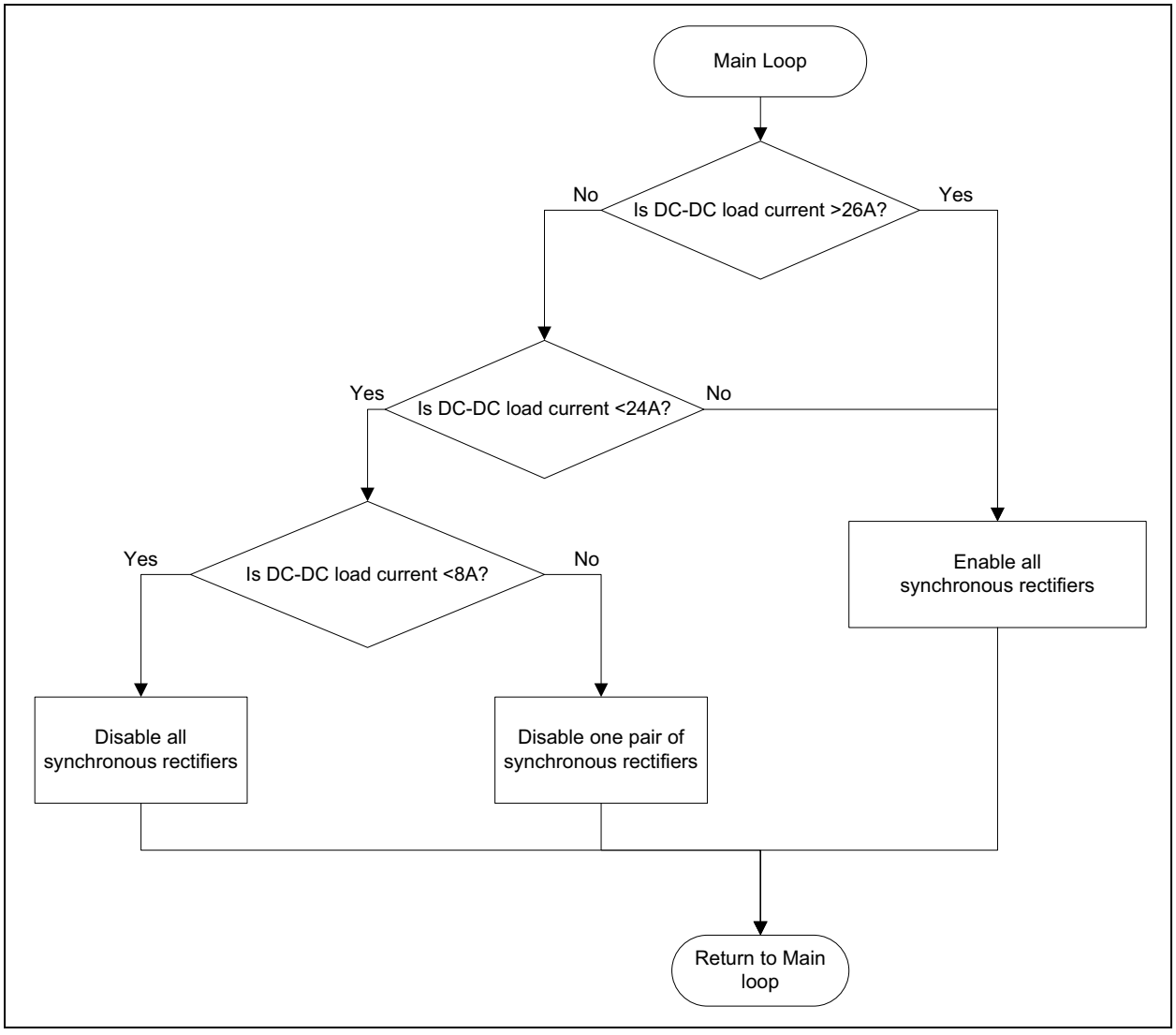
The system utilizes two pairs of synchronous MOSFETs connected in parallel. When a load of 8A to 24A is detected, one pair of synchronous MOSFETs is disabled to reduce switching losses.

At loads greater than 26A, the conduction losses on the secondary side of the DC-DC converter dominate the power losses. Therefore both pairs of synchronous MOSFETs are enabled to provide the lowest possible on-state resistance and therefore the highest possible efficiency.

TABLE 14: TIMING INFORMATION

Algorithm	Synchronous Rectifier Control
Calling function	Main loop
Frequency of execution	N/A – will be executed when no interrupts are being processed
Maximum instructions	57
Approximate MIPS utilization	< 1 MIPS

FIGURE 23: SYNCHRONOUS RECTIFIER CONTROL



POWER DERATING BASED ON INPUT VOLTAGE

The system power is derated for input voltages below 110 VAC. However, the power derating function is implemented on the secondary side. This is achieved by transmitting the RMS input voltage value from the primary to the secondary side using the serial communications channel.

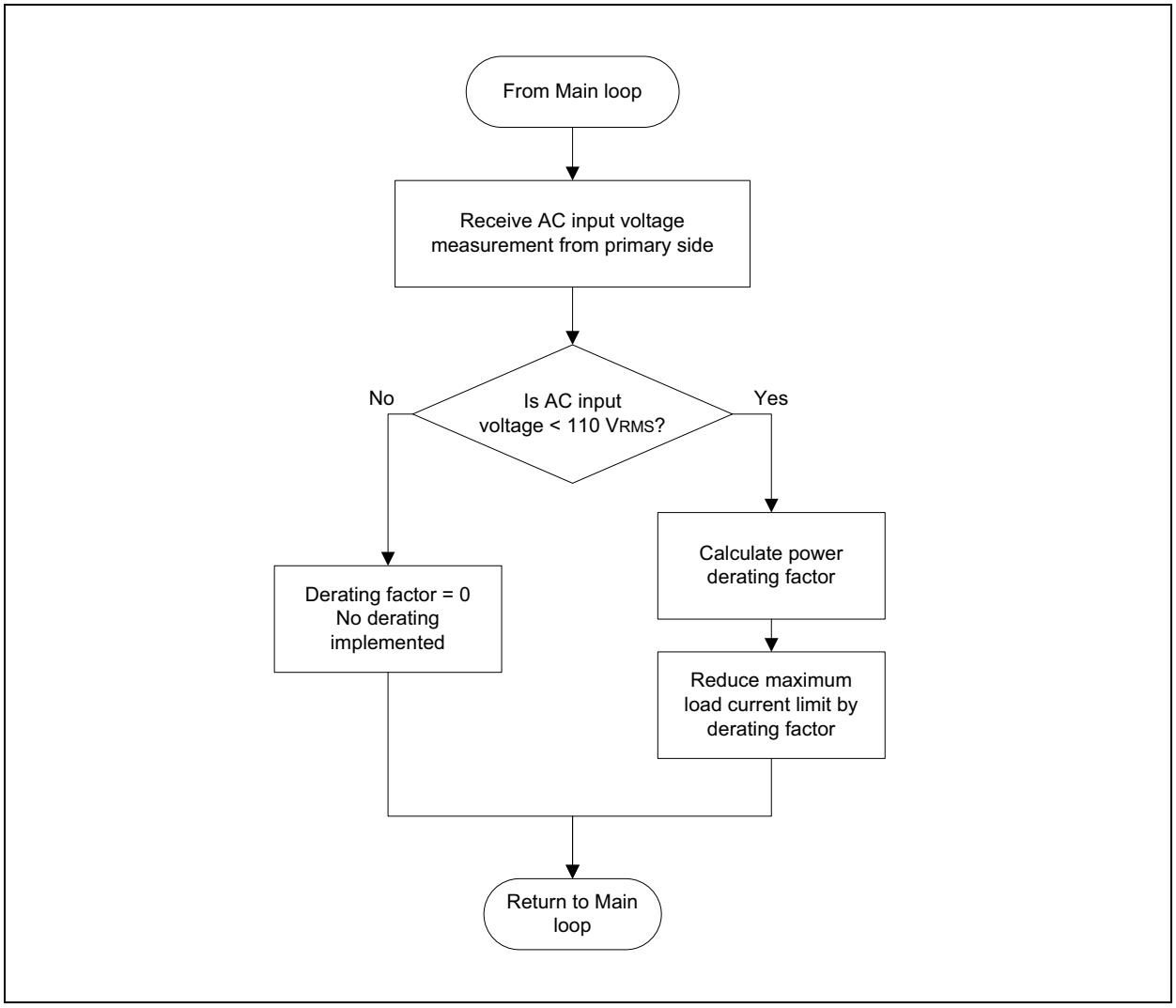
After receiving the RMS input voltage information on the secondary side, a derating factor is calculated. If the input voltage is found to be greater than 110 VAC, the derating factor is zero, and no power derating is applied. For input voltages that are below the threshold level, the derating factor is proportional to the deviation below the threshold.

The maximum load current limit is then reduced by an amount equal to the derating factor, to limit the maximum output power that the system will support. If the load current exceeds this new current limit, the system will enter the overcurrent Fault handling routine.

TABLE 15: TIMING INFORMATION

Algorithm	Power Derating
Calling function	Main loop
Frequency of execution	N/A – will be executed when no interrupts are being processed
Maximum instructions	57
Approximate MIPS utilization	< 1 MIPS

FIGURE 24: POWER DERATING



LOAD SHARING

The Platinum-rated AC/DC Reference Design supports parallel connection of multiple systems. This is accomplished with the help of a power supply OR-ing circuit, and a load share signal. The OR-ing circuit helps to isolate a singular failure on the shared voltage bus without interruption in the shared bus voltage.

Load sharing is achieved by generating a load-share signal that provides information about the present loading of the shared voltage bus, with respect to the combined load capacity of all the parallel supplies. This signal is generated by summing that from each individual supply connected on the shared voltage bus.

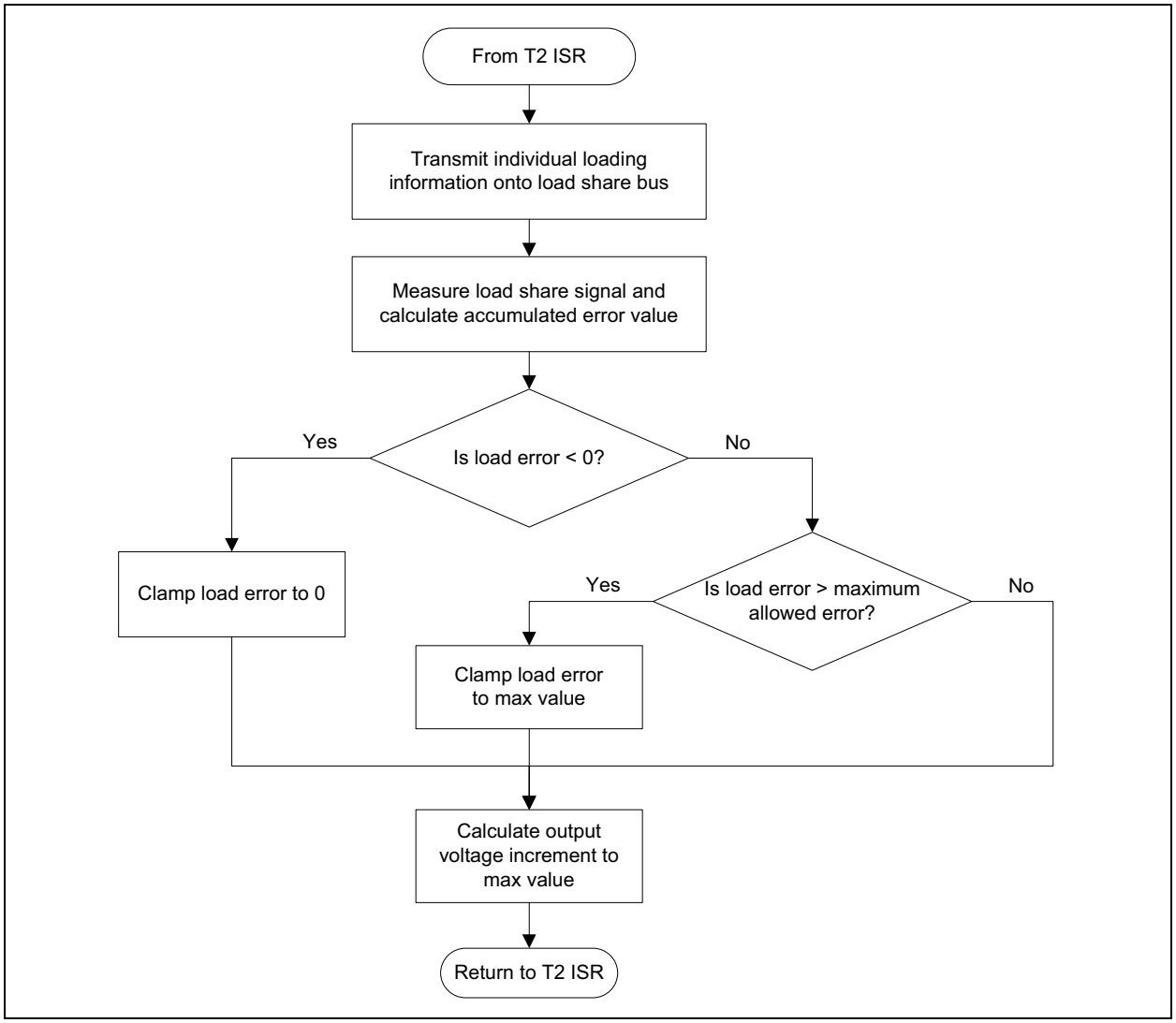
To achieve the load sharing function, each individual power supply compares this load-share signal with its own measured load. If the load-share signal is found to be greater than the loading of the individual supply, the load sharing algorithm increments the output voltage reference for the individual power supply until the load error is minimized.

If the load-share signal is detected to be lower than its own load, then the output voltage reference is decreased if the output voltage reference is between 12.0 V and 12.1 V DC to allow other PSUs to take the lead. If the current output voltage reference is within the range of 11.9V and 12.0 V DC, no action is taken as there is enough headroom for the other PSUs to take the lead. Figure 25 shows the flowchart for the load sharing function.

TABLE 16: TIMING INFORMATION

Algorithm	Load sharing
Calling function	Timer 2 ISR
Frequency of execution	4800Hz
Maximum instructions	117
Approximate MIPS utilization	< 1 MIPS

FIGURE 25: LOAD SHARING



SECONDARY FAULT HANDLING

There are additional faults that are handled from the secondary side, including the following:

- **Output Current Fault:** If the output load current is detected to be greater than the maximum rating, the software starts a time-out counter. This counter is configured to turn OFF the outputs if the overcurrent condition remains for more than 5 seconds.
- **Temperature Shutdown:** The reference design includes three temperature sensors on various locations on the board, identified as potential hot spots. These locations are:
  - On the bottom side of the board, below the primary side heat sink
  - On the bottom side of the board below the secondary side heat sink
  - On the bottom side of the board, near the fan connectors

All three temperatures are collected on the secondary side. There, they will be checked and the highest individual temperature will be used for fan control and shut down procedures.

The fans remain OFF below an ambient temperature of 60°C. Between an ambient temperature of 63°C to 70°C, the fans operate at 50% speed. Between 70°C to 80°C, they operate at 100%. Above 80°C, the output is turned OFF.

SECONDARY TIMING RELATIONSHIPS

The scheduling of various tasks on the secondary side is implemented in a fashion similar to the primary side.

The secondary side software is also interrupt based, and algorithms are divided into high, medium and low priority tasks. The PWM Special Event ISR is assigned the highest priority, during which the current and voltage control loops are executed on alternate interrupts. The PWM special event trigger is modified on every interrupt to allow measurement of currents in each interleaved phase of the DC/DC converter, while also keeping the ADC measurements synchronous to the PWM signal.

The medium priority tasks are executed in the Timer2 ISR, which is configured to generate an interrupt at a rate of 4800 Hz.

Finally, the low priority tasks are executed in the main loop, as they are not critical for the system operation. The low priority tasks are executed at any time when no high or medium priority interrupts are requested.

The diagrams in Figure 26 and Figure 27 describe the various timing relationships on the secondary side software.

Note:	The timing diagrams are drawn showing relative trigger events. Block size does not represent actual algorithm duration.

FIGURE 26: SECONDARY SIDE SOFTWARE TIMING DIAGRAM (HIGH PRIORITY ALGORITHMS ONLY)

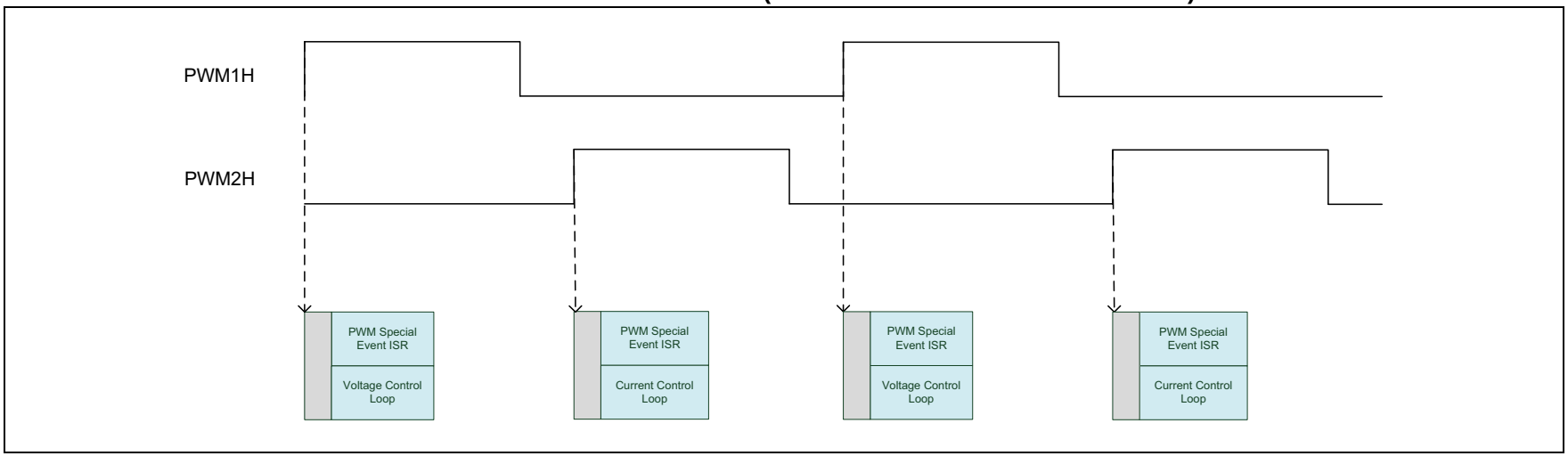
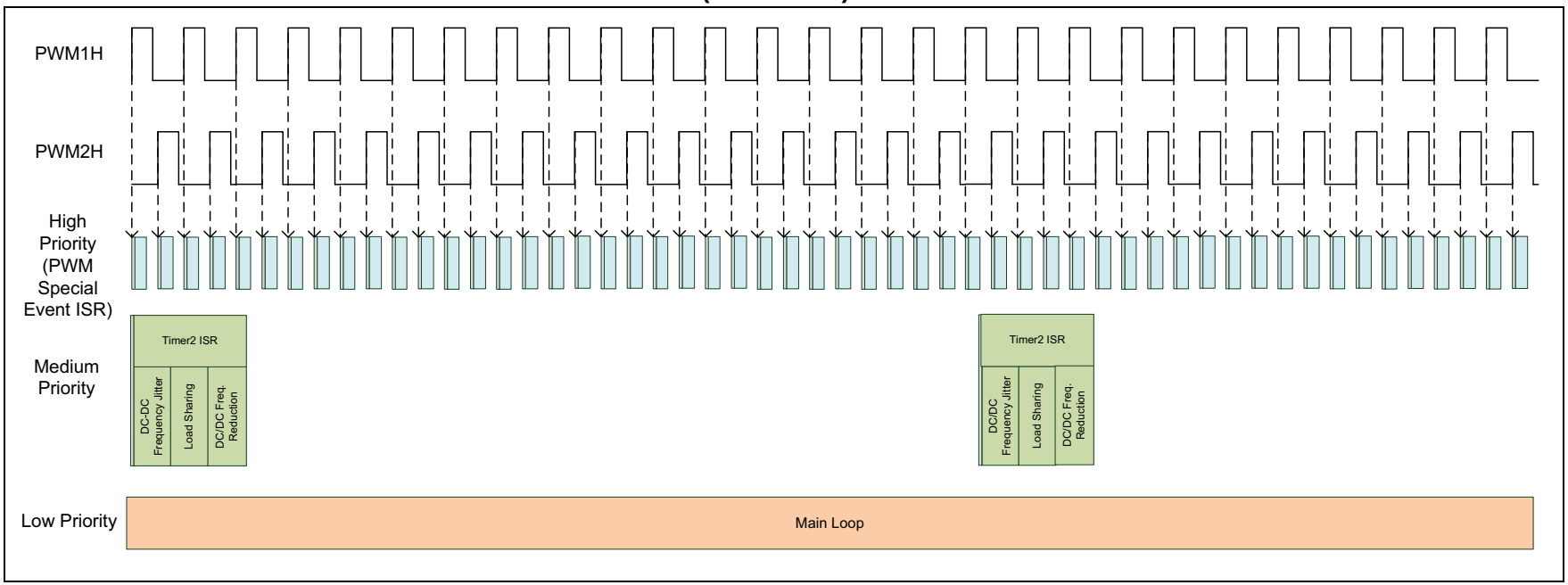


FIGURE 27: SECONDARY SOFTWARE TIMING DIAGRAM (COMPLETE)



SERIAL COMMUNICATIONS

The Platinum-rated AC/DC Reference Design exchanges data between the primary and secondary sides through an isolated serial communication interface. The UART module on the dsPIC DSC devices used on both sides is utilized for the communication.

The data transmitted from the primary side to the secondary side is listed in Table 17, while those transmitted from the secondary side to the primary side are listed in Table 18.

TABLE 17: PRIMARY TO SECONDARY DATA TRANSMISSION

Data Buffer Index	Parameter
0	PFC Output Bulk Voltage
1	PFC Input Voltage (RMS)
2	PFC Input Current
3	Primary Heat Sink Temperature
4	PFC Switching Period
5	PFC Current Loop Proportional Gain
6	PFC Current Loop Integral Gain
7	PFC Voltage Loop Proportional Gain
8	PFC Voltage Loop Integral Gain
9	PFC Status Flag

TABLE 18: SECONDARY TO PRIMARY DATA TRANSMISSION

Data Buffer Index	Parameter
0	DC/DC Output Voltage
1	DC/DC Output Current
2	PFC Control Flag

In addition to the primary-secondary serial communications, the reference design also configures the I^2C module on the secondary side to provide system status information (see Table 19). This information can be accessed by a remote client to monitor various operating conditions and system status information.

TABLE 19: SECONDARY TO I^2C CLIENT DATA TRANSMISSION

Data Buffer Index	Parameter
0	PFC Input Voltage (RMS)
1	PFC Input Current (RMS)
2	PFC Switching Period
3	PFC Output Bulk Voltage
4	Primary Heat Sink Temperature
5	PFC Current Loop Proportional Gain
6	PFC Current Loop Integral Gain
7	PFC Voltage Loop Proportional Gain
8	PFC Voltage Loop Integral Gain
9	PFC Status Flag
10	N/A
11	Load Share Bus Input
12	Load Share Bus Output
13	Load Share Bus Integrator Signal
14	N/A
15	N/A
16	DC/DC Switching Period
17	Synchronous Rectifier State
18	DC/DC Output Voltage
19	DC/DC Output Current
20	Secondary Temperature 1
21	Secondary Temperature 2
22	N/A
23	DC/DC Current Loop Proportional Gain
24	DC/DC Current Loop Integral Gain
25	DC/DC Voltage Loop Proportional Gain
26	DC/DC Voltage Loop Integral Gain
27	DC/DC Primary Current
28	DC/DC Primary Current filtered
29	Fault State
30	Maximum Output Current-Limit
31	Current-Limit Counter

NOTES:

APPENDIX A: DESIGN PACKAGE

A complete design package for this reference design is available as an executable installer. This design package can be downloaded from the Microchip corporate Website at: www.microchip.com

Design Package Contents

The design package contains the following items:

- System Firmware (Primary and Secondary)
- Schematics (PDF)
- PCB Drawings (PDF)
- Bill of Materials
- Demonstration instructions (PDF)
- System Overview (PDF)
- Efficiency Measurement Guidelines (PDF)
- Typical Test Results

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NOTES:

APPENDIX B: ELECTRICAL SPECIFICATIONS

The electrical specifications for the reference design are listed in Table 20.

TABLE 20: REFERENCE DESIGN SPECIFICATIONS

Specification	Minimum	Nominal	Maximum	Unit
Input Voltage Range	85	90 to 264	270	VAC
Input Frequency Range	47	—	63	Hz
Output Voltage	11.94	12.00	12.06	VDC
Output Current(1)	—	—	60	A
Power Rating	—	—	720	W
IPFC Switching Frequency	20	96	100	kHz
DC/DC Switching Frequency	70	96	100	kHz
Bulk Voltage	380	—	400	VDC
Hold-up Time(2)	20	30	32	ms
Input Current THD				
VIN: 115 VAC @ 60A	—	1.1	—	%
VIN: 230 VAC @ 60A	—	6.5	—	%
Power Factor				
VIN: 115 VAC @ 60A	—	0.99	—	—
VIN: 230 VAC @ 60A	—	0.99	—	—
Line Regulation	—	±0.7	±1	%
Load Regulation	—	—	±1	%
Output Ripple and Noise(3)	—	—	120	mVPP
Total Efficiency (10 … 100% of Load)	85.5	—	94.1	%
Stand-by Power (230 VAC)	—	—	2.8	W
Peak Inrush Current(4)	—	—	33	A
EMC(5)				
Open Frame	EN 55022, Class A			
Enclosed	EN 55022, Class B			

Note 1: Output is protected against sustained short-circuit conditions.

2: Values at a bulk voltage of 400V DC and 60A output load current.

3: Test performed with 60A output load current.

4: Test performed at 264 VAC, turn on at 90° and with 60A output load current.

5: Values taken under full load conditions at 110V AC input voltage.

NOTES:

APPENDIX C: TEST RESULTS

This appendix provides information on the test results for the reference design, as well as a few operational waveforms.

Efficiency

Figure 28 and Figure 29 highlight efficiency of the reference design. Figure 28 shows the efficiency at 230 VAC versus load and Figure 29 shows the efficiency at full load versus input voltage.

FIGURE 28: EFFICIENCY VS. OUTPUT LOAD CURRENT AT 230 VAC

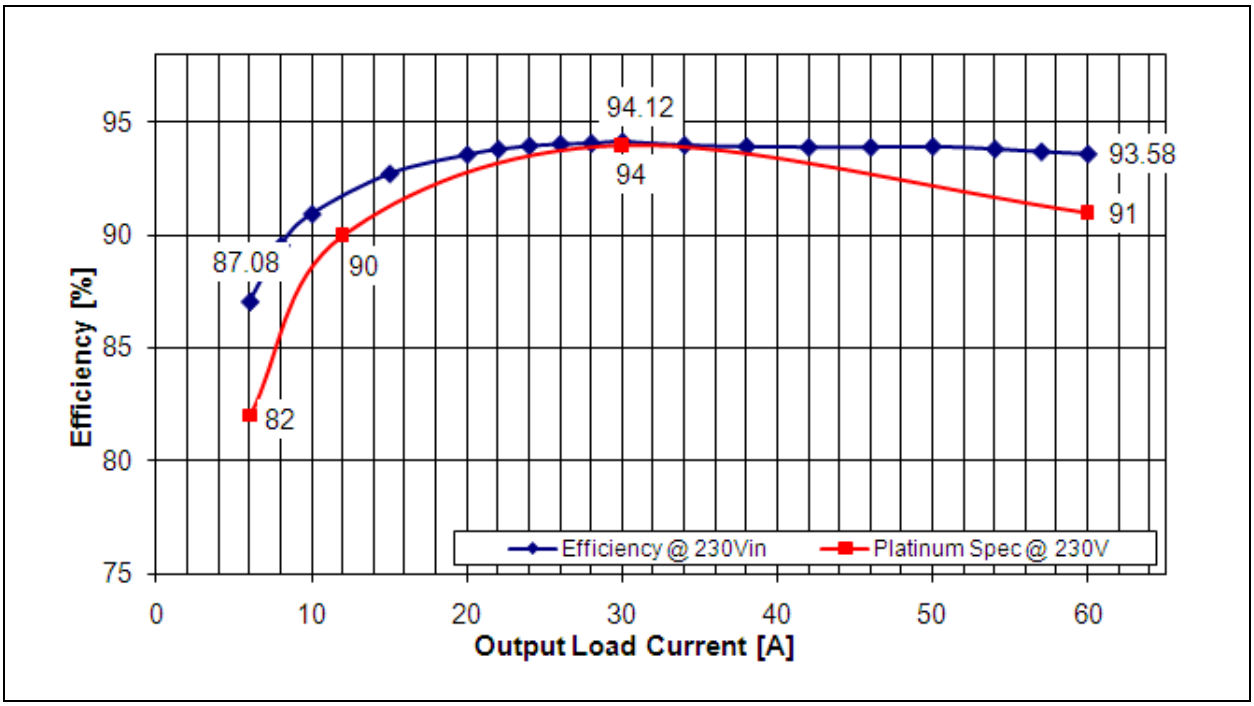
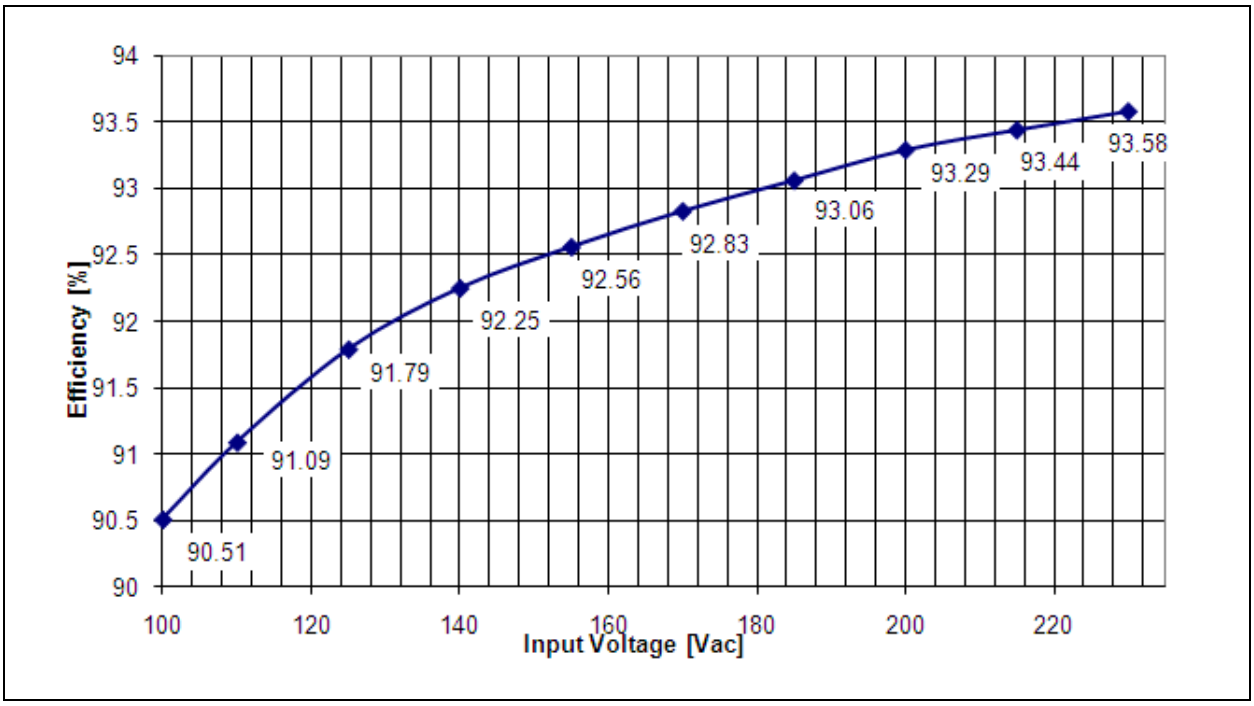


FIGURE 29: EFFICIENCY VS. INPUT VOLTAGE AT 60A OUTPUT LOAD CURRENT



Output Voltage Ripple

Output voltage ripple is measured across the output capacitors with the shortest possible probe ground lead. Figure 30 and Figure 31 show the output voltage ripple of the reference design at 115 VAC and 230 VAC, respectively.

FIGURE 30: OUTPUT VOLTAGE RIPPLE, IOUT: 60A, VIN: 115 VAC

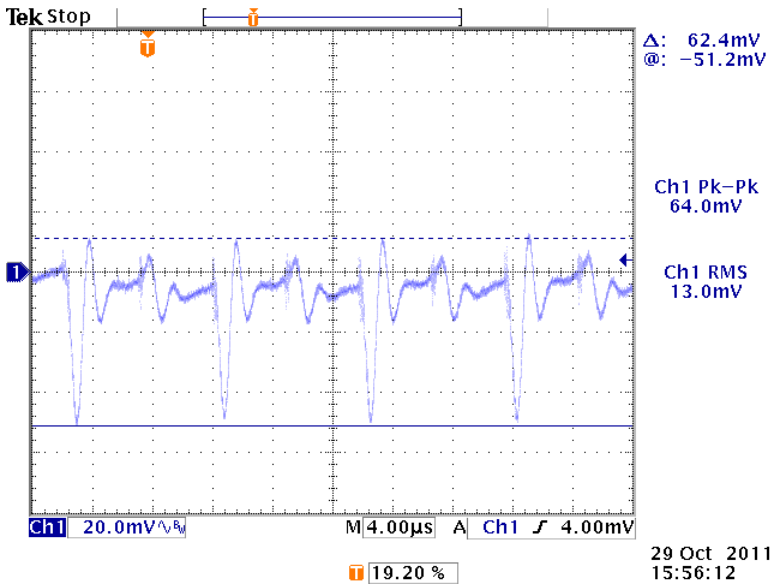
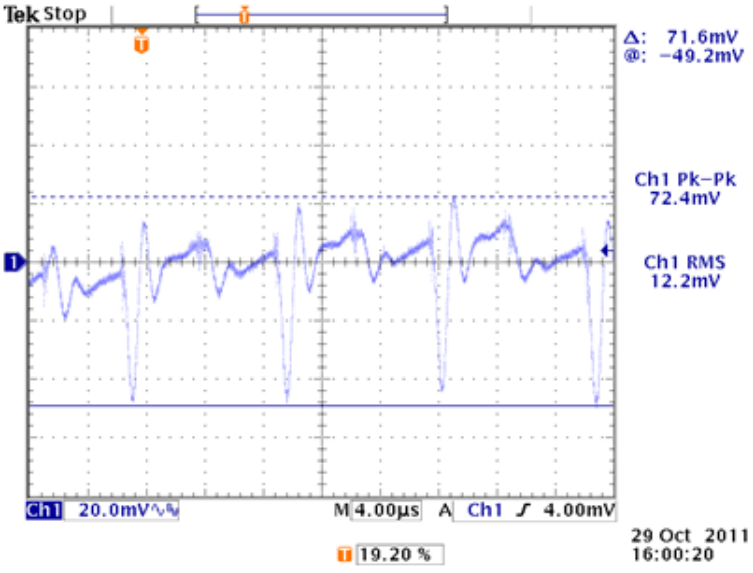


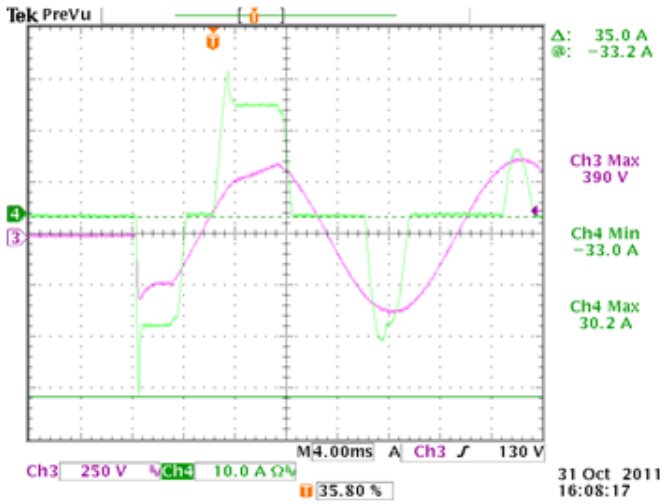
FIGURE 31: OUTPUT VOLTAGE RIPPLE, IOUT: 60A, VIN: 230 VAC



Inrush Current

Peak inrush current is measured at 264 VAC, 60A output load current with the AC source turned on at the peak (90°). Measured peak inrush current is 33A, as shown in Figure 32.

FIGURE 32: PEAK INRUSH CURRENT



Legend:

Channel 3 (violet): AC input voltage

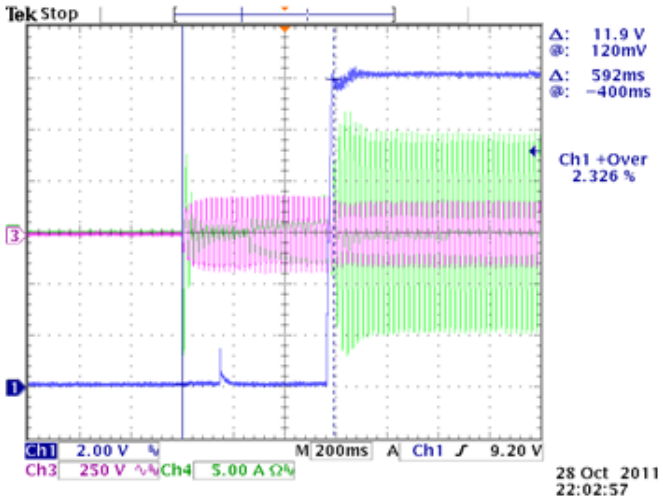
Channel 4 (green): AC input current

Power Supply Switch-on Delay

The switch-on delay is measured from the time AC voltage is applied to the power supply until the 12V output is regulated. The switch-on delay consists of two main components: the time required for the auxiliary power supply to start-up, and the time required to analyze the input voltage/frequency and perform a soft-start on the IPFC and DC/DC converters.

The switch-on delay at 110 VAC and 60A output load current is approximately 600 ms (Figure 33). The switch-on delay at 230 VAC and 60A output load current is approximately 720 ms (Figure 34).

FIGURE 33: SWITCH-ON DELAY VIN = 110 VAC, 60A OUTPUT LOAD CURRENT



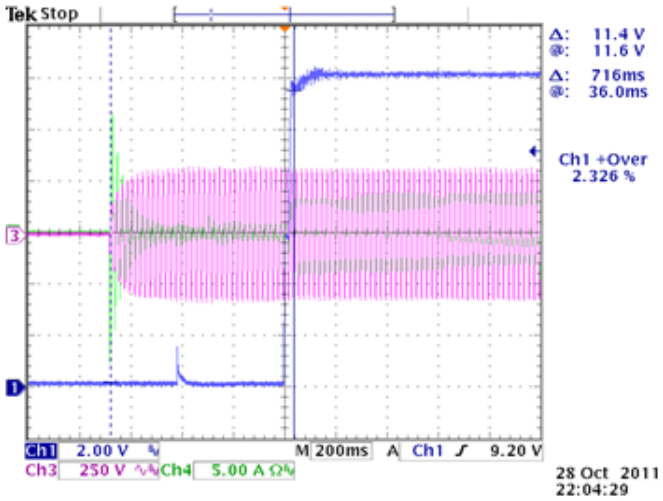
Legend:

Channel 1 (blue): 12V output voltage

Channel 3 (violet): AC input voltage

Channel 4 (green): AC input current

FIGURE 34: SWITCH-ON DELAY VIN = 230 VAC, 60A OUTPUT LOAD CURRENT



Legend:

Channel 1 (blue): 12V output voltage

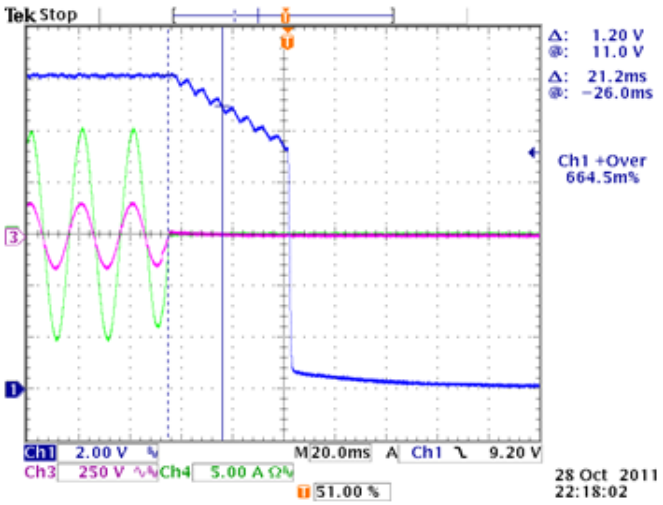
Channel 3 (violet): AC input voltage

Channel 4 (green): AC input current

Hold-up Time

The hold-up time is measured from the time AC power is lost, to the time the regulated output drops out of operating range. At 60A output load current, and at an input voltage of 110/230 VAC, the hold-up time was measured to be greater than 20 ms (see Figure 35 and Figure 36).

FIGURE 35: HOLD-UP TIME VIN = 110 VAC, 60A OUTPUT LOAD CURRENT



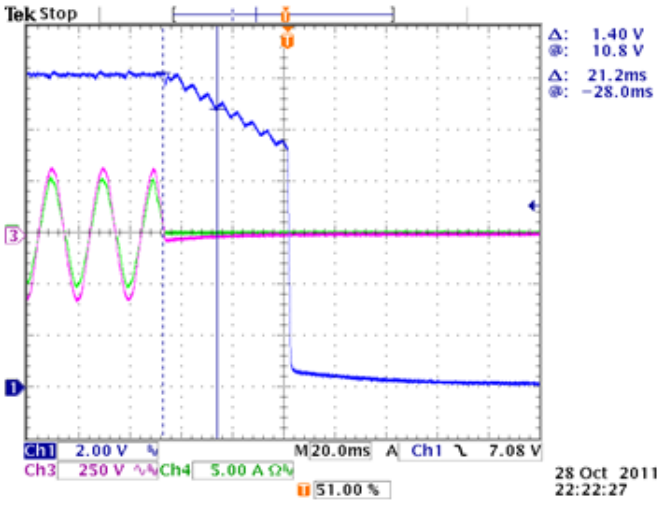
Legend:

Channel 1 (blue): 12V output voltage

Channel 3 (violet): AC input voltage

Channel 4 (green): AC input current

FIGURE 36: HOLD-UP TIME VIN = 230 VAC, 60A OUTPUT LOAD CURRENT



Legend:

Channel 1 (blue): 12V output voltage

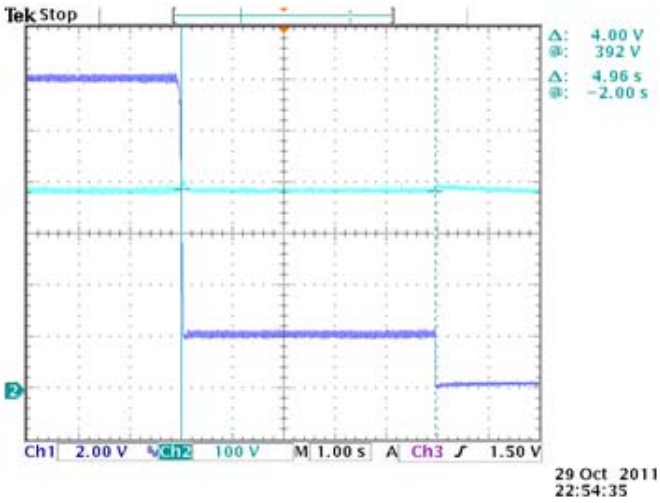
Channel 3 (violet): AC input voltage

Channel 4 (green): AC input current

Overcurrent Protection

In the event of an overcurrent condition the maximum output load current is sustained for five seconds before the output voltage is disabled, as shown in Figure 37. This shutdown event is programmable and has been selected for five seconds for demonstration purposes.

FIGURE 37: OVERCURRENT TEST VIN = 230 VAC, 64A OUTPUT LOAD CURRENT



Legend:

Channel 1 (blue): 12V Output Voltage

Channel 2 (light blue): DC Bus Voltage

EMI Performance

Figure 38 shows the pre-measured graph of the EMI characteristic. This test was performed on an open-frame board without an enclosure.

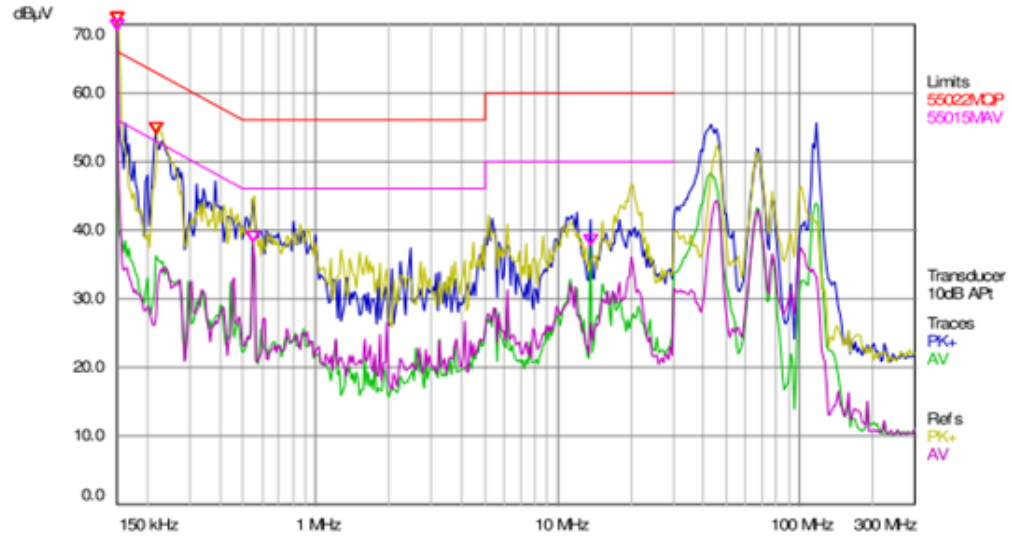
The EN55022 standard is typically defined between 150 kHz and 30 MHz. As general rule, the frequencies shown can be split into three major sections:

- Switching Band between 150 kHz to 1 MHz
- Diode Band up to approximately 20 MHz
- MOSFET band up to approximately 30 MHz

The pre-measurement graph shown in Figure 38 also covers the frequency band up to 300 MHz to discover potential layout and/or component issues.

FIGURE 38: EMI CHARACTERISTIC

Pre-measurement Graph



Peak Search Results

Trace	Frequency (MHz)	Level (dBµV)	Limit (dBµV)	Delta Limit (dB)	Delta Ref (dB)	Comment
1 PK+	0.15	81.59 *	66.00	15.59	1.12	L1 gnd
2 AV	0.15	69.11 *	56.00	13.11	0.10	L1 gnd
1 PK+	0.216	54.07	62.97	-8.90	9.24	L1 gnd
2 AV	0.55	38.31	46.00	-7.69	0.29	L1 gnd
2 AV	13.65	37.87	50.00	-12.13	11.32	L1 gnd

NOTES:

APPENDIX D: KNOWN ISSUES

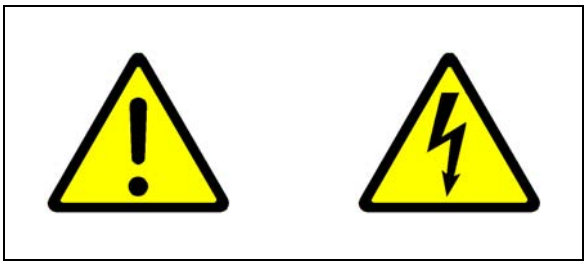
This appendix provides information on all known issues and items not yet implemented.

The following features have not been implemented:

- Output power derating for temperature
- System restart from over temperature condition

NOTES:

APPENDIX E: SAFETY NOTICES



The following safety notices and operating instructions should be observed to avoid a safety hazard. If in any doubt, consult your supplier.

WARNING – This reference design must be earthed (grounded) at all times.

WARNING – The reference design should not be installed, operated, serviced, or modified except by qualified personnel who understand the danger of electric shock hazards and have read and understood the user instructions. Any service or modification performed by the user is done at the user's own risk and voids all warranties.

WARNING – It is possible for the output terminals to be connected to the incoming AC mains supply and may be up to 410V with respect to ground, regardless of the input mains supply voltage applied. These terminals are live during operation AND for some time after disconnection from the supply. Do not attempt to access the terminals or remove the cover during this time.

General Notices

- The reference design is intended for evaluation and development purposes and should only be operated in a normal laboratory environment as defined by IEC 61010-1:2001
- Clean with a dry cloth only
- Operate flat on a bench, do not move during operation and do not block the ventilation holes
- The reference design should not be operated without all of the supplied covers fully secured in place
- The reference design should not be connected or operated if there is any apparent damage to the unit

NOTES:

APPENDIX F: THIRD PARTY CONSULTANT

Company Profile of APtronic Adaptive Power Solutions AG, Germany

The development of the Platinum-rated AC/DC reference design was a cooperative project to analyze and benchmark the capabilities of digital control loops in real-world applications with stringent requirements.

APtronic develops and produces customized power converters, inverters and universal power supplies for telecom and industrial applications.

Aptronic has locations in the US, Europe and Asia. It is ISO 9001 certified and a member of the Power Sources Manufacturers Association (PSMA).

Founded: September 2000

Legal entity: Corporation

Board of Directors: Walter Knittel (CEO), Theodor Schulte (COO)

Address: APtronic AG, An der Helle 26, 59505 Bad Sassendorf-Lohne, Germany

For more information visit http://www.aptronic.de/

NOTES:

APPENDIX G: REVISION HISTORY

Revision A (January 2012)

This is the initial release version of this document.

Revision B (June 2012)

The **"Software Overview"** section was extensively updated.

Appendix F: "Third Party Consultant" was added.

Minor updates to text and formatting were incorporated throughout the document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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